Silicon Systems®
A Texas Instruments Company

SSI 34P3410
11.25 to 60 Mbit/s Read Channel with Adaptive Threshold Qualifier

Prototype

March 1997

DESCRIPTION

The SSI 34P3410 device is a high performance BiCMOS single chip read channel IC that contains all the functions necessary to implement a complete zoned recording system. Functional blocks include a pulse detector with adaptive threshold qualifier, programmable filter, 4-burst servo capture, Time Base Generator, and Data Synchronizer. NRZ data rates from 7.5 - 40 Mbit/s, (Raw Data rate from 11.25 to 60 Mbit/s), can be programmed by digital commands without external component switching.

The SSI 34P3410 allows complete flexibility in read channel configuration. All critical parameters can be programmed by a microprocessor via a bi-directional serial port and a bank of internal registers. Thus, a low component count and low cost zoned recording system can be implemented.

The SSI 34P3410 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL

- **7.5 to 40 Mbit/s NRZ data**
- **Bi-directional serial port for access to internal registers**
- **Complete zoned recording application support**
- **Low power operation (600 mW typical @ RRC = 60 MHz and 5 V)**
- **Programmable power management (sleep mode < 5 mW)**
- **Power supply range (4.5 to 5.5 V)**
- **Small footprint 48-pin TSSOP package**

PULSE DETECTOR

- **Temperature compensated, exponential control AGC**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low drift AGC hold circuitry**
- **Adaptive threshold qualifier for data extraction**
- **Traditional window qualifier for timing extraction**
- **Programmable pulse qualification threshold level**
- **CMOS RDIO signal output for servo timing support**
- **Internal LOW-Z and fast decay timing for rapid transient recovery and AGC acquisition**
- **Fast decay mode is self-timed for optimal AGC recovery**
- **0.5 ns max pulse pairing with sine wave input**
- **Independent window voltage qualification threshold in servo and data modes**
- **Independent qualification thresholds for data and timing extraction**

SERVO CAPTURE

- **4-burst servo capture with, A-B, and C-D output**
- **Internal servo burst hold capacitors**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 2.25 to 13.5 MHz**
- **Programmable boost of 0 to 13 dB**
- **Programmable group delay equalization of ±30%**
- **Independent cutoff frequency setting in data mode and servo mode**
- **Independent boost setting in data mode and servo mode**
- **Matched normal and differentiated outputs**

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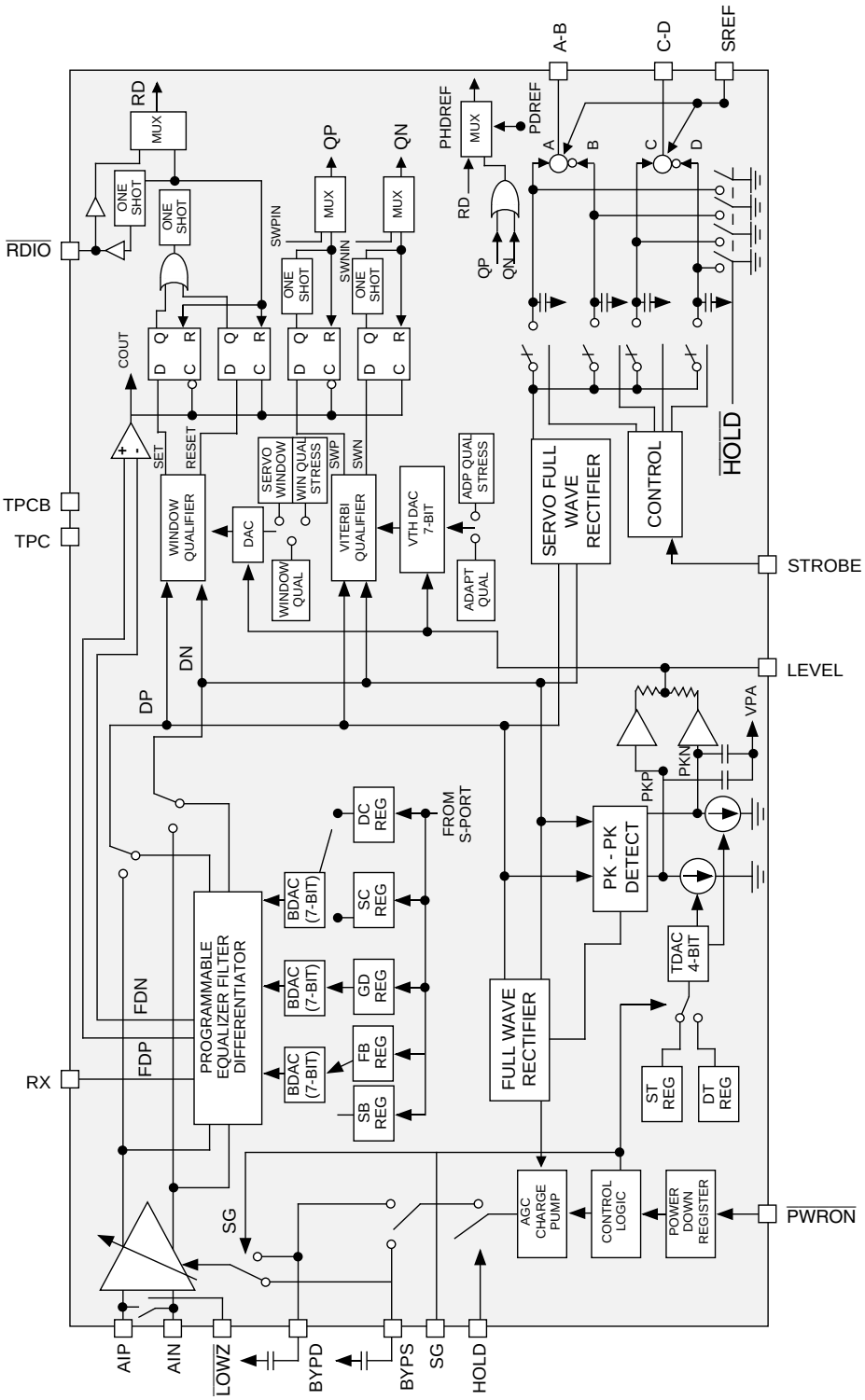
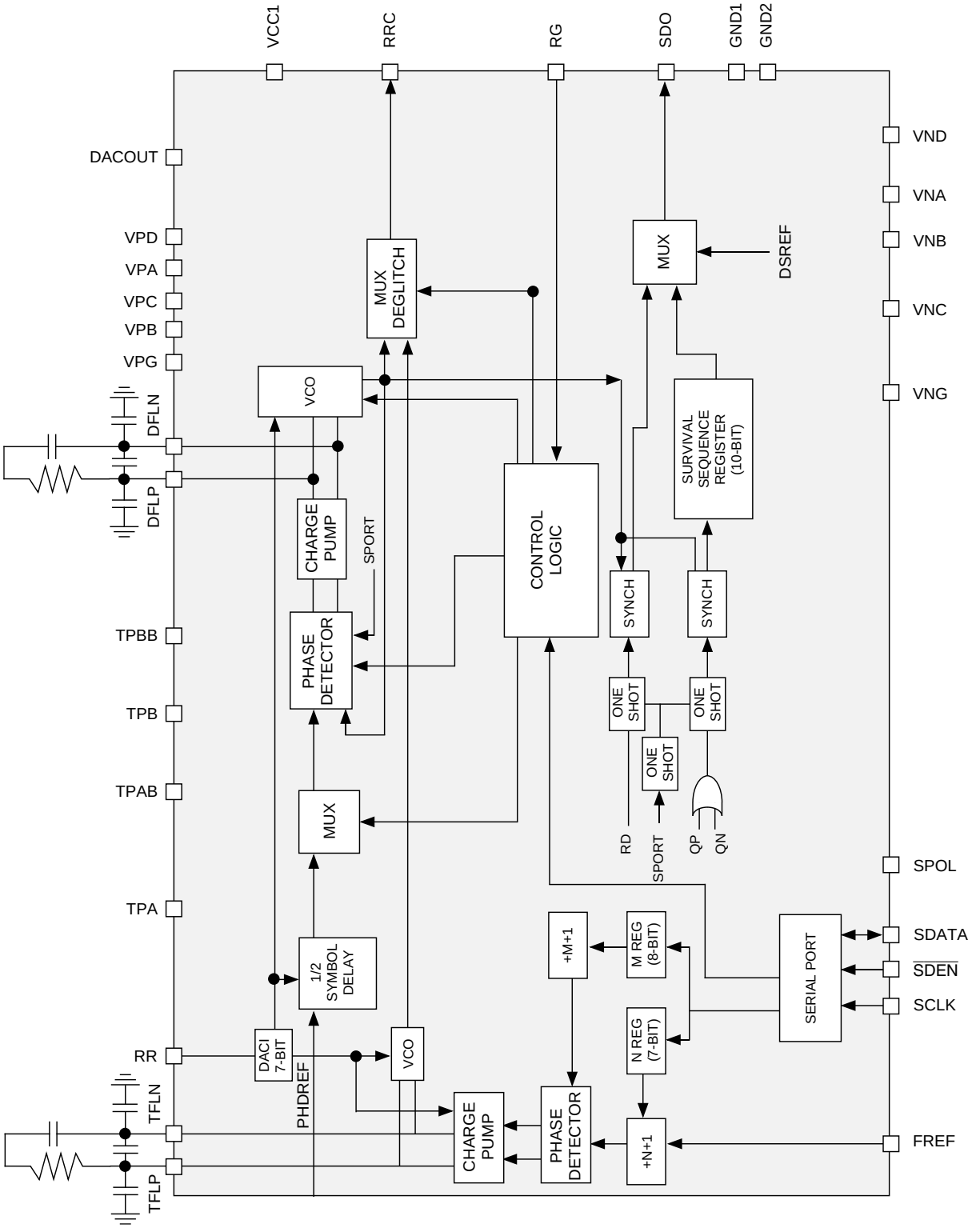
BLOCK DIAGRAM - FRONT END



BLOCK DIAGRAM - BACK END



FEATURES (continued)

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 60 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to Data Synchronizer VCO

DATA SYNCHRONIZER

- Fully integrated Data Synchronizer
  - No external delay lines or active components required
  - No external active PLL components required
- Selectable PLL input from adaptive threshold qualifier or traditional window qualifier
- Selectable Data Synchronizer input from adaptive threshold qualifier or traditional window qualifier
- Fast PLL acquisition phase lock loop
  - Zero phase restart technique
  - Phase detector gain gear shift
- Programmable decode window symmetry
  - Window shift control ±20% of decode window
  - Includes delayed read data and VCO reference monitor points

FUNCTIONAL DESCRIPTION

The SSI 34P3410 is a complete high performance read channel device with the following functions:

- AGC loop including a variable gain amplifier and programmable active filter
- Adaptive threshold and classic window pulse qualification
- 4-burst servo demodulator
- Time Base Generator
- Data Synchronizer

It supports NRZ data rates from 7.5 to 40 Mbit/s, (i.e., raw data rate from 11.25 - 60 Mbit/s). Designed for low power applications, it allows completely flexible power management. See the block diagrams of the device on the previous pages.

Most critical system parameters are user-programmable by writing to a bank of 8-bit registers. These registers can be written to or read back via a 3-line bi-directional serial interface. Upon application of power to the device, these registers power up in the default state shown in table 2.4. The state of the serial port is unchanged when the part goes into sleep mode.

AGC AND PULSE DETECTOR DESCRIPTION

The adaptive threshold qualifier, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wideband variable gain amplifier, a wide band and high precision fullwave rectifier, a dual rate charge pump, and an advanced adaptive threshold qualifier. The entire signal path is fully-differential to minimize external noise pick up.

AGC Circuit

The AGC is designed to maintain the peak-to-peak amplitude at the filter output at 1 Vp-p. The Filter output, DP/DN, can be monitored at the differential testpoints TPC and TPCB. With an asymmetrical read signal, the peak-to-peak differential signal at DP/DN will be less than 1 Vp-pd since the AGC circuit is based on the fullwave rectified DP/DN.

The AGC amplifier gain is controlled by the voltage at:

- The BYPD pin if SG = ‘0’, e.g., in non-servo mode or
- The BYPS pin if SG = ‘1’, e.g., in servo mode

External integrating capacitors, CBYPD and CBYPS, should be connected between VCC and the BYPD pin and the BYPS pin, respectively.

In non-servo mode, a dual rate charge pump drives CBYPD with a charging/discharging current that depends on the instantaneous differential voltage at the DP/DN pins, and in servo mode the charge pump drives CBYPS.

Attack currents, out of CBYPD, lower VBYPD which reduces the amplifier gain, while decay currents, into CBYPD, increase VBYPD which increases the amplifier gain. When the signal at DP/DN is greater than 1 Vp-pd (volt peak-to-peak differential), the nominal attack current of 0.13 mA is used to reduce the amplifier gain. If the signal is greater than 1.25 Vp-pd, a fast attack current of 1.04 mA is sunk to reduce the gain.