Abridged Version

Silicon Systems®
A Texas Instruments Company

SSI 34P3402A

8 to 53 Mbit/s Read Channel w/Adaptive Threshold Qualifier

Preproduction

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DESCRIPTION

The SSI 34P3402A device is a high performance BiCMOS single chip read channel IC that contains all the functions necessary to implement an adaptive threshold read channel. Functional blocks include a pulse detector with adaptive threshold qualifier, programmable filter, and data synchronizer. Raw data rates from 8 to 53 Mbit/s can be programmed by digital commands.

The SSI 34P3402A allows complete flexibility in read channel configuration. All critical parameters can be programmed by a microprocessor via a bi-directional serial port and a bank of internal registers.

The SSI 34P3402A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **8 to 53 Mbit/s raw data rate**
- **Bi-directional serial port for access to internal registers**
- **Low power operation (<TBD mW typical @ RRC = 53 MHz and 5 V)**
- **Programmable power management (sleep mode <1 mW)**
- **Power supply range (4.5 to 5.5 V)**
- **Small footprint 48-Pin TQFP package**

PULSE DETECTOR

- **Temperature compensated, exponential control AGC**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low drift AGC hold circuitry**
- **Programmable AGC fixed gain mode**
- **Adaptive threshold qualifier for data extraction**
- **Traditional window qualifier for timing extraction**
- **Programmable pulse qualification threshold level**
- **CMOS RDIO signal output for servo timing support**
- **Internal LOW-Z and fast decay timing for rapid transient recovery and AGC acquisition**
- **Fast decay mode is self-timed for optimal AGC recovery**
- **0.5 ns maximum pulse pairing with sine wave input**
- **Independent qualification thresholds for data and timing extraction**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 2 to 16 MHz**
- **Programmable boost of 0 to 13 dB**
- **Programmable group delay equalization (up to 38% change in group delay)**
- **Matched normal and differentiated outputs**
- **±10% Fc accuracy from 10 to 16 MHz**
- **Less than 1% total harmonic distortion**

DATA SYNCHRONIZER

- **Fully integrated data synchronizer**
  - **No external delay lines or active components required**
  - **No external active PLL components required**
- **Selectable PLL input from adaptive threshold qualifier or traditional window qualifier**
- **Selectable data synchronizer input from adaptive threshold qualifier or traditional window qualifier**
- **Fast PLL acquisition phase lock loop**
  - **Zero phase restart technique**
  - **Programmable phase detector gain gear shift**
- **Programmable decode window symmetry**
  - **Window shift control ±15% of decode window**
  - **Includes delayed read data and VCO reference monitor points**

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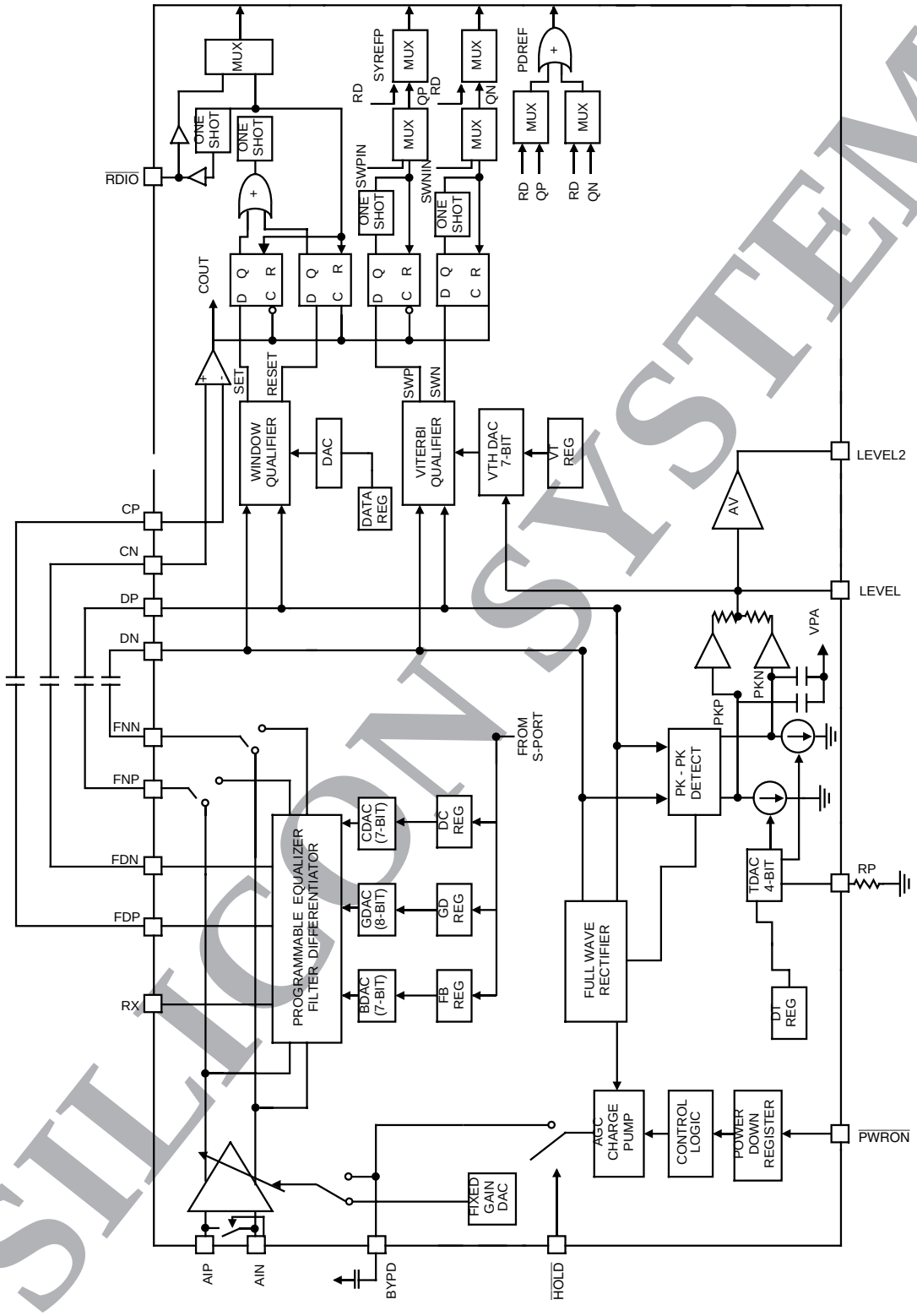
BLOCK DIAGRAM A



BLOCK DIAGRAM B