

January 1997

## DESCRIPTION

The SSI 34P3400 device is a high performance BiCMOS single chip read channel IC that contains all the functions necessary to implement a complete zoned recording disk drive system. Functional blocks include a pulse detector with adaptive threshold qualifier, programmable filter, 4-burst servo capture, time base generator, and data synchronizer with raw data interface. Raw data rates from 9 to 45 Mbit/s can be programmed by digital commands without external component switching.

The SSI 34P3400 allows complete flexibility in read channel configuration. Essentially all critical parameters can be programmed by a microprocessor via a bi-directional serial port and a bank of internal registers. Thus, a low component count and low cost zoned recording system can be implemented.

The SSI 34P3400 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

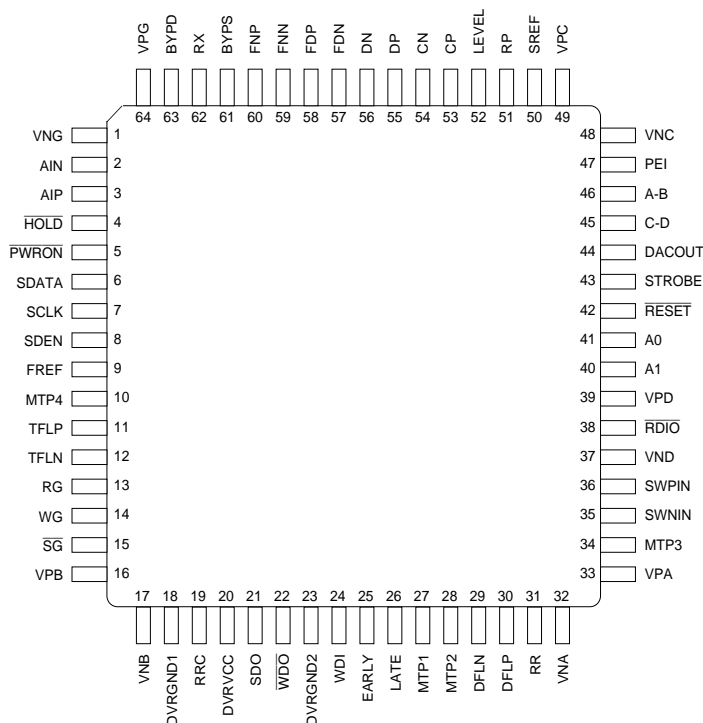
## FEATURES

### GENERAL

- **9 to 45 Mbit/s raw data rate**
- **Bi-directional serial port for access to internal registers**
- **Complete zoned recording application support**
- **Low power operation (600 mW typical @ 45 Mbit/s and 5 V)**
- **Programmable power management (sleep mode < 1 mW )**
- **Power supply range (4.5 to 5.5 V)**
- **Small footprint 64-Lead TQFP package**

(continued)

## PIN DIAGRAM

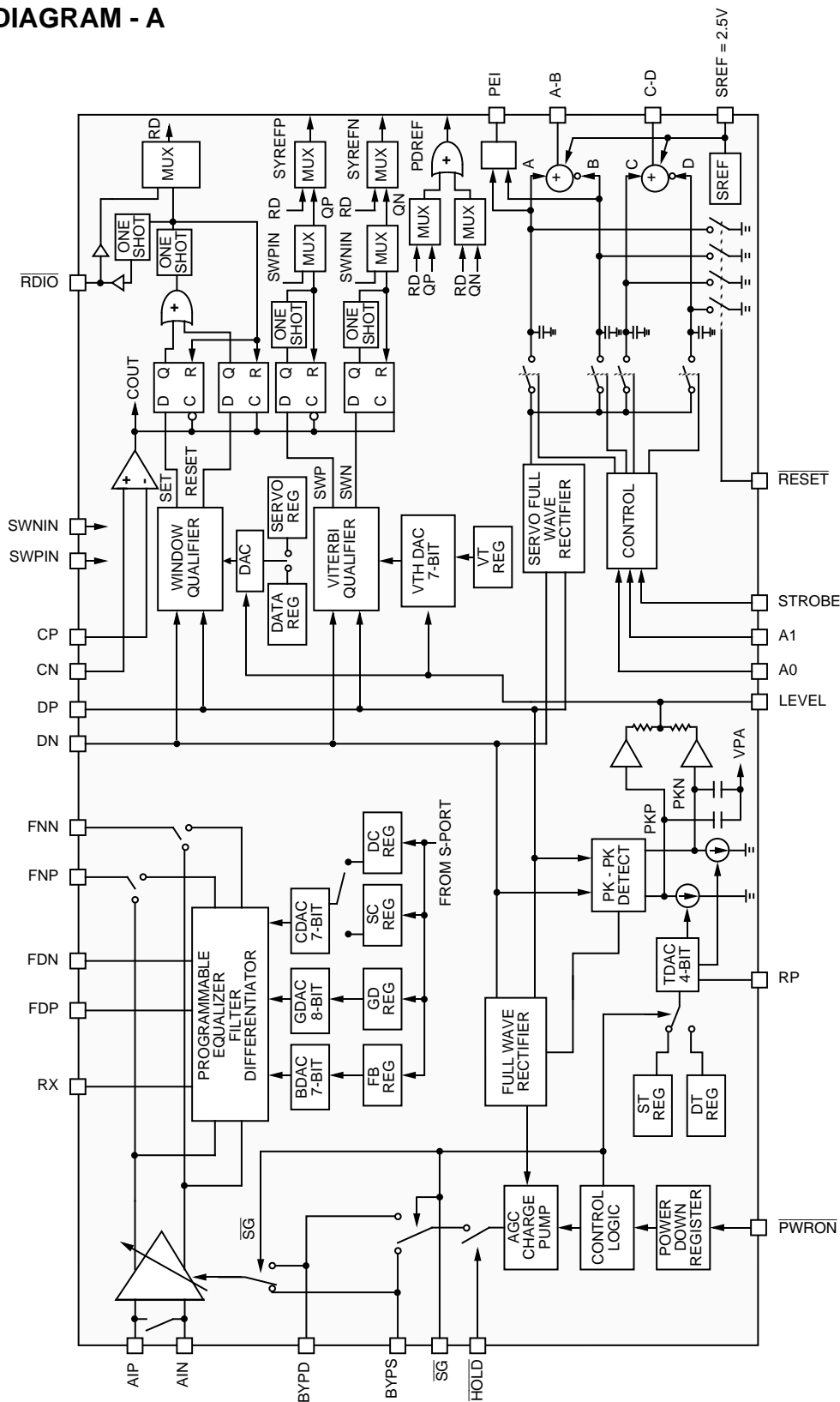


64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 34P3400  
45 Mbit/s Read Channel  
w/Adaptive Threshold Qualifier

BLOCK DIAGRAM - A



### BLOCK DIAGRAM - B



# SSI 34P3400

## 45 Mbit/s Read Channel

### w/Adaptive Threshold Qualifier

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#### FEATURES (continued)

##### AGC

- Temperature compensated, exponential control AGC
- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low drift AGC hold circuitry
- Internal LOW-Z and fast decay timing for rapid transient recovery and AGC acquisition
- Fast decay mode is self-timed for optimal AGC recovery

##### PULSE DETECTOR

- Adaptive threshold qualifier for data extraction
- Traditional window qualifier for timing extraction
- Programmable pulse qualification threshold level
- CMOS  $\overline{\text{RDIO}}$  signal output for servo timing support
- 0.5 ns max pulse pairing with sine wave input
- Independent window voltage qualification threshold in servo & data modes
- Independent qualification thresholds for data and timing extraction

##### SERVO CAPTURE

- 4-burst servo capture with PEI output, A-B, and C-D output
- Internal servo burst hold capacitors

##### PROGRAMMABLE FILTER

- Programmable cutoff frequency of 2 to 16 MHz
- Programmable boost of 0 to 13 dB
- Programmable group delay equalization (up to 30% change in group delay)
- Independent cutoff frequency setting in data mode and servo mode
- Boost setting available in data mode and servo mode
- Matched normal and differentiated outputs
- $\pm 10\%$   $f_c$  accuracy from 10 to 16 MHz
- Less than 1% total harmonic distortion from 10 to 16 MHz
- Less than 1.5% total harmonic distortion from 2 to 10 MHz

#### TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 90 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

#### DATA SYNCHRONIZER

- Fully integrated data synchronizer
  - no external delay lines or active components required
  - no external active PLL components required
- Selectable PLL input from adaptive threshold qualifier or traditional window qualifier
- Selectable data synchronizer input from adaptive threshold qualifier or traditional window qualifier
- Fast PLL acquisition phase lock loop
  - zero phase restart technique
  - programmable phase detector gain gear shift
- Programmable decode window symmetry
  - window shift control  $\pm 30\%$  of decode window
  - includes delayed read data and VCO reference monitor points
- Programmable write precompensation
- External/Internal write precomp control
- PLL and data detection circuits capable of operating with d = 0 encoding