Silicon Systems®
A Texas Instruments Company

SSI 34P3216B
Read Preamp/Channel for Tape Storage

Prototype

February 1997

DESCRIPTION

The SSI 34P3216B integrates all the functions needed for a tape read channel and write driver: preamplifier, automatic gain control (AGC), equalization filter, pulse qualifier, raw-data monostable, power supply monitors, and an H-bridge write driver. Each major functional block may be programmed through a serial port interface and on-chip CMOS data registers.

MR bias current, gain, filter characteristics, pulse qualifier hysteresis, and write current parameters can be controlled via the 10 programmable registers. In addition, programmable test modes allow the preamp, AGC, and filter to be individually bypassed or tested in combination.

The AGC section controls the input signal level to the filter, and includes a voltage-controlled gain amplifier, full-wave rectifier, and dual-rate charge-pump. The AGC circuit has a 28 dB gain range, and may be forced to a fixed-gain mode by a control bit in the AGC control register. The dual-rate charge pump insures fast gain acquisition after mode transitions.

The 7-pole, linear-phase, 0.05° equiripple low-pass filter features 0.4 to 4.0 MHz program-mable cutoff frequency, and symmetrical/unsymmetrical pulse slimming capability. Filter cutoff frequency is trimmed at wafer probe to insure accuracy. Filter functions are controlled by 7-bit DACs for superior resolution, and DC coupling with internal offset correction loops eliminate the need for external coupling capacitors.

The pulse qualifier has two modes of operation: dual comparator, and hysteresis mode. In hysteresis mode, a qualified peak of one polarity must be followed by a qualified peak of opposite polarity before detection of another peak of the same polarity is allowed. Detection threshold levels are set by a 7-bit DAC.

The write driver is an H-bridge configuration, and write current is programmable from 5 to 30 mA with a 5-bit DAC. An on-chip power supply monitor shuts down the driver if the VCC supply voltage falls below a predetermined value.

The device requires a single nominal +5 V power supply, and features a micropower shutdown mode.

The SSI 34P3216B utilizes an advanced 1.0µ BiCMOS process technology, and is available in a 48 SSOP package.

FEATURES

- **Inductive or MR head interface**
- **MR bias current range of 4 to 20 mA in 0.25 mA steps (6 bits)**
- **Input noise = 1.5 nV/√Hz max**
- **Input capacitance = 19 pF max**
- **Selectable gain = 34 dB or 40 dB**
- **Locked 0 dB gain capability**

AUTOMATIC GAIN-CONTROLLED-AMPLIFIER (AGC)

- **Gain control range of 28 dB**
- **Locked 0 dB gain capability**
- **Gain hold mode with controlled drift**
- **Precision full-wave rectifier with peak detect output (LEVEL)**
- **Programmable peak detector droop current from 3 to 50 µA in 3.1 µA steps (4 bits)**
- **Programmable charge punp currents over a 4-to-1 range in 4 steps (2 bits)**
- **Fast attack/decay modes at read/write transitions for rapid gain acquisition**
- **Fast recovery mode at power-up to minimize transitions**

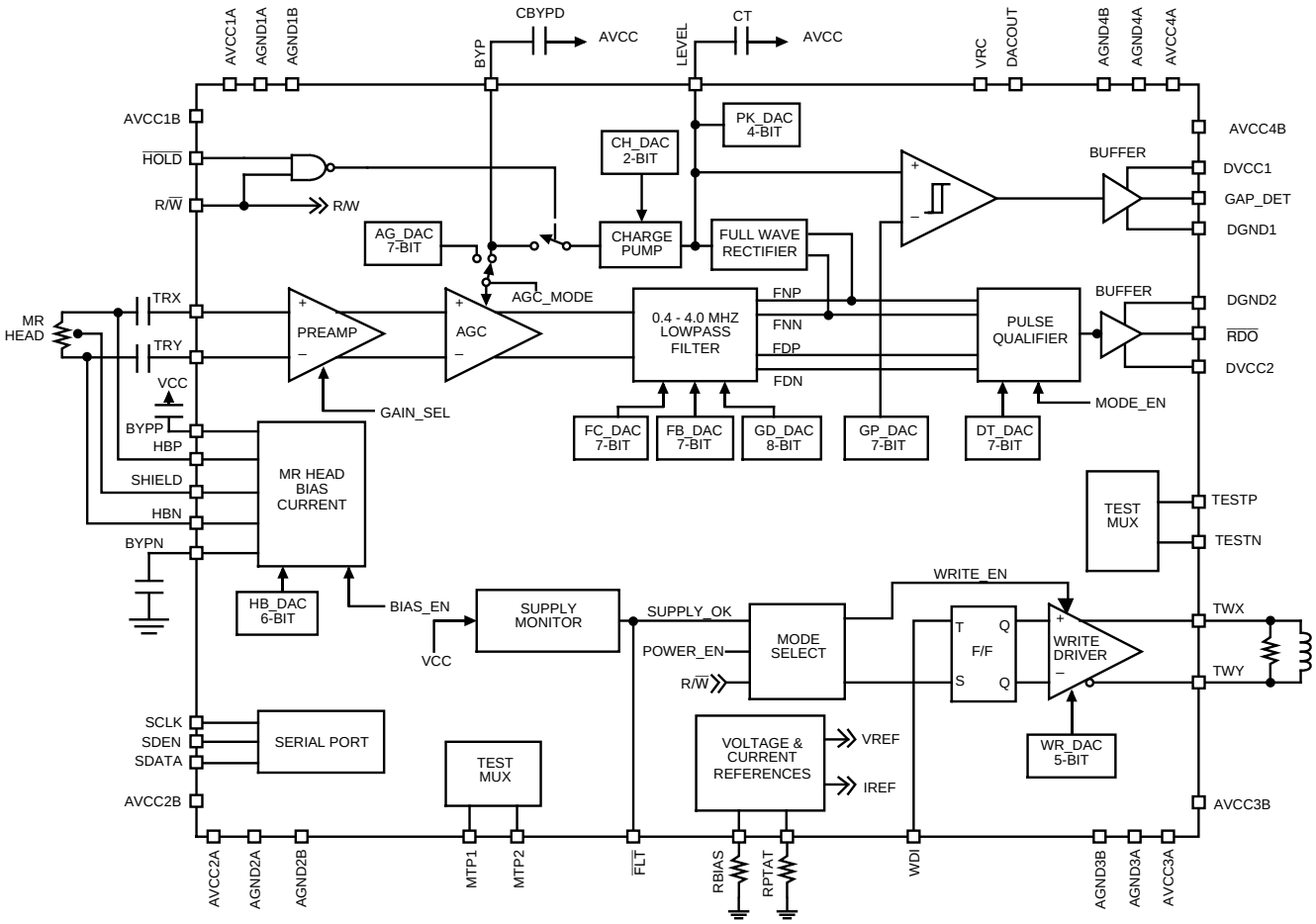
PROGRAMMABLE EQUALIZATION FILTER

- **7-pole equi-ripple lowpass filter with 2 symmetric zeros slimming**
- **Programmable cutoff frequency from 0.4 to 4 MHz in 28 kHz steps (7 bits)**
- **Programmable boost/equalization from 0 to 13 dB in 0.1 dB steps (7 bits)**
- **Programmable group delay Δ% from -20 to +20 % in 0.3% steps (7 bits)**
- **Locked 0 dB gain capability**
- **Normal and differentiated output signals**

(continued)

SSI 34P3216B
Read Preamp/Channel for Tape Storage

BLOCK DIAGRAM



FEATURES (continued)

PULSE QUALIFIER

- Choice of dual-comparator or hysteresis mode qualification
- Choice of fixed threshold or variable threshold scaled by LEVEL
- Buffered $\overline{\text{RDO}}$ (raw data out) CMOS-compatible output

GAP DETECT CIRCUIT

- Fault threshold range from 10% to 90% of nominal level in 0.63% steps (7 bits)
- Buffered $\overline{\text{FLT}}$ CMOS-compatible output

HEAD WRITE DRIVER

- Write current range from 5 to 30 mA in 0.8 mA steps (5 bits)
- Head output voltage swing = 3 V peak minimum

POWER SUPPLY MONITOR

- Write driver inhibited for values of VCC below 3.8 V
- CMOS $\overline{\text{FLT}}$ logic output to indicate low VCC

PROGRAMMABILITY AND TEST MODES

- Full functional and parametric programmability through serial port interface
- Single or combination block bypassing
- Differential analog test points with access to major functional block outputs
- PECL digital test points to monitor internal logic signals

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914