Silicon Systems®
A Texas Instruments Company

SSI 39C1011
1394 Native Bridge Link Controller

Prototype

January 1998

DESCRIPTION

Housed in a 100 pin TQFP package, the SSI 39C1011 is a member of the Silicon Systems chip set enabling an ATA/ATAPI device to be interfaced via the 1394 serial bus. Operating at 5 volts, the SSI 39C1011 directly interfaces with an external PHY chip to communicate over a 1394 serial bus. State machine controller inside the 39C1011 manages all incoming and outgoing packets. Full data buffering enables error detection and recovery. When a previously received data block is being transferred out of the data buffer on one interface, the next data block can be received into the data buffer from the other interface in order to reduce latency.

An external DSP has full control over the operation of the SSI 39C1011. A shared paremeter resource called the PRAM buffer (64 x 32 bit configuration) is managed

(continued)

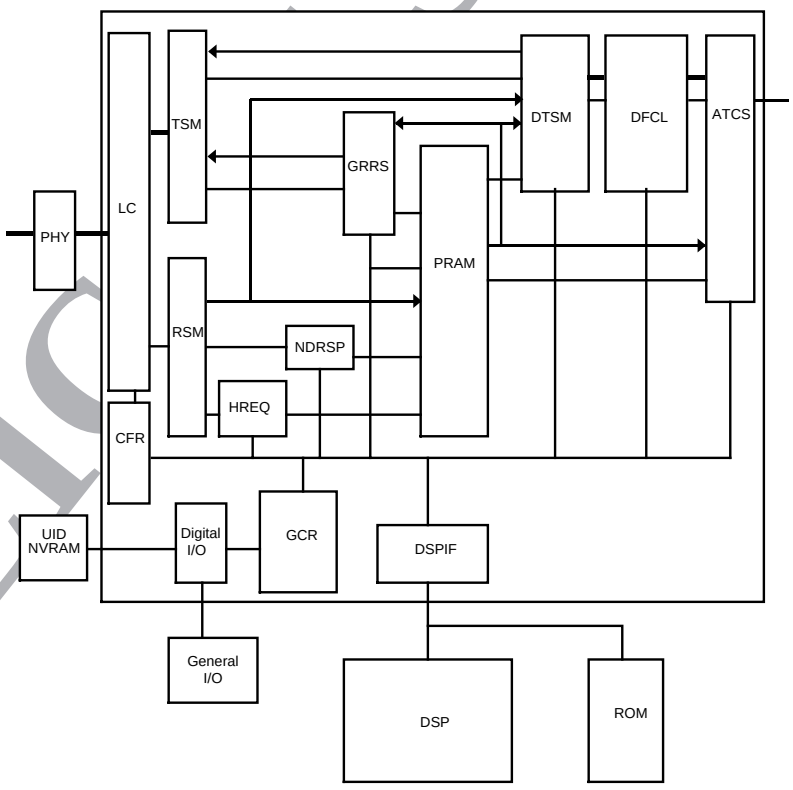
FEATURES

1394 INTERFACE

- **Implements a fully compliant 1394 Link Interface**
- **Transmits and receives 1394 packets in asynchronous mode**
- **Contains a 4 kilobyte (1024 words by 32 bits) data FIFO for optimal transfer performance**
- **Support speeds of 100, 200 and 400 Mbit/s**
- **Interfaces directly to Texas Instruments TSB11C01, TSB11LV01, TSB21LV03, TSB41LV03 and TSB41LV06 Phy chips**

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

by the DSP to send or store packets. To receive a packet in the PRAM, the DSP allocates the PRAM address and maximum length to HREQ and/or NDRSP. To send a packet, the DSP constructs it in the PRAM. It then writes the PRAM address and length to the GRRS.

For data transfers from the initiator to the device, the DSP constructs a two quadlet header for the read request in the PRAM. It then writes the PRAM address to the DTSM. The DTSM constructs and sends this packet out and waits for a response from the initiator. When it receives the response, it stores the header in the PRAM and the data in the DFCL FIFO. It then notifies the DSP that the transaction is done.

For data transfers from the device to the initiator, the DSP constructs a two quadlet header for the write request in the PRAM. It then writes the PRAM address to the DTSM. The DTSM constructs and sends this packet header followed by the data in the DFCL FIFO as specified by the data length field. It waits for an acknowledgement complete or write response from the initiator to complete the packet. It then notifies the DSP that the transaction is done.

For the DSP to write to the ATA/ATAPI task files or send a packet command (ATAPI), it can construct the information in the PRAM. It then writes to the ATCS the address to read the contents. Alternatively, the DSP can read or write individual ATA/ATAPI registers directly via the DSPIF.

FEATURES (continued)

ATA/ATAPI INTERFACE

- Support PIO modes 0-4 and DMA modes 0 – 2 under DSP control
- ATA/ATAPI task file register access, automatic or manual mode under DSP control
- Support for up to 2 Logical units under DSP control

SBP-2 PROTOCOL

- Support for multiple initiators
- Implements SBP-2 command fetch, decode and execution under DSP control
- UID ROM interface and password storage

DSP INTERFACE

- 16 bit data bus support
- Supports multiple processor types including TMS320Cxx DSPs
- Direct Read and write access of all registers and Parameter RAM
- Maskable interrupt attention to DSP device
- Wait state handshake

AUTOMATION CAPABILITIES

- Automated 1394 transmit and receive transactions including CRC generation and checking
- Automated data transfers between ATA interface and 1394 serial bus, with manual control override

GENERAL

- 5 V operation.
- 4 general programmable I/O ports.
- Programmable clock source to DSP