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## DESCRIPTION

The SSI 39C1010 device is a CMOS integrated circuit housed in a 100 pin TQFP package. The device is a member of the Silicon Systems chip set enabling an ATA or ATAPI controller to be interfaced via the 1394 serial bus. Operating at five volts, the SSI 39C1010 directly interfaces with an external Phy chip to communicate over a 1394 serial bus. The SSI 39C1010 implements the SBP-2 protocol defined for "Tailgate" operation. State machine controller inside the SSI 39C1010 manages all incoming and outgoing packets transfer. Full packet data buffering enables packet error detection and 1394-ATA/ATAPI transfer speed matching. When a packet is being transferred, the next packet can be saved in the data buffer to enhance latency. The SSI 39C1010 manages all the 1394, SBP-2 and ATA/ATAPI activities automatically. No firmware or external controller is needed.

## FEATURES

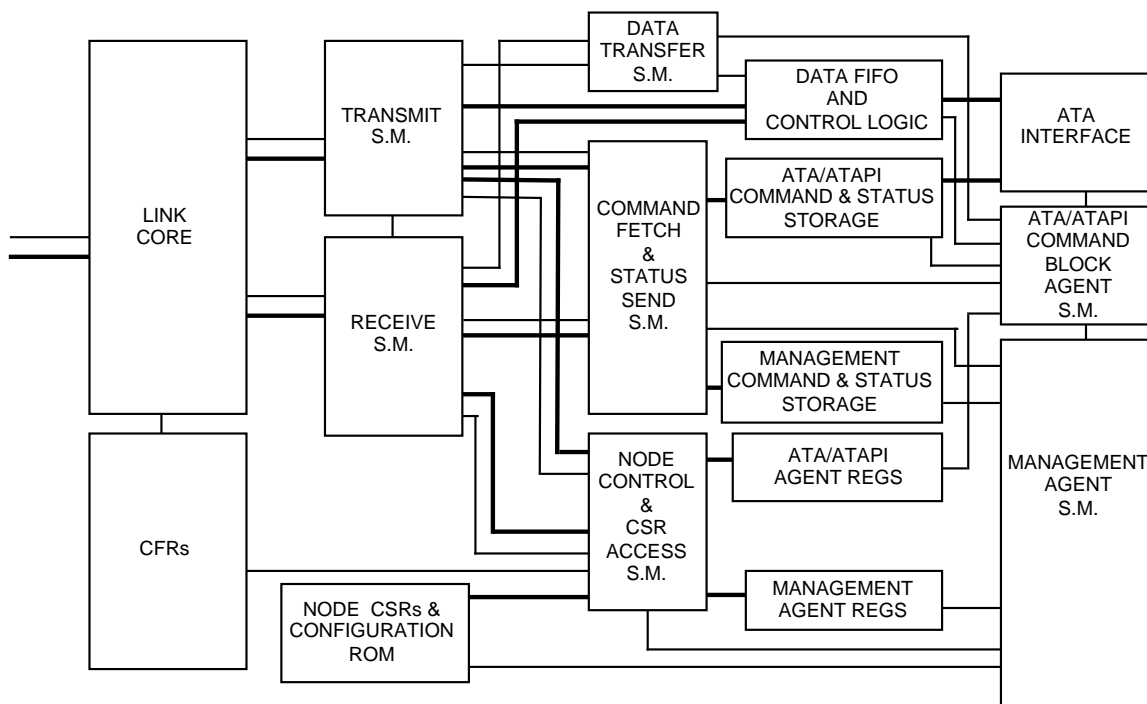
- **1394 Interface**
  - Transmits and receives 1394 packets in asynchronous mode
  - 4 KB data FIFO for optimal transfer performance
  - Supports speeds of 100, 200 and 400 Mb/s
  - Interfaces directly to TSB11C01, TSB11LV01 and TSB21LV03 Phy chips
- **ATA/ATAPI Interface**
  - Performs the function of an ATA/ATAPI host interface
  - Support PIO modes 0-4, DMA modes 0-2
- **SBP-2 protocol**
  - Implement SBP-2 management and command fetch, decode and execute
  - Implement SBP-2 and tailgate registers
  - Configuration ROM
- **General**
  - 5 V operation

# SSI 39C1010

## 1394-ATA/ATAPI Tailgate

## Link Controller

## BLOCK DIAGRAM



**Prototype:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

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