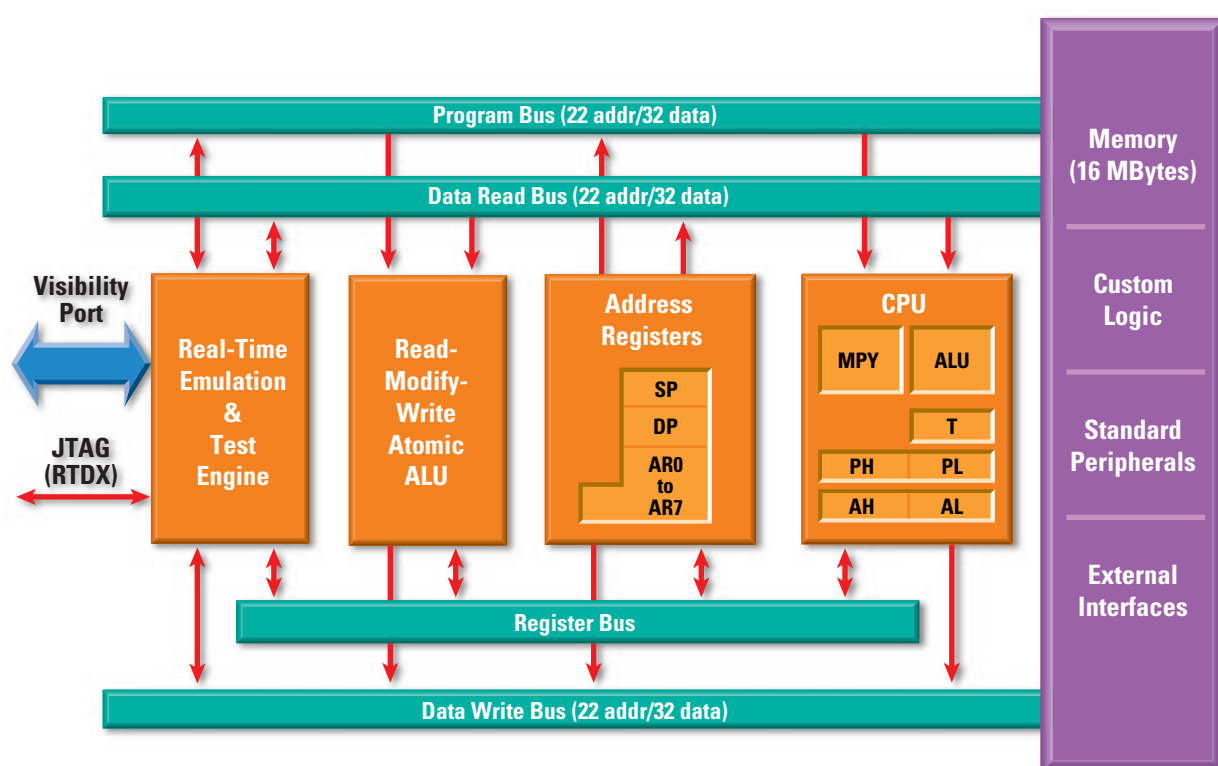


## Mass Storage Technology Fact Sheet

# TMS320C2700

### 'C2700: An Innovative Approach



Integrated 'C2700 core enables design of tomorrow's real-time systems today.

### Redefines DSP for Mass Storage World

With the new TMS320C2700 DSP, Texas Instruments introduces a breakthrough architecture that unites the flexibility, ease of use and cost-efficiency of an MCU with the high performance of a DSP — all in a single device.

The 'C2700 architecture has been custom built from the ground up to address the specific requirements of high-performance, high-precision mass storage electronics. This all-platform uniprocessor combines the efficient C language compiling, interface control and ease of programming capabilities found

in the most advanced MCUs with the precise servo/spindle control of DSPs.

TI's 'C2700 architecture features the best from both technologies, combining 100 MIPS of DSP performance with traditional MCU strengths of ease of software development, compactness of code and flexibility of interrupt handling. By incorporating this level of functionality, flexibility and power in a cost-effective, single-chip solution, the new 'C2700-based DSPs provide a future-ready solution to the ever-increasing performance and time-to-market demands of tomorrow's sophisticated mass storage applications.

### The 'C2700 core provides performance for advanced systems

Using TI's 0.25 micron CMOS process, the 'C2700 core is embedded in the ASIC back-plane for custom digital mass storage solutions. The core provides 100 MIPS of calculating power at 100 MHz, 5x the performance of any MCU currently in use for storage applications. TI plans to migrate the 'C2700 to its 0.18 micron Timeline technology and 150 MIPS in late 1998.

This advanced level of power provides today's customers with areal density leadership at a reasonable cost. Beyond this, it enables drive engineers to accommodate future performance

requirements brought on by emerging technologies, like microactuators, very high-speed motors, high-speed interface and 8x or greater DVDs. TI's low cost development path for the 'C2700 will carry designers through multiple product cycles without a major investment in firmware.

The new TI 'C2700 DSP core utilizes a modified Harvard architecture that can be addressed as a single software stack for Von Neumann operations. It features two data read busses and an instruction read bus, with several enhancements aimed at improving code density

and performance in interrupt-driven applications in the storage industry.

Offering the power of a high-performance RISC microprocessor, the core is optimized for real-time control and data processing in storage applications, providing an ideal computing engine for advanced controller development. It is completely compatible with advanced all-digital CMOS read channel technology, keeping the drive designer well ahead of the curve in the bits-per-inch race.

The 'C2700 provides this level of performance at no additional

cost in hardware, opening the door for developers to take optimum advantage of the DSP's advances in integration and power. Furthermore, it opens the door for the design team to focus on creating product innovation and differentiation that will drive the future of storage product electronics.

### ***Industry-leading code efficient architecture***

Optimized for both servo and interface system control, the 'C2700 architecture features efficient addressing modes and specialized instructions that combine to produce the highest level of code compactness in the industry. More compact code executes faster, consumes less power and reduces memory cost.

To help maintain this level of code density, the 'C2700 architecture has been designed to utilize read-modify-write operations. A single instruction directs the processor to read data from memory, modify it and write it back to memory. Virtually all MCUs require three or more steps to perform this common embedded system I/O operation. This single, or atomic, instruction provides a distinct advantage over traditional load-store or RISC architectures because it generates less code, executes the code faster and protects the operation from being corrupted by interrupts. With the 'C2700 devices, these logical or arithmetic operations can be performed on any memory location.

In developing the 'C2700 architecture, existing firmware code for all major drive manufacturers was closely examined. Virtually all of the most commonly used instructions were implemented as part of the 'C2700's final instruction set, allowing drive designers to work as they have with previous generations of less capable MCUs. TI has also developed a family of tools to port existing legacy code to this new platform to further reduce development time and costs.

## **Architecture Feature Summary**

### **General features**

- 16-bit, fixed point architecture
- 100 MIPS performance in a 3V, 0.25-micron version
- 10 ns instruction cycle time
- 32-bit on-chip data bus fetches two words in a single cycle
- Register-based architecture
- 16- or 32-bit instructions with total address space equal to 16 MB
- Dedicated stack pointer

### **DSP features**

- Separate program and data busses (modified Harvard architecture)
- 16x16-bit multiplier
- Single-cycle multiply and accumulate (MAC)
- Saturation instructions and modes

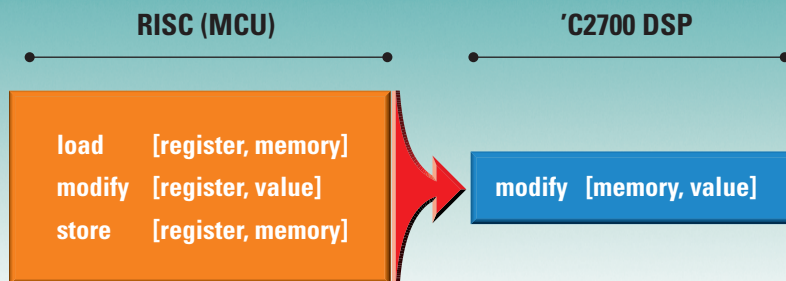
### **MCU features**

- Configurable in Von Neumann mode (combined bus)
- Single-cycle, atomic, read-modify-write operations (logical and arithmetic)
- Automatic context save and restore for fast interrupt response
- Fast interrupt response (80 ns latency, 160 ns for full context switch)
- MCU-like instruction set mnemonics

### **Emulation features**

- Zero-overhead, hardware-based, real-time debug capability
- Real-Time Data Exchange (RTDX™) capability
- Two hardware break points
- Single data watch point
- Benchmarking counter
- Programmable signature analysis
- Available real-time code trace and custom ICE module

## 'C2700 Code Efficiency Improves Performance and Lowers Cost



Single instruction set maximizes code efficiency, netting improved performance and lower cost.

### Uniprocessor technology cuts development time in half

The 'C2700 architecture features two innovations that work together to cut application development in half. A highly efficient C compiler reduces the up-front development time, while the real-time emulation component significantly decreases the time spent in debugging.

#### • Highly efficient C compiler

To provide a more programmer-friendly alternative to assembly language, a complete C language programming environment has

been provided for the 'C2700. This environment utilizes one of the most code-efficient C compilers ever developed, actually limiting code growth to less than 10 percent — far below the 30 percent or more typically encountered in MCUs. The 'C2700 architecture and C compiler were designed in tandem, therefore the compiler takes advantage of the system's efficient code features, like the read-modify-write instruction set.

The C compiler offers several benefits to the designer of firmware and servo control

applications. The efficiency of the compiler supports the desire of many programmers to use C in embedded systems, due to its ease of use, portability and maintenance, and enables even the most time-critical code to be written in a high-level language. Time-consuming assembly programming is virtually eliminated.

#### • Advanced emulation capability

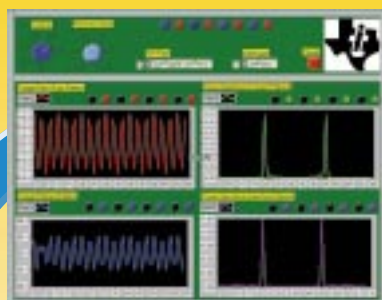
An important innovation for system debug and development is inclusion of TI's new real-time debug technology in the 'C2700 hardware. Used in conjunction with the integrated JTAG-based or parallel visibility ports, this unique technology enables developers to see and modify internal registers and memory while the processor continues to operate at full speed in its normal mode. Furthermore, designers can service real-time interrupts while single-stepping through non-time critical code.

Real-Time Data Exchange (RTDX™) is an advanced DSP analysis technology that provides a real-time visibility port, or window, into device performance. With RTDX, developers can transmit and

'C2700's real-time capabilities add value on many levels.

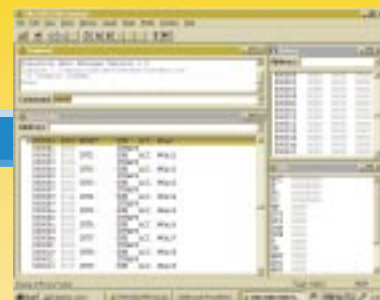
## Revolutionary Real-Time Solutions

### Real-Time Data Exchange (RTDX™)



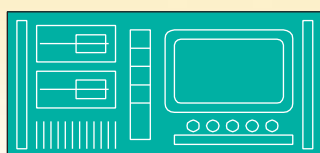
Maximize Performance

### Real-Time Emulation



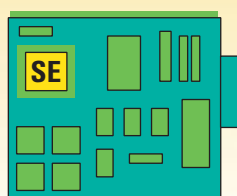
Find Bugs Faster

### Real-Time Test

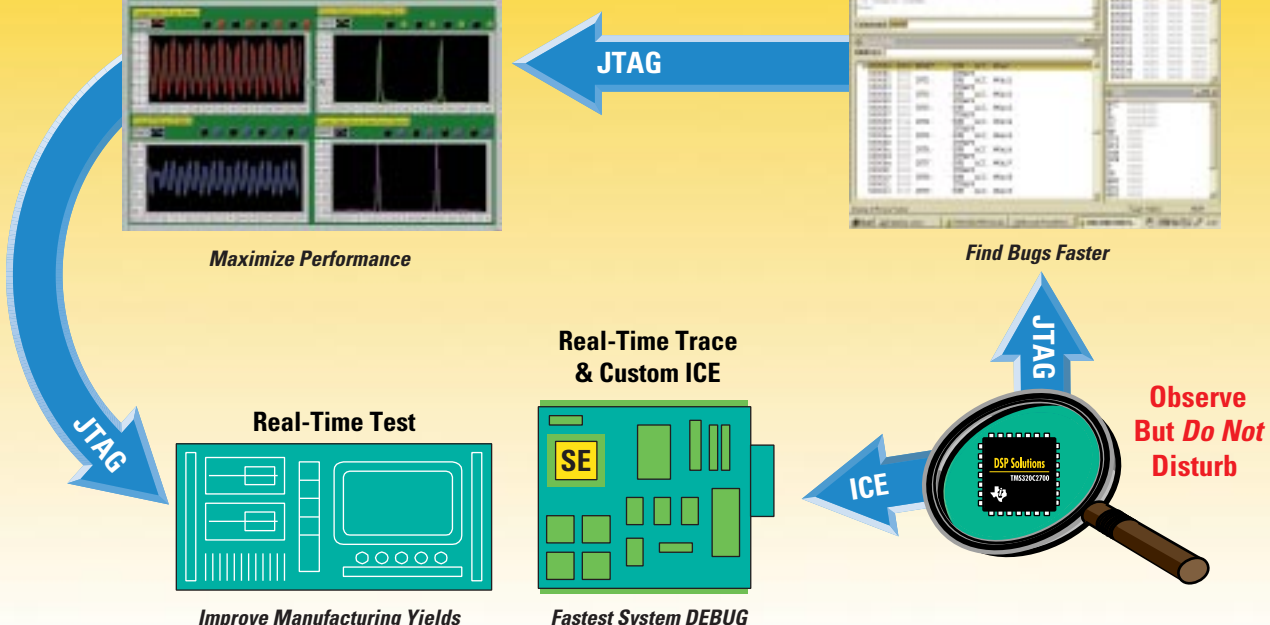


Improve Manufacturing Yields

### Real-Time Trace & Custom ICE



Fastest System DEBUG



receive data between the host and target DSP at speeds of up to 30 Mb/sec. They can monitor, analyze and modify code executing at 100 MHz without impacting results or halting applications.

Through this window, users can display the state of the system graphically or save the data to a file while the processor is running at full speed. With greater visibility into system operations, developers can easily optimize their designs and maximize their system performance in a shorter time.

For example, RTDX can provide the servo designer with a means to plot the servo error signal during seek or track operations and better optimize mechanical performance. Interface designers can use this unique debug capability to monitor and analyze buffer fill rates, or to optimize buffer sizes and performance within their system.

RTDX also offers the ability for manufacturing customers to monitor and test products while on the production line. Production problems or faults can be detected while the system continues to run, enabling the user to realize higher overall manufacturing yields.

In addition to the JTAG-based real-time debug, an available ICE system provides full 100 MHz

trace of all executed code and accessed memory. The system records all core bus activities and executed instructions, along with precise timing information. Break or trigger events can be generated using thousands of address comparators and a sophisticated state machine. The ICE system provides reconfigurable on-chip memory, and can even be used with 'C2700 devices that feature custom ASIC logic.

#### **Design reduces overall system cost**

The 'C2700 architecture reduces system cost through several mechanisms. For systems that typically utilize two processors, such as high-performance HDD or DVD, the integration of DSP and MCU technology on a single chip enables designers to avoid the cost of multiple processors. The code compactness of the architecture reduces memory requirements and a small core size meets the needs of the most cost constrained applications.

The power of the architecture also opens the door for hardware functions to be replaced with software. For example, integrated DSP-based adaptive controls can help the manufacturer eliminate or loosen tolerance on mechanical components.

#### **Code compatibility**

The 'C2700 architecture retains code compatibility with TI's widely used 'C2xLP DSP core, but with significantly higher performance. In this way, designers looking to enhance their mass storage applications preserve their initial investment and realize a true ease of migration to the more powerful 'C2700 series.

#### **Third party support**

TI's Storage Products Group offers versatile in-house tools and hardware/firmware support personnel to aid our 'C2700 customers in the development of customized embedded processor solutions. In addition, the 'C2700 is supported by TI's extensive third party network. This network provides a wide range of software and hardware tools, including debuggers and real-time operating systems from both the DSP and MCU industries.

#### **Additional information**

To obtain additional information on the 'C2700 architecture and core, please contact your local TI Sales Office, or visit the 'C2700 web site at [www.ti.com/storage](http://www.ti.com/storage).

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