TMS320C62x

Device	Internal Cycle Time	Nominal Voltage	On-Chip RAM Prog/Cach	On-Chip RAM Data	Synchronous Memory Interface	Host Port	MeBSP	DMA	Package
TMS320C62x	5 ns	2.5/3.3 V	512K	512K	(1) 32-bit	(1) 16-bit	2	4	352-lead BGA

- 16-bit host port for host-to-access on-chip memory
- Four direct memory access (DMA) channels with bootloading capability for efficient access to external memory/peripherals
- Two multi-channel buffered serial ports (MeBSPs) for simplified interface to telecommunications trunks and efficient interprocessor communication
- Two 32-bit timers that allow easy algorithm implementation
- Ultra-thin 352-lead ball grid array (BGA) package for reduced board-space requirements.

Defining a New Generation of DSP Performance

As the new generation of TI's industry-leading TMS320 DSP family, the 'C62x DSPs will again redefine the possibilities of signal processing system design. An unparalleled combination of hardware and software synergy make the generation the new industry performance leader.

For More Information

Samples of the TMS320C6201 can be ordered today from Texas Instruments and its authorized distributors. If you would like more information on how to put the power of this new generation to work for you and your application, please contact your local TI field sales office today. Or you'll find more information at *http://www.ti.com/sc/c6x* on the World Wide Web.

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THE WORLD LEADER IN DSP SOLUTIONS

Product Bulletin

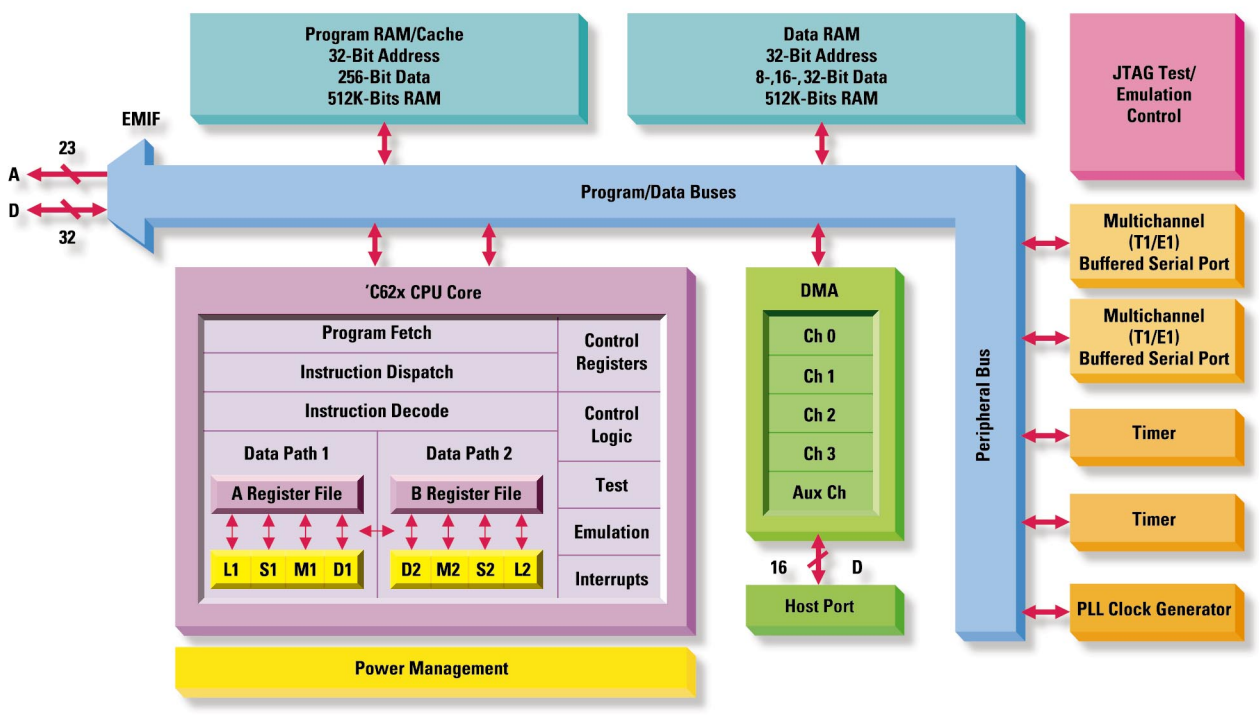
TMS320C62x Digital Signal Processors

In Production Today!

Key Features:

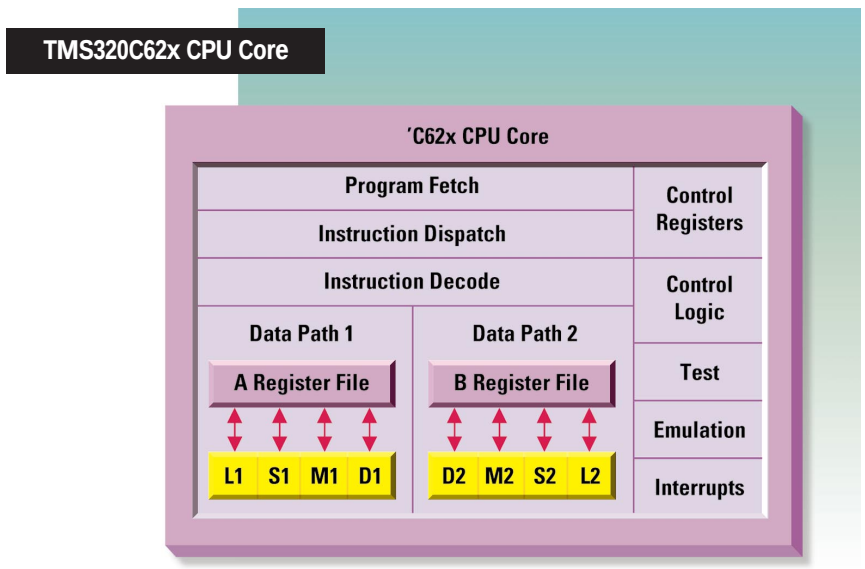
- 1600 MIPS at 200 MHz
- VelociTI™ advanced VLIW DSP architecture
- Four direct memory access (DMA) channels
- Industry's most advanced DSP C compiler
- Assembly Optimizer efficiently schedules tasks for maximum performance and ease in assembly language program
- Eight independent functional units
- Allows up to eight 32-bit instructions to be executed each cycle

TMS320C62x Digital Signal Processor



As the first in a new generation of DSP products from Texas Instruments, the TMS320C6x now gives designers an easy-to-use, cost-effective solution that achieves up to 10 times the performance of any other fixed point DSP on the market. The device represents breakthrough technology that enables new applications and energizes existing ones for multi-channel, multi-function applications. Applications such as pooled modems, wireless base stations, remote access servers (RAS), digital subscriber loop (xDSL) systems, cable modems, intelligent cruise control, personalized home security systems and multi-channel telephony systems. For these complex applications, the 'C62x offers the ability to replace multiple current generation DSPs at up to a 50 percent system cost reduction. As a DSP Solution from TI, OEMs designing with the 'C62x get the assurance of optimized code and compiler efficiency, third-party support tools and system-level experience that simplify the design and development of DSP-based end-equipments.

The TMS320C6201 is the new industry benchmark — the first in the TMS320C62x generation of devices, which utilize a common core based on VelociTI, TI's advanced Very Long Instruction Word (VLIW) DSP architecture. The generation's ultra-high performance is a combination of its unique VelociTI architecture and unsurpassed development environment that offers three times the efficiency of other fixed-point DSP compilers.



The eight functional units of the 'C62x core provide the compiler and Assembly Optimizer with many execution resources.

Breakthrough VelociTI Architecture Means Unparalleled High Performance

Traditionally, the advantages associated with VLIW architectures were often difficult to obtain. A lack of sophisticated code generation tools often meant that programmers were required to spend many hours optimizing their code for performance only to find these optimizations were largely negated by cumbersome and unwieldy code sizes.

The 'C6000 platform eliminates these drawbacks with the highly parallel and independent VelociTI architecture that emphasizes software-based flexibility through the industry's most efficient C compiler and the industry's first Assembly Optimizer. For designers, the direct translation is faster time-to-market with highly integrated and differentiated products.

The 'C62x core's performance is a product of a highly deterministic architecture that enables maximum code performance. The 200 MHz device outperforms the competition with more than 1600 million instructions per second (MIPS) and 400 million multiply-accumulates (MMACs) per second. The advent of such a high-performance DSP significantly lowers costs for manufacturers. As an example, a single TMS320C6201 can implement 30 vocoder channels at $3-per-channel in a wireless base station. Previous generation DSPs could only implement five channels at $7-per-channel. In a typical RAS application, a single 'C6201 can support 10-15 V.34 modems at a cost of about $9 per modem. Current high-end DSP-based systems only achieve one modem per DSP at about $18 per modem.

The eight functional units of the 'C62x core, which include two multipliers and six arithmetic units, are highly orthogonal, providing the compiler and Assembly Optimizer with many execution resources. Eight 32-bit, RISC-like instructions are fetched by the CPU each cycle. VelociTI's instruction packing feature allows these eight instructions to be executed in parallel, serially, or in parallel/serial combinations. This optimized scheme enables significant reductions in code size, program fetches and power consumption.

'C6000 Third-Party Hardware and Software Support

Third Party	Support
Ariel	Computer Telephony, xDSL and OEM DSP
Cheops	Imaging Hardware and Software
D2 Technologies	Embedded Voice Processing (EVP™) Software
DSP Research	'C6x Development Boards
DSP Software Engineering, Inc.	Soft-Modem and Telecom Software
Eonic Systems	Real-Time Operating Systems for DSP
GO DSP	Software Development Tools
HotHaus Technologies, Inc.	Telecommunications Software
Innovative Integration	DSP Coprocessor
Loughborough Sound Images	Computer Telephony and Signal Processing Platforms
MVP Development Group	Highly Optimized 'C6x Software Libraries for Audio Compression and ITU Telecom Standards
Pentek	Communications Boards
ViaDSP	Telephony Gateways
White Mountain DSP, Inc.	Multi-Platform Debug Support
Signals & Software Limited	High-Density ISP Modem
Spectrum Signal Processing	Hardware, Interface Silicon & CTI Software for DSPs
Spectron Microsystems	SPOX Real-Time Operating Systems
Sonitech, Inc.	SPIRIT-6000 Series of High-Performance Board-Level

Other features of the 'C62x core that contribute to its leading performance include byte addressability, a 32-bit address reach, 8-bit overflow protection, saturation, bit counting and normalization. In addition, all instructions are conditional, reducing costly branching and increasing parallelism for higher sustained performance.

Advanced Development Environment—Gets powerful designs to market fast

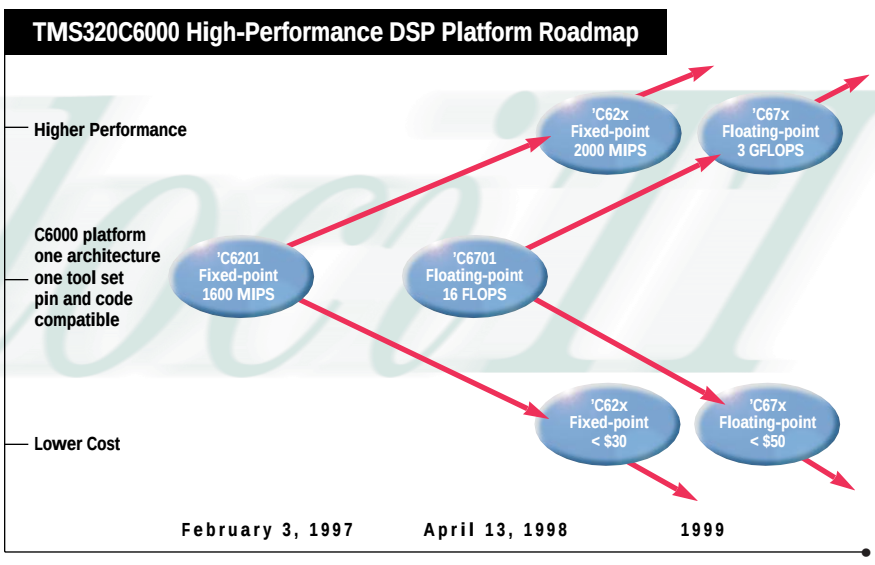
Beyond raw MIPS, the 'C6000 platform's power is designed for easy user accessibility across a broad range of multi-channel applications. Simple yet highly efficient programming contributes largely to this goal, allowing designers to quickly develop applications with only a basic understanding of the device's architecture.

Advanced C compiler

The 'C6000 architecture's dominating performance is captured by its highly efficient C compiler. The compiler gives designers much of the performance of hand-coded assembly language in a fraction of the time normally required for task-intensive code optimization. In conjunction with the advanced VLIW core, the compiler enables optimizing features such as instruction packing, conditional branching, variable width instructions and pre-fetched branching.

Industry's First Assembly Optimizer

Another major breakthrough of the 'C6000 platform is the DSP industry's first Assembly Optimizer. The tool is designed to simplify assembly-language programming of critical loop kernels and help further speed time-to-market. The Assembly Optimizer accepts linear, RISC-like assembly code and schedules it for optimum performance. Features of the 'C6000 Assembly Optimizer include loop optimization, serial-to-parallel assembly, software pipelining, register allocation and resource utilization feedback.



Other 'C6000 Tools

An effective debugger is also critical in reducing time-to-market for new applications. The 'C6000 development environment provides a new intuitive Windows™-based graphical user interface (GUI) for debugging and improved visibility into source code execution characteristics. The GUI debugger also incorporates a dynamic profiler to help users find bottlenecks and improve code efficiency.

TI will introduce a real-time scan-based emulator that allows program analysis without stopping the program. The tool features a JTAG serial interface, software and hardware program breakpoints and performance analysis.

The TMS320C6201

As the first device in the 'C62x generation, the TMS320C6201 adds to the 'C62x core some important features that make it ideal for multi-channel, multi-function applications. It is the first in a line of advanced VLIW, 32-bit 'C62x devices from Texas Instruments, providing more than 10 times the performance of DSPs currently used in these applications. Additional features of the 'C6201 include:

- Large on-chip memory for fast algorithm execution and reduced system part count (512K-bits program/cache and 512K-bits data memory)
- 32-bit external memory interface supports SDRAM, SBSRAM, and numerous types of asynchronas memories for a broad range of external memory requirements and maximum system performance