TMS320c2xx ESSP peripheral update

This document contains the data sheet information and electrical characteristics of the TMS320F206 rev 2.x digital signal processors. **The data is preliminary and subject to change at any time**.

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A.1 TMS320C2xx Enhanced Synchronous Serial Port (ESSP) Features

- Full-Duplex, double-buffered Synchronous Serial Port

- Highly Flexible Operation:
  - Burst and Continuous modes
  - Supports 8- and 16-bit word lengths
  - Multi-channel mode with glueless interface to as many as four voice-band or telephony codecs for telecommunications applications such as line cards.
  - Serial Peripheral Interface (SPI) mode

- Independent four-level deep FIFO for both the receive and transmit sections
  - Programmable FIFO level interrupts to reduce software overhead
  - FIFO level status bits

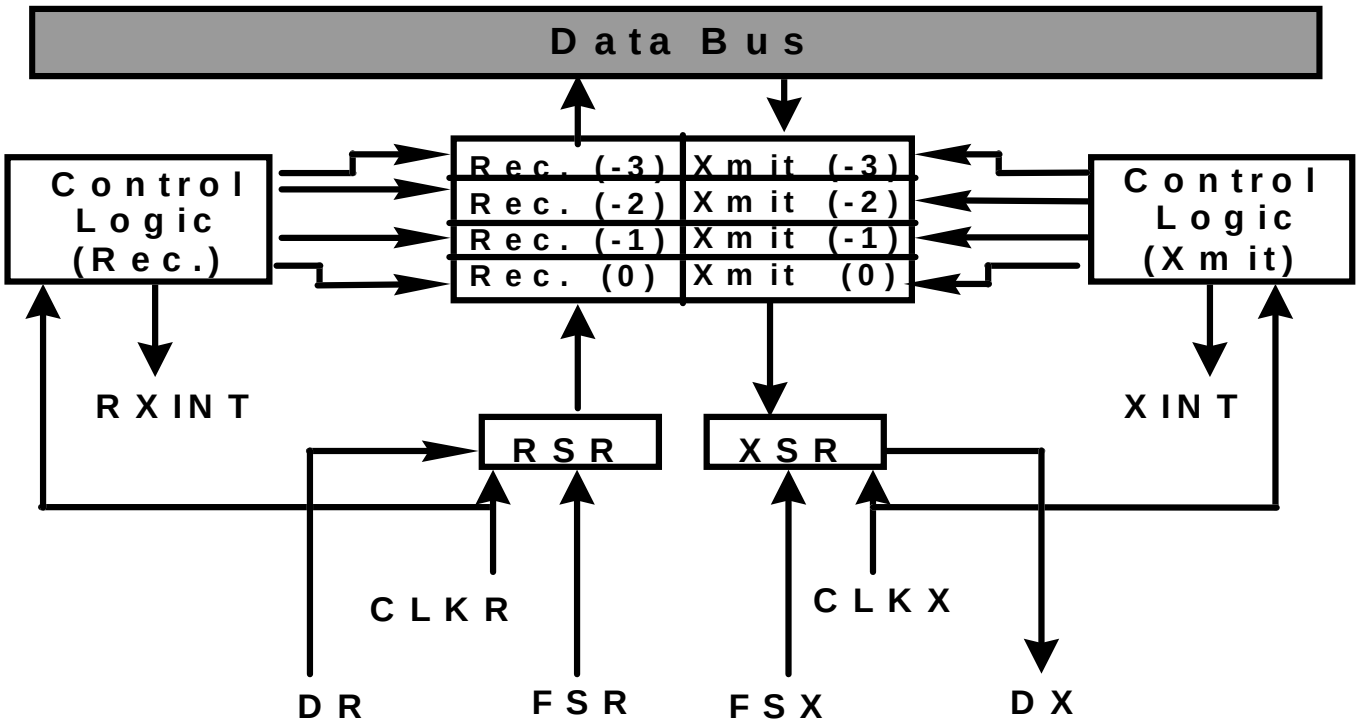
- Various clocking options to ease interfacing in many applications
  - Internal shift clock, CLKX, derived from an independent 8-bit pre-scalar
  - Internal frame sync, FSX, derived from an independent 8-bit pre-scalar
  - Polarity control on shift clock, CLKX, and frame sync pulse, FSX

- High impedance control on data transmit pin DX for TDM applications
- Pre-scalars are configurable as a general-purpose 16-bit counter.
- Fast Transfer Rate:
  - 20 Mbits/s at 25ns cycle time

A.2 Enhanced Synchronous Serial Port (ESSP)

A full duplex, (bi-directional) 8/16 bit, synchronous serial port provides direct communication with serial devices such as codecs, serial A/D (analog to digital) converters, and other serial systems. The interface signals are compatible with codecs and many other serial devices. The serial port may also be used for intercommunication between processors in multiprocessing applications.

Figure 1 Enhanced Synchronous Serial Port Block Diagram



Both receive and transmit operations have a four-deep First In First Out (FIFO) buffer. The advantage of having a FIFO is to alleviate the CPU from being loaded with the task of servicing a transmit or receive data packet on every interrupt, thus allowing a continuous communications stream of 8/16–bit data packets. The continuous mode provides operation, that once initiated, requires no further frame synchronization pulses when transmitting at maximum packet frequency. The maximum transmission rate for both transmit and receive operations will be the CPU clock divided by two, CLKOUT1(frequency)/2. Therefore, the maximum rate at 50ns is 10Mbit/s,14.28Mbit/s at 35ns, and 20Mbit/s at 25ns. The serial port is fully static and thus will function at arbitrarily low clocking frequencies.

Three signals are necessary to connect the transmit pins of the transmitting device with the receive pins of the receiving device for data transmission. The transmitted serial data signal (DX) sends the actual data. The transmit frame synchronization signal (FSX) initiates the transfer (at the beginning of the packet), and the transmit clock signal (CLKX) clocks the bit transfer. The corresponding pins on the receive device are DR, FSR and CLKR, respectively.

A.3 Serial Port pins

The Enhanced Synchronous Serial Port has six dedicated pins for external interface. Table 2 explains the functions of these pins.

Table 1 TMS320C2XX Interface signals

100 PIN	'C2xx PIN NAME	I/O/Z	DESCRIPTION
			Serial Port Signals
87	CLKX	I/O	Transmit clock. Clock signal for clocking data from the DX (data receive register) to the DX pin (data transmit pin). The CLKX can be an input if the MCM bit in the SSPCR is set to 0. It can also be generated internally. Internal CLKX rate is defined by the input clock to the pre-scalar and by the equation CLKX rate = CLKOUT1 /((2*(CLXCT+1)). The internal CLKX can also feed a frame sync pre-scalar to generate internal frame sync synchronous to CLKX and at variable rates. The Pre-scalars for CLXK and FSX are defined in the I/O register SSPCT at IS@FFF3h
84	CLKR	I	Receive clock input. External clock signal for clocking data from the DR (data receive) pin into the RSR (serial port shift register). Must be present during serial port transfers. If the serial port is not being used, this pin can be sampled as an input via the IN0 bit of the SSPCR.
85	FSR	I	Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data receive process.
86	DR	I	Serial data receive input. Serial data is received into the receive shift register RSR from DR pin.
89	FSX	I/O	Frame synchronization pulse for transmit input/output. The falling edge of the FSX pulse initiates the data transmit process beginning the clocking of the XSR. Following reset, FSX is an input. This pin may be selected by software to be an output when the TXM bit in the serial control register, SSPCR, is set to 1. The Frame sync can be generated internally. The Frame sync rate can be either defined by the pre-scalar FSXCT or by the rate at which data is written into the transmit FIFO. The internal CLKX can also feed a frame sync pre-scalar to generate internal frame sync synchronous to CLKX and at variable rates. Internal FSX rate is defined by the input clock to the pre-scalar and by the equation FSX rate = CLKX pin clock /((2*(FSXCT+1)). The Pre-scalars for CLXK and FSX are defined in the I/O register SSPCT at IS@FFF3h. .
90	DX	O	Serial port transmit output. Serial data is transmitted from transmit shift register XSR through DX pin. DX is placed in high impedance when not transmitting.

A.4 Control and status registers

The Enhanced Synchronous Serial Port operates through the five I/O mapped registers (SDTR, SSPCR, SSPST, SSPMC, SSPCT) and two internal registers (XSR and RSR) that are not accessible. These registers are listed in Table 2.

Table 2 Serial Port Registers

Registers	ADDRESS	Value at Reset	Description
SSP registers			**I/O mapped registers**
SDTR	IS@FFF0	xxxxh	Data transmit/receive FIFO register
SSPCR	IS@FFF1	0030h	Synchronous Serial port control register
ESSP registers			
SSPST	IS@FFF2	0000h	Status register
SSPMC	IS@FFF3	0000h	Multi-channel register
SSPCT -CLXCT	IS@FFFB	xx00h	Shift clock pre-scalar (CLKX) low byte
SSPCT -FSXCT	IS@FFFB	00xxh	Frame sync pre-scalar (FSX) high byte
			Internal registers
XSR			Transmit shift register
RSR			Receive shift register

x - Indicates undefined or value based on the pin levels at reset.

A.5 SSPCR register

The synchronous serial port register (SSPCR), controls various modes and clock sources necessary to interface the serial port to external devices. The SSPCR register bit definitions are listed in Table 4.

Figure 2 Serial Port Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREE	SOFT	TCOMP	RFNE	FT1	FT0	FR1	FR0	OVF	IN0	XRST	RRST	TXM	MCM	FSM	DLB
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 3 Serial Port Control Register Bits Summary

Bit	Name	Function
0	DLB	The Digital Loopback Mode Bit can be used to put the serial port in digital loopback mode. When DLB=1, DR and FSR are connected to DX and FSX, respectively, through multiplexers. Additionally, if CLKR is driven by CLKX if MCM=1. If DLB=1 and MCM=0, CLKR is taken from the CLKR pin of the device. This configuration allows CLKX and CLKR to be tied together externally and supplied by a common external clock source. If DLB=0, DR, FSR, and CLKR are taken from the respective device pins. Note, that TXM must be set to one for proper operation in DLB mode. Note also that the FSX and DX signals appear on the device pins when DLB=1, but FSR and DR do not.
1	FSM	The Frame Synch Mode Bit specifies whether frame synchronization pulses are required for serial port operation. If FSM=1, a frame sync pulse is required on FSX/FSR for the transmission/reception of each word. When the serial port is operated in the continuous mode, FSM=0.
2	MCM	The Clock Mode Bit specifies the clock source for CLKX. If MCM=0, CLKX is taken from the

		pin. If MCM=1, CLKX is driven by an on–chip clock source having a frequency equal to one–half of CLKOUT1. Note, that if MCM = 1 and DLB = 1, a CLKR signal is also supplied by the internal source.
3	TXM	The Transmit Mode Bit configures the FSX pin as an input (TXM = 0) or as an output (TXM = 1). When TXM = 1, frame sync pulses are generated internally when data is transferred from the fifo to XSR to initiate data transfers. The internally generated framing signal is synchronous with respect to CLKX. When TXM = 0, the transmitter idles until a frame synch pulse is supplied on the FSX pin.
4 5	RRST XRST	The Transmit Reset and Receive Reset signals reset the transmitter and receiver, respectively. If the SSPCR is to be modified to reconfigure the serial port, a total of two writes should be made to the SSPCR. The first write should write zeroes to XRST and RRST and the desired configuration to bits 0-4. The second write should write ones to XRST and RRST, taking the serial port out of reset.
6	IN0	The Input 0 bit allows the CLKR to be used as a bit input. IN0 reflects the current level of the CLKR pin of the device. The level on this pin can be read by reading the SSPCR register. This bit can be tested by using the BIT or BITT instructions. Note that there is a latency of between 0.5 and 1.5 CLKOUT1 cycles in length from CLKR switching to the new CLKR value being represented in the SSPCR.
7	OVF	Overflow flag (OVF) status signal that indicates when the receiver has finished due to FIFO overflow (continuous mode). The OVF bit is set when the receive FIFO overflows and is cleared when the receive FIFO is read.
8 9	FR0 FR1	FR1 FR0 0 0 Receive FIFO is not empty. 0 1 Receive FIFO has 2 or more words 1 0 Receive FIFO has 3 or 4 words 1 1 Receive FIFO is full.
10 11	FT0 FT1	FT1 FT0 0 0 Transmit FIFO has 1 or more words available. 0 1 Transmit FIFO has 2 or more words available. 1 0 Transmit FIFO has 3 or 4 words available. 1 1 Transmit FIFO is empty. 4 data spaces available.
12	RFNE	Receive FIFO not empty. Data still exists in receive FIFO.
13	TCOMP	Transmit complete. All data has successfully be transferred out of the transmit FIFO.
14	SOFT	The SOFT bit. This bit is enabled when the FREE bit is 0. If FREE = 0, the SOFT bit selects immediate stop if 0, stop after word completion if 1. At reset, this bit is zero.
15	FREE	The FREE bit. If FREE = 1, free run is selected, regardless of the value of the SOFT bit. If FREE = 0, the SOFT bit selects the emulation mode. At reset, this bit is zero.

A.5.1 Selecting CLKX and FSX source

The SSPCR register bits MCM (bit2) and TXM (bit3) define the source for the shift clock CLKX and frame sync FSX. These two clock sources are based on the type of external device that need to be interfaced with the serial port. Table 5 explains the clock sources selection using the SSPCR register bits.

Table 4 Selecting Shift Clock CLKX and Frame sync FSX sources

MCM	TXM	CLKX source	FSX source
0	0	External	External
0	1	External	Internal
1	0	Internal	External
1	1	Internal	Internal

A.6 New ESSP registers

A.6.1. SSPST register

The SSPST register is an additional register used by the serial port to enable and disable ESSP features. It has additional FIFO status bits. Refer to Table 6 for more details.

Figure 3 Serial Port status Register -SSPST IS@FFF2h

15	14	13	12	11	10	9	8	7 6 5	4 3 2	1	0
DRP pin	FSN	FSXOX	FSXST status	RSVD	CLN	CLXOX	PRSEN	Transmit FIFO status	Receive FIFO status	SGNEX Sign-extend	BYTE 8/16 bit
R	R/W	R/W	W1C/R		R/W	R/W	R/W	R	R	R/W	R/W

1. Data word size - Bit 0 of this register defines the data word length as 16-bit or 8-bit. The default value at reset is 0, selecting 16-bit data word size. Any 8-bit data can be received or transmitted by setting bit 0 to 1.

2. Sign-extend - Bit 1. In 8-bit data word this bit when set to 1, sign extends the MSB bits of the 16-bit word. If the bit is reset to 0, the MSB bits will be filled with zeros.

3. Status of the receive and transmit FIFOs
   - Bit 2,3,4 and 5,6,7 define the status of the receive and transmit FIFOs. These are 3-bit registers, giving five valid combination indicating the contents of the FIFOs.

4. Pre-scale clock enable PRSEN.
   - Bit 8 when set to 1, will enable the input clock source to the CLKX pre-scalar CLXCT and extend the scaled CLKX to the SSP. If reset to 0 the pre-scalar will not count down as there is no input clock to the counter.

5. Input clock source CLXOX bit.
   - In the general purpose counter mode(GPC bit =1), bit 9 selects the input clock source to the 16 bit counter (SSPCT). If CLXOX bit is 0 the input clock will be CLKX pin clock (either CLKOUT1/2 or external CLKX depending on the MCM bit). If CLKXOX bit is 1 the input clock will be CLKOUT1. In all other modes this bit has no effect (don't care x).

6. Shift clock CLKX invert bit, CLN
   - Bit 10 selects the polarity for the shift clock CLKX. If reset to 0 the CLKX will be in normal mode. If set to 1 the CLKX will be inverted for internal and external CLKX. CLN bit controls both the CLKX and CLKR polarity. In the internal CLKX mode the out going CLKX will be inverted once and the incoming CLKR signal will be inverted once. Thus, if CLKX and CLKR pins are external connected, the polarity of the CLKX/CLKR are the same with respect to the SSP core.

7. Reserved - Bit 11.

8. Pre-scalar FSXST status bit.
   - Bit 12 is the FSXST bit that will be set to 1 every time the FSXCT pre-scalar counter reaches 0x0000. This bit can be read and cleared by writing a 1 to the bit 12. This bit is also a counter status bit in 16 bit counter mode. It will be set to 1 whenever the 16-bit counter reaches 0x0000. This bit will not initiate an interrupt if GPI is enabled in SSPMC register.

9. Internal FSX selection bit, FSXOX
   - Bit 13 selects the type of internal frame sync that will be issued from FSX pin. If set to 1 the FSX is from the pre-scalar FSXCT. If reset to 0 the internal FSX will be at the rate with which data is written into the transmit FIFO.

10. Frame sync invert bit, FSN
    - Bit 14 selects the polarity for the frame sync. At reset it will be reset to 0 and selects FSX to be high for one CLKX duration. The data transmit and receive is based on the falling edge of FSX. If FSN is set to 1, the polarity of the FSX is inverted. The FSX will remain high during data transmit or receive (8/16 CLKX cycles). FSN bit controls both the FSX and FSR polarity. In the internal FSX mode, the out going FSX will be inverted once and the incoming FSR will be inverted once. Thus, if FSX and FSR pins are external connected, the polarity of the FSX/FSR are the same with respect to the SSP core.

11. DR pin read bit - Bit 15 is DRP bit which gives visibility to DR pin. Its a read only bit.

A.6.2 SSPMC register

The SSPMC is a register at FFF3 in the I/O space to select multi-channel and 16-bit counter features in the Enhanced Synchronous Serial Port. Figure 4 explains the bit fields used to control multi-channel option on the ESSP.

15	Bit 14-7	6	5	4	3	2	1	0
SSPRST	Reserved	SPI	CH1	CH0	MMODE	GPI	CHLT	GPC
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 4 Serial Port Multi-channel Register - SSPMC IS@FFF3h

1. General purpose counter bit, GPC.

- Bit 0 configures the two pre-scalars CLXCT, FSXCT as a 16-bit counter. When GPC is 1 both CLXCT and FSXCT are used for 16-bit counter . The input to the counter is either internal CLKOUT1 or CLKX pin clock, defined by CLXOX, bit 9 in SSPST register. In the counter mode the pre-scalars are not available for SSP clock scaling. GPC bit should be 0 if the pre-scalars are to be used for CLKX and FSX scaling.

2. 16 bit Counter halt bit CHLT.

- Bit 1 can be used to stop the 16-bit counter, when the pre-scalars are used as counter. 0 is default, indicates counter is counting, 1 will stop the counter.

3. General purpose counter interrupt bit, GPI

- Bit 2 configures the XINT interrupt of the SSP as 16-bit counter interrupt. When ever the 16-bit counter reaches 0, an interrupt will be generated.

4. Multi-channel mode bit MMODE

- Bit 3 if reset to 0, deselects multi-channel option on the serial port. Default Bit 3 if set to 1 selects multi-channel mode and uses the pre-scaled frame sync FSX only. In this mode more than one frame sync pulses are generated on different pins for glueless interface to multiple codecs. The FSX and CLKX signals are internally connected to FSR and CLKR pins respectively. CLKR and FSR pins are available as outputs for generating multi- channel frame sync FSX2, FSX3. The fourth channel frame sync FSX4 is generated on IO0 pin (pin96). In this mode IO0 is not available as general purpose I/O pin.

5. Channel select bits, CH1, CH0

- Bits 5 4 select the number of channels that are available in the multi-channel mode. These bits have no effect if MMODE bit is 0.

0 0 Selects one channel with one frame sync pulse FSX1 on FSX pin. The FSX rate is defined only by the FSX pre-scalar, FSXCT.

0 1 Selects second channel with the second frame sync pulse FSX2 on CLKR pin (pin 84). Frame sync FSX2 will be issued on the 2 CLKX cycle from the LSB bit of the first channel.

1 0 Selects third channel with the third frame sync pulse FSX3 on FSR pin (pin 85). Frame sync FSX3 will be issued on the 2 CLKX cycle from the LSB bit of the second channel.

1 1 Selects fourth channel with the fourth frame sync pulse FSX4 on IO0 pin (pin 96). Frame sync FSX4 will be issued on the 2 CLKX cycle from the LSB bit of the third channel. In this mode IO0 pin is not available for IO operation.

6. SPI mode bit, - Bit 6 selects a 8/16 bit serial peripheral interface SPI mode. This mode is available only in Burst mode with internal shift clock CLKX. If bit 6 is reset to 0, the SPI mode is disabled. If bit 6 is set to 1 then SPI mode is selected with internal CLKX. In this mode CLKX is issued only during the time data bits are transmitted or received. Data will be transmitted/received when ever transmit FIFO has data, along with an FSX signal. Pre-scaled FSX cannot be used in this mode. For receiving data synchronous to CLKX, connect CLKX to CLKR and FSX to FSR. CLKR and FSR are internally connected to CLKX and FSX respectively. CLKX pin will be low normally in SPI mode. If CLN bit is enabled in SSPST register, then CLKX pin will be high in between data transmit.

7. Reserved bits - Bits 14-7

8. SPRST - Bit 15 resets the current operation of SSP. At reset this bit will be zero enabling normal operation. If set to 1, the SSP will reset as below,
   a. Reset transmit FIFO pointers and transmit shift register.
   b. Reset receive FIFO pointers and receive shift register
   c. Pre-scalar logic will reload pre-scalar counters if GPC=0,
      if GPC=1, no reload to pre-scalars. Reset all logic, except counter logic.
   d. All control register bits (SSPCR) are not affected by this. However, all status bits will be reset.

Table 5 On_chip Enhanced Synchronous Serial Port status and pre-scale registers.

NAME	ADDRESS	Value at Reset	DESCRIPTION
SSPST	IS@FFF2	0000h	Enhanced Synchronous Serial Port FIFO status bit and word select register Bit0 - 0 - 16 bit data word - default 1 - 8 bit data word Bit 1 - 0 - zero fill unused MSBs in 8-bit word mode 1 - Sign-extend unused MSBs in 8-bit word mode Bit 4 3 2 - Receive FIFO status 0 0 0 - FIFO empty 0 0 1 - FIFO has 1 word 0 1 0 - FIFO has 2 words 0 1 1 - FIFO has 3 words 1 0 0 - FIFO has 4 words Bit 7 6 5 - Transmit FIFO status 0 0 0 - FIFO empty 0 0 1 - FIFO has 1 word to transmit 0 1 0 - FIFO has 2 words to transmit 0 1 1 - FIFO has 3 words to transmit 1 0 0 - FIFO has 4 words to transmit Bit 8 - 0 - PRSEN disables input clock to pre-scalars in SSPCT 1 - PRSEN enables input clock to pre-scalars in SSPCT. Bit 9 - 0 - CLXOX selects CLKOUT1 clock as input to 16 bit counter 1 - CLXOX selects CLKX pin clock as input to 16 bit counter Useful only in 16-bit counter mode. In all other modes, don't care. Bit 10 - 0 - CLN does not affect the shift clock CLKX, default 1 - CLN inverts the shift clock CLKX and CLKR. Bit 11 - Reserved Bit 12 - 0 - Pre-scalar still counting, FSXST bit is zero 1 - FSXST bit is set if pre-scalar value is 0x0000h Bit 13 - 0 - Selects the internal FSX at the transmit FIFO write rate 1 - Selects the internal FSX from FSX pre-scalar FSXCT Bit 14 - 0 - No change on the polarity of FSX pulse - high pulse for one CLKX 1 - FSN will invert the polarity of FSX pulse -low pulse. - Setting FSN to 1 affects FSR polarity. FSR will also be inverted. Bit 15 - Reads the DR pin

SSPMC	IS@FFF3	0000h	Enhanced synchronous serial port multi-channel register Bit 0 - 0 - Pre-scalars used for CLKX and FSX 1 - GPC sets the two pre-scalars in 16-bit general purpose counter mode Bit 1 - 0 - 16-bit Counter running 1 - Stop 16-bit counter Bit 2 - 0 - XINIT interrupt tied to SSP transmit interrupt 1 - GPI selects XINIT interrupt to 16-bit general purpose counter interrupt Bit 3 0 - Default value of MMODE bit. Multi-channel feature not selected 1 - Selects multi-channel feature for the SSP Bit 5 4 - CH1 - CH0 0 0 - Selects one channel by issuing one Frame sync FSX1 from FSX pin 0 1 - Selects two channel by issuing second Frame sync FSX2 from CLKR pin. Second FSX2 will trail FSX1, by two clock CLKX cycles from the LSB bit of the first channel. 1 0 - Selects three channel by issuing third Frame sync FSX3 from FXR pin. Third FSX3 will trail FSX2, by two clock CLKX cycles from the LSB bit of the second channel. 1 1 - Selects four channel by issuing fourth Frame sync FSX4 from IO0 pin. Fourth FSX4 will trail FSX3, by two clock CLKX cycles from the LSB bit of the third channel Bit 6 0 - Deselects 8/16 bit SPI mode. Default - Selects 8/16 bit SPI mode, with internal shift clock CLKX only Bits 7-14 - Reserved. Bit 15 - SSPRST bit to stop current operation of SSP.
SSPCT	IS@FFFB	0000h	Enhanced synchronous serial port counter register Internal Shift clock CLKX counter CLXCT (bits 7-0). 8-bit Pre-scalar used to generate internal shift clock (CLKX). The CLKX rate is defined by the equation CLKX = CLKOUT1/(2*(CLXCT+1)). Internal Frame sync FSX counter FSXCT (bits 15-8). 8-bit Pre-scalar used to generate internal frame sync (FSX). The FSXX rate is defined by the equation FSX =Pre-scalar input clock/(2*(FSXCT+1)). FSX pre-scalar input could be either external CLKX pin clock or pre-scaled internal CLKX.

A.6.3 SSPCT register

The shift clock CLKX and frame sync FSX can come from external or internal sources. The SSPCR register bits define the source of these clock sources. The SSPCT register holds two 8-bit pre-scale counters to provide user specific shift clock CLKX and frame sync clock FSX. The CLXCT counter is an 8-bit pre-scalar to divide CLKOUT1. The pre-scalar output clock is defined by the equation, CLKOUT1((2*(CLXCT+1)) . CLXCT is the pre-scale value defined in the SSPCT register bits 7-0. At reset the CLXCT register value is zero, which defines the CLKX rate to be at (CLKOUT1)/2. This register can be written with any desired 8-bit pre-scale value. The pre-scalar functions as a down counter, and the counter value can be read anytime. The input clock source to the pre-scalar can be CLKOUT1 only. PRSEN,bit 8 of the SSPST register should be set to 1 and enables input clock to the pre-scalar.

Once 8-bit pre-scalar values are written to the register SSPCT, PRSEN has to be enabled to start the counter counting down. The pre-scalar values are loaded into the counter from the internal buffers only after PRSEN is enabled. Enabling PRSEN should always follow any pre-scalar update. The pre-scalar has an internal buffer register which gets updated every time SSPCT is written. The counter after reaching 0x0000, reloads the pre-scale value from the buffer and counts down. This sequence of reload and count down will repeat until, PRSEN bit in SSPST is reset to 0. If the PRSEN is reset to 0, the pre-scalar will not have any input clock source to count down.

The 8-bit pre-scalar FSXCT for FSX also functions similar to the CLKX pre-scalar CLXCT. The frame sync FSX pre-scalar FSXCT takes the CLKX pre-scalar output or external CLKX pin clock as input. This helps to generate a variable frame sync pulse synchronous to CLKX. Most applications require a FSX rate, that is a multiple of the CLKX rate. The FSX rate is defined by the equation, CLKX pin clock/((2*(FSXCT+1)). FSXST bit (Bit 12 in SSPST) will be set every time FSXCT reaches 0x0000, and can be reset by writing a 1 to the FSXST bit.

Figure 5 Serial Port Count Register -SSPCT IS@FFFB

15 - 8	7- 0
8-bit pre-scalar -FSXCT	8-bit pre-scalar -CLXCT
R/W	R/W

A.7 Programmable internal CLKX and FSX rates

The device clock CLKOUT1, external shift clock CLKX and the 8-bit pre-scalars can provide various CLKX/FSX clock rates, to match several serial interface devices. Some such interface devices, like the CODECS operate in slave mode expecting external shift clock. Table 8 below provides various shift clock rates and frame sync that can be generated for voice band applications, using the pre-scalars.

Table 6 CLKX and FSX rates using pre-scalar values

CLKOUT1	Pre-scale value CLXCT Decimal - Hex	CLKX rate	Pre-scale value FSXCT Decimal -Hex	FSX rate	Remarks
40.96Mhz	0	20.48Mhz	255 - FFh	40 Khz	
	9 - 9h	2.048Mhz	127- 7Fh	8 Khz	VBAP/Combo codec rates
	159 - 9Fh	64Khz	3 - 03h	8 Khz	
20.48Mhz	0	10.24Mhz	255 - FFh	20 Khz	
	4 - 4h	2.048Mhz	127- 7Fh	8 Khz	VBAP/Combo codec rates
	159 - 9Fh	64Khz			
12.288x2 = 24.576Mhz	0	12.288			
	1h	6.144Mhz			
	5h	2.048Mhz	127- 7Fh	8 Khz	VBAP/Combo codec rates
	7h	1.536Mhz	95 - 5Fh	8 Khz	VBAP/Combo codec rates
	191 - BFh	64Khz	3 - 03h	8 Khz	

A.8 Pre-scalars as general purpose counter

The two 8-bit pre-scalars in SSPCT register can be used as a single 16-bit down counter. The GPC bit in SSPMC register enables the 16-bit counter mode. While GPC is set to 1 the pre-scalars are not available for scaling CLKX and FSX. The 16 bit counter can accept either CLKOUT1 clock or CLKX pin clock as its input. The counter value can be read any time and can be stopped be setting CHLT bit in the SSPMC register. The counter will flag a status bit FSXST when ever it reaches 0x0000. The counter will reload the counter value after it reaches 0x0000 and will continue to count down. This FSXST bit is cleared by writing a one to the bit.

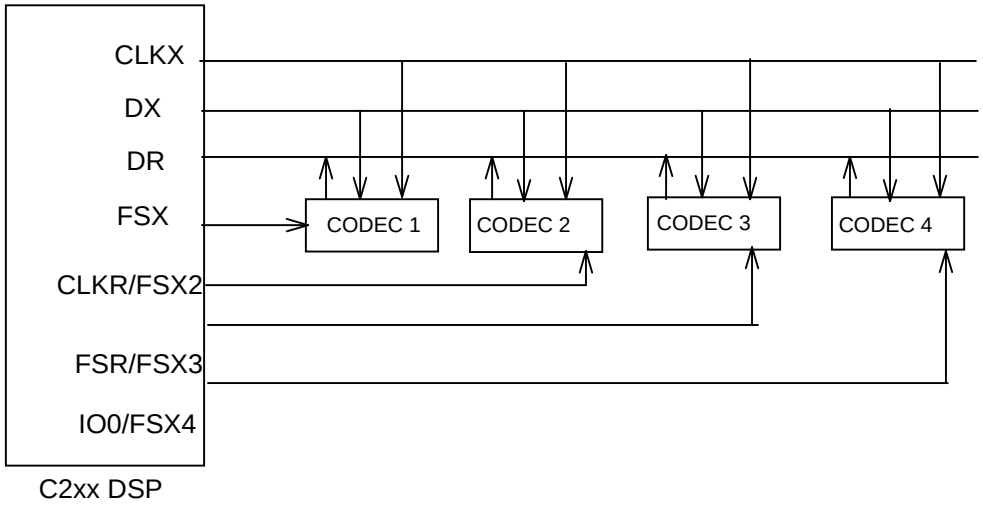
A.9 ESSP register programming considerations

The SSP features are enabled by SSPCR register only. The ESSP registers need not be changed for the standard SSP features. This provides compatibility to the existing codes on rev1.0 silicon. To enable any of the ESSP features the ESSP registers SSPCT, SSPMC and SSPST should to be initialized. Its recommended to initialize the registers SSPCT, SSPMC first followed by SSPST register. The pre-scalars are enabled only after the PRSEN bit (bit 8 in SSPST) is set to 1. So it is essential that the other registers are pre-loaded before enabling the PRSEN bit in SSPST register.

While changing CLKN or FSN bits initialize the SSPST register in two steps. First load the SSPST registers bits with PRSEN bit 0. Provide at least one CLKX cycle delay before setting PRSEN bit to. This should help all internal synchronization of the clocks (FSX/CLKX). This would also make the pre-scalars and the clock circuit to respond the stable clock (FSX/CLKX,FSR,CLKR)edges. However, in any initialization sequence the pre-scalar clocks will be stable after the first reload of the pre-scalar counters.

A.10 Multi-channel frames

Figure 6 Four channel codec interface



A.10.1 8-bit Four channel interface timings

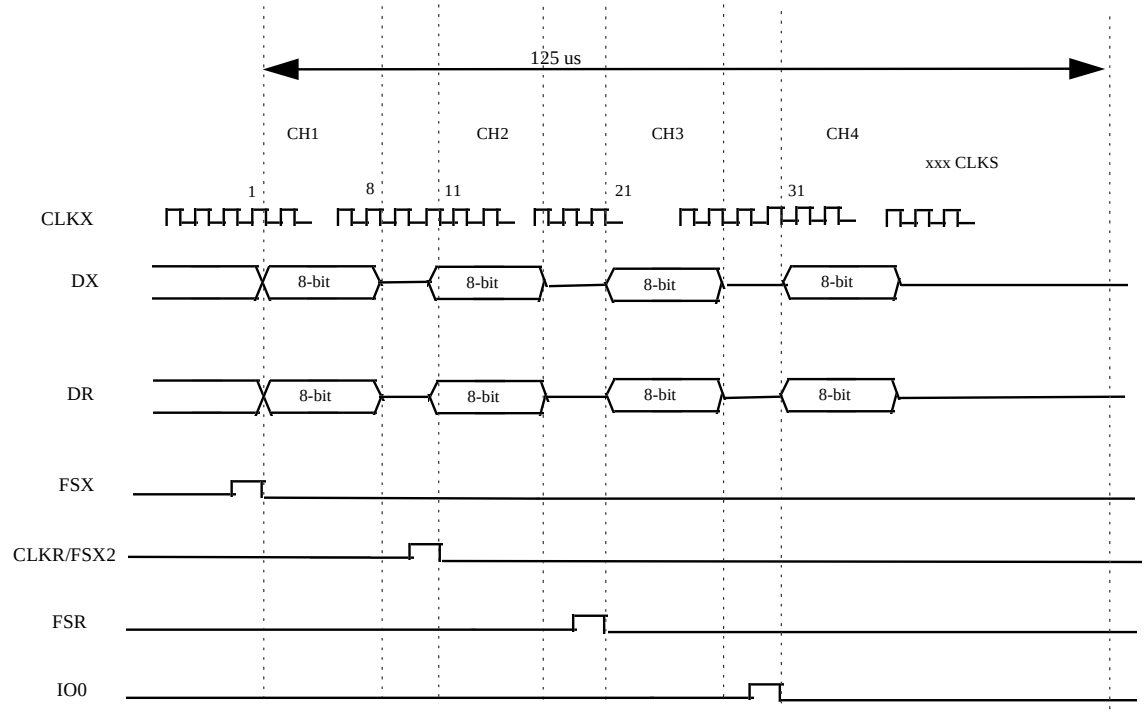


Figure 7 Four 8-bit codec interface timing

A.10.2 16-bit Four channel interface timings

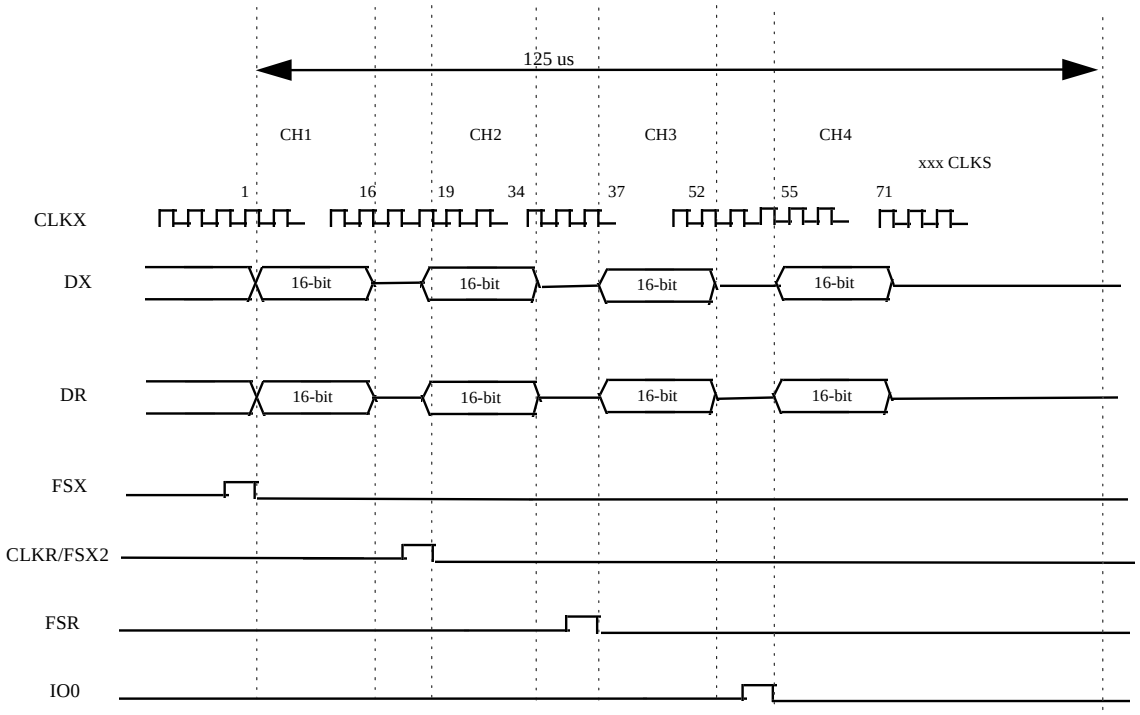


Figure 8 Four 16-bit Codec interface timings

A.11 Serial port configuration table A & B

Table 7 ESSP configuration - Table A - Burst Mode

		SSPCR			SSPMC register								SSPST register											
Option	Function	FSM	MCM	TXM	SSPRST	SPI	CHB1	CHB0	MMODE	GPI	CHLT	GPC	FSN	FSXOX	FSXST	CKN	CLXOX	PRSEN	BYTE	CLKX	FSX	CLXCT	CLKX rate	FSXCT	FSX rate
1	RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	External	External	not used	-	not used	-
2	SSP Option	1	0	0	0	0	X	X	0	0	X	0	0	0	0	0	0	0	0/1	External	External	not used	External CLKX	not used	External
3	SSP Option with FSXCT	1	0	1	0	0	X	X	0	0	X	0	0	1/0	0	0	X	1	0/1	External	Internal	not used	External CLKX	Used for internal FSX	Internal FSX. Defined by FSXCT
4	SSP Option	1	0	1	0	0	X	X	0	0	X	0	0	0	0	0	X	X	0/1	External	Internal	not used	External CLKX	not used	TX FIFO write rate
5	SSP Option	1	1	0	0	0	X	X	0	0	X	0	0	0	0	0	X	0	0/1	Internal	External	not used	½ CLKOUT1	not used	External FSX
6	SSP Option with CLXCT	1	1	0	0	0	X	X	0	0	X	0	0	0	0	0	X	1	0/1	Internal	External	used for CLKX	½ CLKOUT1 or Pre-scaled	not used	External FSX
7	SSP Option with 8-bit Prescalars	1	1	1	0	0	X	X	0	0	X	0	0	1	0	0	X	1	0/1	Internal	Internal	used for CLKX	½ CLKOUT1 or Pre-scaled	used	Defined by FSX Pre-scale
8	SSP Option	1	1	1	0	0	X	X	0	0	X	0	0	0	0	0	X	0	0/1	Internal	Internal	not used	½ CLKOUT1	not used	Defined by write to TX FIF0
9	SSP Option with CLXCT	1	1	1	0	0	X	X	0	0	X	0	0	0	0	0	X	1	0/1	Internal	Internal	used for CLKX	½ CLKOUT1 or Pre-scaled	not used	Defined by write to TX FIF0
10	Multi-channel	1	1	1	0	0	0/1	0/1	1	0	0	0	0	X	0	0	X	1	0/1	Internal	Internal	used	½ CLKOUT1 or Pre-scaled	used	FSX1 is defined by FSXCT
11	Multi-channel	1	0	1	0	0	0/1	0/1	1	0	0	0	0	X	0	0	X	1	0/1	External	Internal	used	½ CLKOUT1 or Pre-scaled	used	FSX1 is defined by FSXCT
12	SPI	1	1	1	0	1	0	0	0	0	0	0	0	X	0	0	X	1	0/1	Internal	Internal	used	½ CLKOUT1 or Pre-scaled	not used	Defined by write to TX FIF0
13	Timer/SSP	1	1	1	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	Internal	Internal	used	½ CLKOUT1	used	Defined by write to TX FIF0
14	Timer/SSP	1	1	0	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	Internal	External	by	½ CLKOUT1	by	External
15	Timer/SSP	1	0	1	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	External	Internal	16-bit	External	16-bit	Defined by write to TX FIF0
16	Timer/SSP	1	0	0	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	External	External	counter	External	Counter	External

X - DON'T CARE. Does not affect the selected mode. Replace X with 0 while writing to the registers

u - Used to define other functions in the selected mode. 0 and 1 valid options.

SSP Option - This options refers to all features of the standard SSP, with out the use of ESSP register bits.

Table 8 ESSP configuration - Table B - Continuous Mode

		SSPCR			SSPMC register								SSPST register											
Option	**Function**	**FSM**	**MCM**	**TXM**	**SSPRST**	**SPI**	**CHB1**	**CHB0**	**MMODE**	**GPI**	**CHLT**	**GPC**	**FSN**	**FSXOX**	**FSXST**	**CKN**	**CLXOX**	**PRSEN**	**BYTE**	**CLKX**	**FSX**	**CLXCT**	**CLKX rate**	**FSXCT**	**FSX rate**
1	RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	External	External	not used	-	not used	-
2	SSP Option	0	0	0	0	0	X	X	0	0	X	0	0	0	0	0	0	0	0/1	External	External	not used	External CLKX only	not used	External
3	SSP Option with FSXCT	0	0	1	0	0	X	X	0	0	X	0	0	1/0	0	0	X	1	0/1	External	Internal	Not used	External CLKX only	Used for internal FSX	Internal FSX. Defined by FSXCT
4	SSP Option	0	0	1	0	0	X	X	0	0	X	0	0	0	0	0	X	X	0/1	External	Internal	not used	External CLKX	not used	TX FIFO write rate
5	SSP Option	0	1	0	0	0	X	X	0	0	X	0	0	0	0	0	X	0	0/1	Internal	External	not used	½ CLKOUT1	not used	External FSX
6	SSP Option with CLXCT	0	1	0	0	0	X	X	0	0	X	0	0	0	0	0	X	1	0/1	Internal	External	used for CLKX	½ CLKOUT1 or Pre-scaled	not used	External FSX
7	SSP Option with 8-bit Prescalars	0	1	1	0	0	X	X	0	0	X	0	0	1	0	0	X	1	0/1	Internal	Internal	used for CLKX	½ CLKOUT1 or Pre-scaled	used	Defined by FSX Pre-scale
8	SSP Option	0	1	1	0	0	X	X	0	0	X	0	0	0	0	0	X	0	0/1	Internal	Internal	not used	½ CLKOUT1	not used	Defined by write to TX FIF0
9	SSP Option with CLXCT	0	1	1	0	0	X	X	0	0	X	0	0	0	0	0	X	1	0/1	Internal	Internal	used for CLKX	½ CLKOUT1 or Pre-scaled	not used	Defined by write to TX FIF0
10 11 12	Multi-channel will work in Burst mode only. FSM bit is a don't care for this mode. SPI module will work in Burst mode only. FSM bit is a don't care for SPI mode.																								
13	Timer/SSP	0	1	1	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	Internal	Internal	used	½ CLKOUT1	used	Defined by write to TX FIF0
14	Timer/SSP	0	1	0	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	Internal	External	by	½ CLKOUT1	by	External
15	Timer/SSP	0	0	1	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	External	Internal	16-bit	External	16-bit	Defined by write to TX FIF0
16	Timer/SSP	0	0	0	0	0	0	0	0	u	u	1	0	0	0	0	0/1	1	0/1	External	External	counter	External	Counter	External