TMS320 DSP
DESIGNER'S NOTEBOOK
Number 90

TMS320C6201 System Clock Circuit Example

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Design Problem

How do I provide the TMS320C6201 with a system clock?

Solution

All of the clocks internal to the 'C6201 are generated from a single source through the CLKIN pin. This source clock for the device is an external signal that, depending on the clock mode, either drives the on-chip Phase-Locked Loop (PLL) circuit to generate the internal CPU clock or becomes the internal clock. The source clock may be derived from either an oscillator chip or a clock synthesizer circuit and should be generated from a 3.3V source. Ensure that all clock traces are as short as possible to minimize the distortion of the clock signal.

There are two PLL modes for the device operation:

- CLKMODE x1
- CLKMODE x4

For the x1 mode, all six of the external PLL components may be removed from the design. Also, PLLV must be connected directly to the 2.5V source and the PLLF and PLLG pins should be tied directly together.

For the x4 mode, the values for the PLL circuit (C1, C2, and R2) depend on the CLKIN and CLKOUT frequencies. Table 1 lists component values that can be used for CLKOUT1 frequencies between 100 and 200MHz.

Table 1 : PLL Component Selection Table[1]

Cycle Time (ns)	CLKMODE	CLKIN (MHz)	CLKOUT1 (MHz)	R1 (Ω)	C1 (μF)	C2 (pF)	EMI filter part no.[2]	Lock Time (μs)
5	x4	50	200	16.9	.15	2700	TDK #153	59
5.5	x4	45.5	181.8	13.7	.18	3900	TDK #153	49
6	x4	41.6	166.7	17.4	.15	3300	TDK #153	68
6.5	x4	38.5	153.8	16.2	.18	3900	TDK #153	70
7	x4	35.7	142.9	15	.22	3900	TDK #153	72
7.5	x4	33.3	133.3	16.2	.22	3900	TDK #153	84
8	x4	31.3	125	14	.27	4700	TDK #153	77
8.5	x4	29.4	117.7	11.8	.33	6800	TDK #153	67
9	x4	27.7	111.1	11	.39	6800	TDK #153	68
9.5	x4	26.3	105.3	10.5	.39	8200	TDK #153	65
10	x4	25	100	10	.47	8200	TDK #153	68

It is recommend that 1% resistors be used in the PLL circuit, although 5% resistors are expected to work as well. Also, 10%-tolerance ceramic chip capacitors should be used for their low inductance. Any filter similar to the TDK should provide proper functionality, especially if it has a wider attenuation range.

In multiple-‘C6201 designs, it is important to provide a separate PLL filter circuit to each DSP. Multiple chips on a single filter will not work properly. The DSP will not function properly in x4 mode without a PLL filter.

Figure 1 shows a simple oscillator circuit providing a CLKIN signal to the ‘C6201. If an oscillator is used, its output can be connected to the CLKIN pin of the DSP through a series resistor.

When selecting an oscillator, it is important to note that all rise/fall timings in the ‘C6201 data sheet are based on 20% to 80%, while most oscillators base their timings on a 10% to 90% range. The JITO oscillators from Fox and Oak model 342 are two oscillator sources that should work with the ‘C6201.

[1] This Table is for CLKMODE x4 only. For CLKMODE x1, all six external PLL components may be removed. For this case, PLLV should be connected directly to the 2.5V supply, and the PLLG and PLLF pins should be tied together.
[2] Full EMI filter part number: ACF 451832-153-T

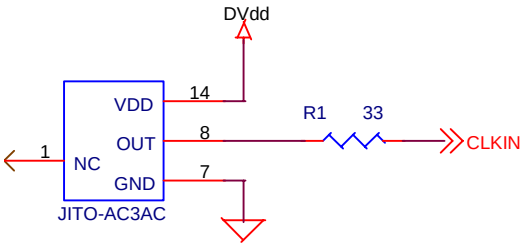

Figure 1: Oscillator Circuit for CLKIN

The circuit shown in Figure 2 demonstrates how to generate the CLKIN signal using a clock synthesizer circuit rather than an oscillator chip. If a synthesizer circuit is used, the internal PLL must be bypassed in 1x mode. MicroClock[3] has developed a clock customized for use with Texas Instruments' DSP products. It requires a single 20MHz crystal and generates a high quality clock signal with a frequency of 118MHz to 200MHz based on the value of CLK_SEL[2:0] (000b for 200MHz).

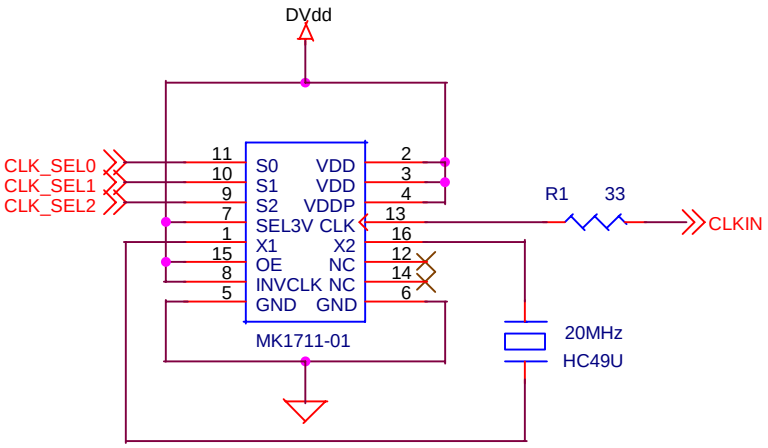

Figure 2: Clock Synthesizer Circuit for CLKIN

Figure 3 shows the locations within the device where each 'C6201 clock is generated. Essentially, the input clock either bypasses the PLL or is multiplied by four within it to generate CLKOUT1, which serves as the internal clock to the device. CLKOUT1 is then used to generate external clocks CLKOUT2, SSCLK, and SDCLK.

CLKOUT1 serves as the internal clock for the rest of the DSP and is used to generate three other clock signals for memory interface: CLKOUT2, SDCLK, and SSCLK. For a complete description on how these clock signals are generated and what their relationship is to CLKOUT1, please see the "External Memory Interface" section of the *Peripherals Reference Guide*.

The necessary filter components for the PLL circuit on the device are also shown in Figure 3. Note that pin 1 of the EMI filter is connected to 2.5V via a jumper. This allows for migration to 3.0 silicon, which calls for 3.3V on this pin. Circuits should be designed with a jumper selecting which power plane pin 1 of the EMI filter is connected to for upward compatibility.

[3] For more details on MicroClock, see their website at http://www.microclock.com.

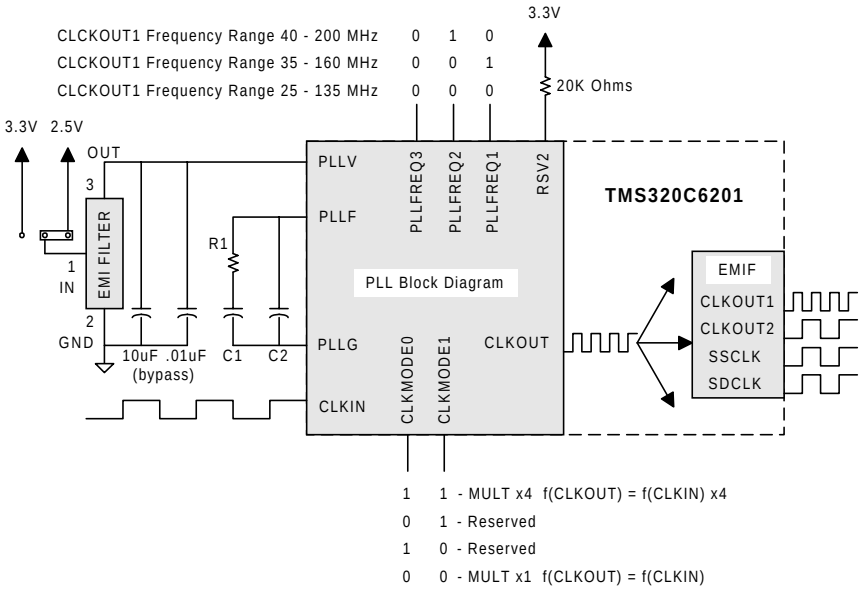

Figure 3: Clock Signals for the TMS320C6201

The values to which the PLLFREQ[3:1] pins should be set is determined by the frequency of CLKOUT1 when using x4 mode. Even though the frequency ranges given in Figure 3 overlap, the lowest frequency range including the desired frequency is the one that should be used to maximize performance. Thus,

- PLLFREQ = 010b should only be used for frequencies between 161 and 200MHz
- PLLFREQ = 001b should only be used for frequencies between 136 and 160MHz
- PLLFREQ = 000b should be used for all slower frequencies.
- All other PLLFREQ values are reserved.

References:

TMS320C6201 Peripherals Reference Guide, Texas Instruments, 1998, Literature number SPRU190