TMS320 DSP
Number 79
DESIGNER'S NOTEBOOK
TEXAS INSTRUMENTS

Initializing the TLC32040 AIC on the TMS320C5x DSK

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Design Problem What is the proper way to initialize the registers of the AIC, given a certain prototype (sampling frequency and low-pass cut-off frequency)?

Solution The main problem which is often encountered consists in setting the correct AIC parameters in order to meet the specifications of a digital filter in terms of sampling frequency and bandwidth.

Introduction

The purpose of this Designer's Notebook page is to provide an easy and efficient way to:

- Study the effects of anti-aliasing according to the sampling frequency (limited to 19.2 kHz for a TLC32040 device) and the low band-pass cut-off frequency.
- Adapt a given prototype defined by its band-pass to the hardware specifications of the TMS320C5x DSP Starter Kit (DSK).
- Synthesize a digital filter and implement it on a 'C5x DSK.

The programs enclosed in the appendices consist in sampling an analog input signal issued from a function generator (e.g., a sinewave) and sending it back to the analog output of the AIC, for visualization on an oscilloscope.

Overview

The initialization of the system can be divided into three distinct parts:

- Initialization of the DSP (software wait-states, sign extension mode, global interrupt register, etc.);
- Initialization of the timer and serial port (e.g., Master Clock frequency, receive and transmit registers, etc.);
- Initialization of the AIC (sampling frequency, low pass-band cut-off frequency, and other parameters, etc.).

The initialization of the 'C50 DSP on the DSK board (status and control registers for wait-state generation, interrupt flags settings, etc.) as well as the initialization of the timer and serial port are explained in details in the *TMS320C5x User's Guide* (SPRU056), specifically chapters 3 and 5.

The initialization of the AIC is based on three parameters:

- The AIC control register (to set up gain, synchronization, loopback, etc.);
- The Tx counter A register (and Rx counter A if synchronous mode is disabled);
- The Tx counter B register (and Rx counter B if synchronous mode is disabled).

The above parameters, in turn, are based on the two following frequencies specified by the system:

- The sampling frequency, F_s;
- The low pass-band cut-off frequency, Fc_{LP}.

In this example, Tx counter A and Tx counter B (also named TA and TB) AIC registers are used in synchronous mode to determine the D/A (and therefore A/D) conversion timing.

The low band-pass cut-off frequency is determined by the approximate formula below:

$$Fc_{LP} = \frac{f_{MCLK}\,(kHz)}{288\ kHz} \times \frac{1}{2} \times \frac{1}{TA} \times 3.6\ kHz$$

(where f_{MCLK} is supplied by the TOUT pin of the DSP and will be equal to 10 MHz in this example).

In case a pass-band filter is used (cf. programmation of the AIC_CTR register), the high band-pass cut-off frequency is determined by the approximate formula below:

$$Fc_{HP} = \frac{f_{MCLK}\,(kHz)}{288\ kHz} \times \frac{1}{2} \times \frac{1}{TA} \times 300\ Hz$$

Method to Determine TA and TB Values According to F_s and F_c

Note: More detailed information regarding the protocol of transmission between the DSP and the AIC can be found in the TLC32040 AIC data sheet (SLAS014).

The TLC32040 AIC integrates a low-pass, switched-capacitor, output-reconstruction filter. In order for the switched-capacitor low-pass or band-pass to meet their transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratios of the clock frequencies to 288 kHz, as it appears in the two formulas above.

The sampling frequency is given by the following formula:

$$F_s = f_{MCLK} \times \frac{1}{2} \times \frac{1}{TA} \times \frac{1}{TB}$$

Once f_{MCLK} is fixed, F_s depends on the TA × TB value and Fc_{LP} depends only on the TA value Therefore, TA and TB are entirely defined by F_s and Fc_{LP} with the following constraints:

1. TA is an integer in the range 4 to 31 (5 unsigned bits).
2. TB is an integer in the range 2 to 63 (6 unsigned bits).
3. F_c as near as possible, but less than F_s /2, to satisfy the *Shannon criteria*.

The procedure to determine TA and TB parameters is the following:

Step 1: Calculate TA × TB related to the desired sampling frequency. Note that if the sampling frequency is not a constraint for your application, then it has to be chosen at least $2xF_c$ according to the *Shannon criteria* and so that TA × TB is an integer.

Step 2: Considering that TA × TB is an integer, within the list of all possible integer values of TA and TB, only some of them satisfy the two first conditions.

Step 3: The user must then choose between these results with the one which satisfies the third condition, on calculating Fc_{LP}.

Example

For an application requiring a sampling frequency F_s= 9.6 kHz and in order to satisfy the *Shannon criteria*, the bandwidth must be limited to 4.8 kHz. Hence, it is recommended to filter the input signal by a low-pass filter with a cut-off frequency of $F_c=\frac{F_s}{2}$ =4.8 kHz. According to the explanations above, the results are:

$$\begin{cases} Fc_{LP} = \dfrac{f_{MCLK}}{2 \times TA} \times \dfrac{3.6}{288} = \dfrac{62.5\,kHz}{TA} \\ TA \times TB = \dfrac{f_{MCLK}}{2 \times F_S} = 625 = 5^4 \end{cases}$$

and the constraints are: $\begin{cases} 4 \le TA \le 31 \\ 2 \le TB \le 63 \end{cases}$

The easiest way to study the different possibilities to obtain the desired sampling frequency and the appropriate cut-off frequency is to fill up a table as shown in Figure 1. The fixed parameter is f_s = 9.6 kHz which involves a product TA × TB = 5^4. First, fill the first column by giving to TB all the possible combinations of the prime factors.

TB	TA	TA × TB	f_c (kHz)
5	125 > **31**		
25	**25**	**625**	**2.5**
125 > **63**			

Figure 1. Possible Values of TA and TB According to Desired f_c and f_S

Only one combination is acceptable:

TA=25 and TB=25 giving a cut-off frequency of 2.5 kHz.

To select one of these set of values, you have to consider the desired cut-off frequency of your anti-aliasing filter and, then, choose the most appropriate. For the 9.6 kHz sampling frequency, the ideal anti-aliasing filter rejects all frequencies above 4.8 kHz. Hence, you will have to adopt the combination: TA=25 and TB=25 and to satisfy with Fc_{LP} = 2.5 kHz.

According to the *Shannon criteria*, the optimized operating conditions are obtained when $f_c \le \frac{f_s}{2}$. Therefore, in most of the cases, we recommend to have f_c as near as possible, but less than $\frac{f_s}{2}$. In case of filtering a signal under aliasing conditions, we let the user choose the most appropriate values for TA and TB registers which depend on the non-disturbed pass-band authorized for the application.

Besides the three steps of establishing the communications between a DSP and the TLC32040 AIC, interrupt service routines must be defined to set up the action to follow after a data word has been received by the AIC or transmitted to it. The main program calls the different routines corresponding to the initialization process, enables or disables the interrupt registers whenever required, then waits for data to be handled by the receive interrupt service routine.

This program, called AICDSK50.ASM, can be downloaded from the TI DSP BBS or ftp site mirror. It can be assembled and linked by the tools supplied with a DSK. The following procedure tells you how to assemble this program to have it run on your board:

DSK5A AICDSK50.ASM (generates the AICDSK50.DSK file)
DSK5L AICDSK50

Operating Recommendations

Analog Input: - Maximum Absolute Input Voltage: 3 V
- Frequency range: 200 Hz–2500 Hz for F_S=8 kHz

Under these recommendations, you should obtain the following results:

Experimental Results

Software Programmation				Hardware Results on a DSK	
F_S (in kHz)	**TA**	**TB**	**F_C (in kHz)**	**Band-Pass (Fc_{LP})**	**Aliasing**
4	25	50	2.5	200–1500 Hz	Yes
8	25	25	2.5	200–2500 Hz	No
10	20	25	3.125	260–3000 Hz	No
10	10	50	6.25	530–3600 Hz	Yes

The results obtained when F_S=8 or 10 kHz (first case) correspond to the case where $F_S > 2F_C$ (see Figure 2).

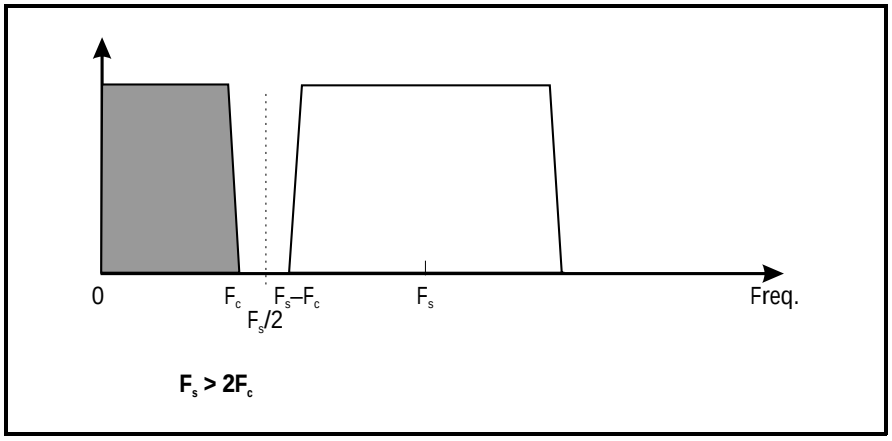

Figure 2. Shannon criteria satisfied

The *Shannon criteria* is satisfied. The band-pass obtained matches with the values of the cut-off frequencies calculated by the formulas above. The first and last result correspond to the case where $F_S < 2F_C$.

The results obtained for these values of TA and TB confirm the presence of aliasing in the output signal between 1.5 kHz and 2.5 kHz for the first case and between 3.6 and 6.25 kHz for the last result. The output signal is not stable on the screen of the oscilloscope, when synchronized by the input signal.

Interpretation

Theoretically, let us consider a low-pass filter instead of a band-pass filter to simplify the reasoning (see Figure 3). Then, all the frequencies between 0 and $F_s/2$ are sampled according to the *Shannon* rule, but the frequencies in $[F_s/2, F_c]$ are under aliasing. Because of the resulting superposition in the spectrum, the resulting non-disturbed bandwidth is actually $[0, F_s–F_c]$ (as represented in the shaded portion in Figure 3).

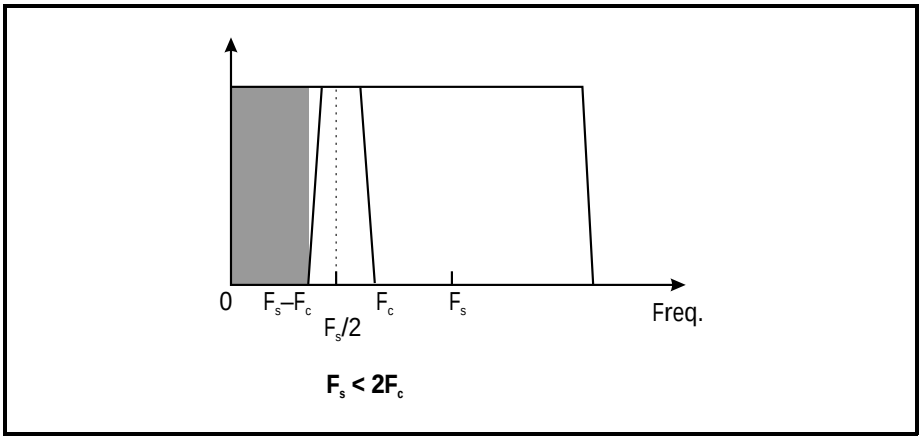

Figure 3. Shannon criteria unsatisfied: aliasing

Experimentally, for the first case, we observe that [200–1500 Hz] is not at all modified by aliasing. In the range [1.5, 2.5 kHz], the signal is subject to aliasing. After 2.5 kHz, the amplitude of the signal falls down.

This Designer's Notebook page compliments Designer's Notebook page #57, Initializing the TMS320C5x DSK Board.