TMS320 DSP
DESIGNER'S NOTEBOOK
Number 69
TEXAS INSTRUMENTS

Viewing TMS320C8x Register Bit Fields and Memory-Mapped Registers in the HLL Debugger

Contributed by Leor Brenman

Design Problem

How can I observe 'C8x register bit fields in the 'C8x HLL debugger? As an example, the MP configuration register, CONFIG, contains the four-bit "type" bit field in bit locations 12 through 15. This field indicates the number of PPs on the particular 'C8x device.

Solution

This document is based on Designer Notebook page #60, *Accessing Status and Control Fields and I/O Ports in the TMS320Cxx HLL Debugger*, but differs enough in actual content and has unique files associated with it to warrant a separate Designer's Notebook page.

Many of the 'C8x registers have individual bit fields. While the 'C8x HLL debugger displays the register values in the CPU register window of the HLL debugger it is not always convenient to view the bit fields in this window. Also, some of the 'C8x registers, such as the VC and TC registers, are memory-mapped, and these are not displayed in the CPU register window.

The 'C8x HLL debugger does not support access of register bit fields and memory-mapped registers natively. However, the 'C8x HLL debugger does have several features that can help display desired field(s) and memory-mapped register in an easy-to-observe manner. One is the WATCH window and watch command, wa. To view the "type" field of the CONFIG register enter the following command in the command window of the MP debugger:

```
wa (CONFIG>>12)&0xf,type,x
```

The watch window will display the word "type" followed by a hexidecimal value that represents bits 12 through 15 of the MP CONFIG register. Omit the ,x to display this value in decimal.

The 'C8x contains several memory-mapped register such as the TC and VC control and status registers. To view a memory-mapped register, such as the TC register REFCNTL located in memory at address: 0x01820000, enter the following command in the command window of the MP debugger:

```
wa (*(0x01820000)>>00)&0xffffffff, REFCNTL,x
```

The watch window will display the word "REFCNTL" followed by the hexidecimal value that represents the 32 bits at location 0x01820000. REFCNTL is made up of two 16-bit registers, REFRATE and RPARLD. By masking off the correct lower and upper half words of REFCNTL, you can observe these two registers as follows:

```
wa (*(0x01820000)>>00)&0x0000ffff,REFRATE,x
wa (*(0x01820000)>16)&0x0000ffff,RPARLD,x
```

These examples are specific to the 'C8x, but can be easily adapted for any other generation of TMS320 DSPs. To avoid having to rewrite these expressions with each debugger session, these expressions can be stored in a take file (see the debugger manual for information on take files). For example, several watch commands to view PP condition flags, stored as bit fields in the status register, sr, can be placed in a file, PPstatus.cmd, as follows:

```
; Filename: PPstatus.cmd
; PP Status register: sr
wa (sr>28)&0x01,Z (Zero):
wa (sr>29)&0x01,V (Overflow):
wa (sr>30)&0x01,C (Carry):
wa (sr>31)&0x01,N (Negative):
```

Enter the following command from the PP debugger command window to display the status codes:

```
take PPstatus.cmd
```

Refer to Designer Notebook page #60 for information on how to create aliases to view, watch, and modify bit fields of registers and memory-mapped registers.

The BBS archive file, HLLREGS.EXE, contains two sets of take files, one set for the PP and one set for the MP. Each take file contains watch commands to display the bit fields of a particular register. After these files have been downloaded, add the path to the directory that contains these files to the D_DIR environment variable. By doing so, these files can be "take"-en regardless of which directory the debugger is invoked from. Table 1 summarizes the files that are included in the archive file.

Processor	Filename	Register
PP	PPcomm.cmd	comm
PP	PPcondfl.cmd	sr, condition flags only
PP	PPd0.cmd	d0, for EALU ops
PP	PPinten.cmd	inten
PP	PPintrgs.cmd	inten and intflg
PP	PPintflg.cmd	intflg
PP	PPlctl.cmd	lctl
PP	PPstatus.cmd	sr
MP	MPconfig.cmd	config
MP	MPemurgs.cmd	ecomcntl, anastat, brk1, brk2 (XDS510 only)
MP	MPfltop.cmd	fltop
MP	MPflttag.cmd	flttag
MP	MPfpst.cmd	fpst
MP	MPie.cmd	ie
MP	MPintrgs.cmd	ie, intpen
MP	MPintpen.cmd	intpen
MP	MPmftrgs.cmd	fltop, flttag, fltadr, fltdth, fltdtl
MP	MPpktreq.cmd	pktreq
MP	MPpperr.cmd	pperror
MP	MPtcregs.cmd	All TC registers
MP	MPvcfrgs.cmd	All VC frame timer registers
MP	MPvcsrgs.cmd	All VC SRT registers

Table 1. Files included in the archive file