TMS320 DSP
DESIGNER'S NOTEBOOK
Number 65

# Interfacing External Memory to the TMS320C5x DSK

*Contributed by Gerald Capwell*

***Design Problem*** How can I connect external program and data memory to the 'C5x DSK? Do I need a special board?

***Solution*** As DSK users become more familiar with programming DSP algorithms, the 10K on-chip RAM size may not be sufficient. Adding external memory is done by soldering connectors on the DSK's JP headers and plugging them into either a development perf board or a dedicated memory module. In either case, the DSK has the opposite gender connector of the interfacing board. It is not recommended to use low-profile connectors, which may inhibit the use of the board space underneath the DSK. Figure 1 illustrates how an unpopulated 4" × 6" perf board can interface to the DSK and be used to create a "work area."

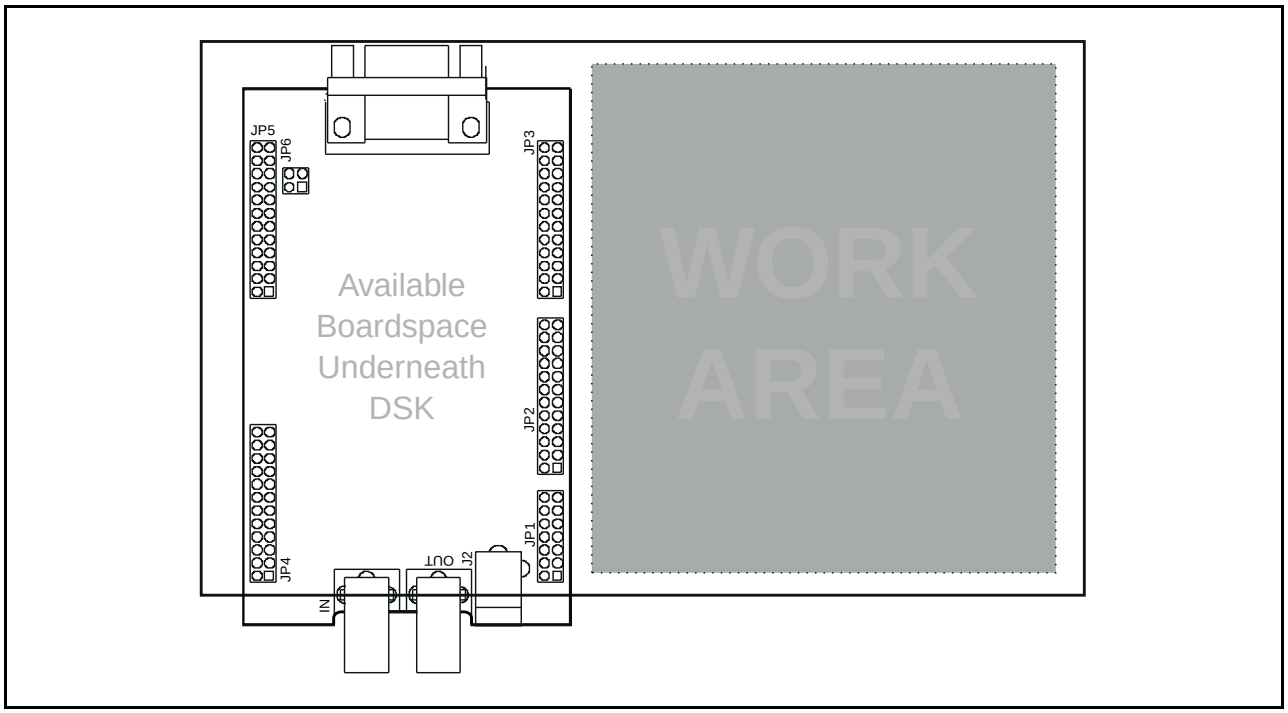


*Figure 1. Example of the DSK "work area"*



**US TMS320 HOTLINE (713) 274-2320 US TMS320 FAX (713) 274-2324 US TMS320 BBS (713) 274-2323 US email=4389750@mcimail.com**

The work area can be used to interface the DSK to many devices including external memory. It is suggested that **regulated** power be supplied to the work area via separate external regulators. The on-board DSK regulators cannot tolerate heavy external loads. Unregulated ±12-V power for loads less than 500 mA can be taken from the V+ and V– pins on the JP headers. However, it is recommended the work area and DSK power sources be independent of each other. In order to isolate the work area from the DSK power, it is suggested that the work area power source be the 9-V AC (rated @ 1 A or higher) adapter, then full wave rectified and regulated at the work area as needed.

Once you have a perf board and power source, interfacing the memory to the DSK is quite simple. The address and data lines of the DSP are located on the JP3 and JP2 headers respectively. The control lines such as, the read strobe ($\overline{RD}$), write strobe ($\overline{WE}$), program strobe ($\overline{PS}$), and $\overline{STRB}$ are located on JP5. Figure 2 illustrates how the DSK headers are used to connect two 128K × 8 memory devices.

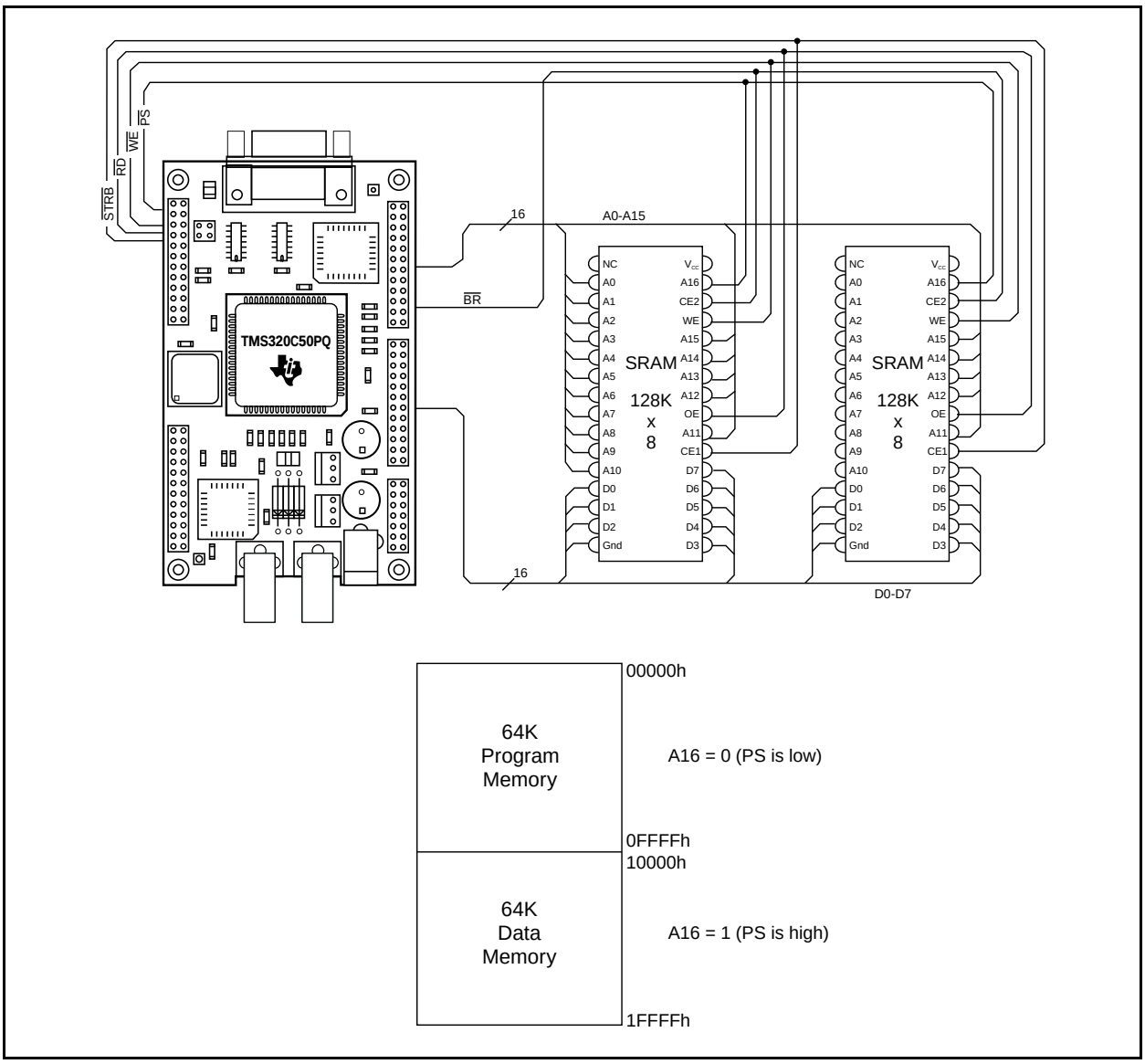


*Figure 2. Connecting external memory to the 'C5x DSK*

One 64K block of memory is used as program memory while the second 64K block is used for data memory. Accesses to the data and program memory are controlled by the $\overline{PS}$ line. Each time the DSP accesses external program memory, the $\overline{PS}$ line goes low, driving A16 low and forcing access to memory locations 00000h – 0FFFFh. Data memory accesses have no effect on the $\overline{PS}$ line (it remains high), therefore memory locations from 10000h – 1FFFFh are accessed.

When the DSP attempts to read external memory, the $\overline{RD}$ line is asserted low. The $\overline{RD}$ line is connected to the memory output enable pin ($\overline{OE}$). When the DSP attempts to write to external memory, the $\overline{WE}$ line is asserted low. The $\overline{WE}$ pin is connect to the memory write enable pin ($\overline{WE}$).

Chip selection pins of the memory device are used to determine when the device has control of the buses. When the initial power-up sequence begins, the DSP will attempt bootloading from the on-board EPROM. The on-board EPROM resides in external memory and **must** have control of the buses. During the bootloading sequence, the data strobe ($\overline{DS}$) and bus request ($\overline{BR}$) lines are brought low to indicate a global data memory access. The external RAM must release control of the buses to the EPROM. Therefore, the external RAM can be enabled (chip selected) only when $\overline{BR}$ is high. Another situation where the RAM must release control of the buses is when the I/O strobe ($\overline{IS}$) is active. External I/O devices are usually activated by the $\overline{IS}$ signal. In Figure 2, the external RAM is enabled only when $\overline{BR}$ is high (CE2) and $\overline{STRB}$ is low ($\overline{CE1}$). It is not required for the RAM device to have an active low chip select ($\overline{CE1}$). The $\overline{CE1}$ pin connects to the strobe ($\overline{STRB}$) pin in order to activate the chip only when external accesses occur, and therefore reducing memory power consumption. In this particular application, the I/O memory is mapped into the 64K data memory block.

In order to use the $\overline{BR}$ pin, you must modify the DSK board. The $\overline{BR}$ pin is not accessible and must be physically connected to a JP header. The most convenient location where the $\overline{BR}$ signal can be found is at pin 23 of the EPROM. Pin 23 of the EPROM is connected to a copper pad and through hole. A piece of wirewrap wire can be soldered to the underside of the through hole and routed to a pin on JP3. Pin 2 of JP3 is connected to $\overline{INT2}$, but can be removed without effecting the board operation. The $\overline{INT2}$ pin connects to a copper pad and through hole on the underside of the DSK. Etch a small portion of the copper PCB run away from the through hole and solder the end of the wirewrap wire to the existing copper run that connects to the header. Once this connection is made, $\overline{BR}$ is available through pin 2 of the JP3 header with no harm to the board. In fact, if you ever need the $\overline{INT2}$ signal, $\overline{BIO}$ is a duplicate signal and can be found on pin 5 of JP2. If you do not want to modify the board, you must add external logic to control the RAM chip select lines. The logic must disable the RAM when the $\overline{IS}$ or $\overline{BR}$ signals are brought low indicating I/O or global space accesses. The associated time delays of the additional logic must be considered when determining the required memory speed.

When deciding on a memory device, be sure to satisfy the timing specifications found in Appendix A of the *TMS320C5x User's Guide*. Remember that the 'C5x DSP is designed for one-cycle reads and two-cycle writes (0 wait states). Therefore, if you satisfy the one-cycle read timing specification, the two-cycle write operation is also satisfied. The read cycle timing specification, referred to as $t_{a(A)}$ or "read data access from address valid," can be found on page A-14 of the *TMS320C5x User's Guide*. The $t_{a(A)}$ specification represents the maximum time in which the external memory must drive valid data onto the data bus after the 'C5x has supplied a valid address on the address bus. For more information regarding the operation of the DSP's external memory interface, please refer to appendix B of the *TMS320C5x User's Guide*.