TMS320 DSP
Number 6
DESIGNER'S NOTEBOOK
TEXAS INSTRUMENTS

# 'C5x EVM Provides for Audio Processing

*Contributed by Joe George*

***Design Problem*** How do I interface a 'C5x to analog signals?

***Solution*** The TMS320C5x EVM, with its input/output RCA jacks and TLC32046 Analog Interface Chip (AIC), offers an easy-to-configure system for audio processing. Whether implementing simple delays and echoes or complex multi-filter digital reverberation, 'C5x features make it easy. Some simple artificial digital reverberation code with absolute delay that simulates four echoes in a room is available on the TMS320 BBS in the file C5XEVAUD.EXE.

The code first initializes the AIC and then sets up the 'C5x's two circular buffer pointers to point at different places in a single 32K word buffer (see Figure 1). This configuration corresponds to a receive pointer and a transmit pointer. In the serial port receive interrupt service routine (ISR) (Example 1), the 'C5x receives and stores data (at sample n) in the single buffer, but manipulates and transmits data stored earlier (`n-absdelay`) in the buffer. This permits a programmable absolute delay, which makes any processing effects more obvious. The manipulation in the ISR shows the scaling of four echoes at 1 (`at n-absdelay`), 1/2 (`at n-absdelay-1*INDX`), 1/4 (`at n-absdelay-2*INDX`), and 1/8 (`at n-absdelay-3*INDX`). The echoes are then summed.

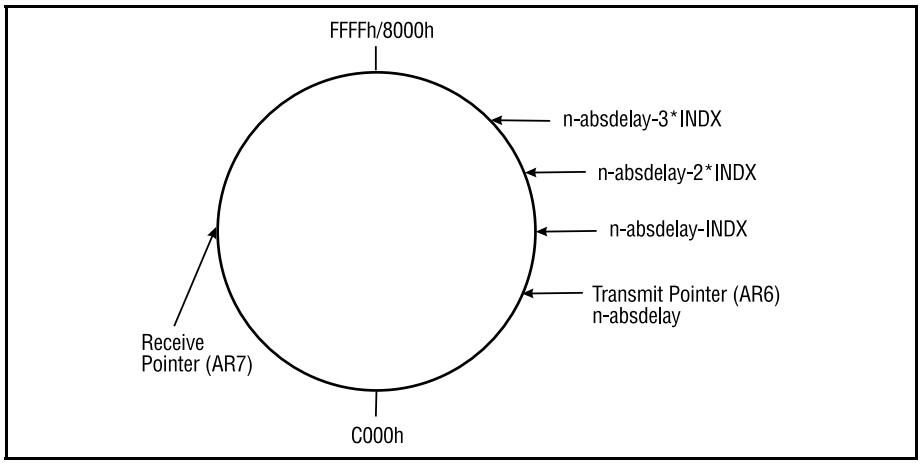


*Figure 1. 32K-word 'C5x circular buffer for reverberation*

The delay between the echoes is previously stored in the index register. This index may be varied in code to hear the effects of various inter-echo delays. To prevent the circular addressing from indexing an invalid address, write a 1 to the most significant bit (MSB) of the indirect address since the buffer from 8000h to FFFFh is always 1. This is done using the Parallel Logic Unit. A NOP is inserted for pipeline considerations as explained in Section 3.6.2 in the TMS320C5x User's Guide. Be sure to mask off the lowest two bits as zeroes at the end of the ISR since they are command bits for the AIC.

```
Example 1:
;
; SERIAL PORT RECEIVE INTERRUPT SERVICE ROUTINE
;
receive:
   MAR     *,AR7           ; Receive Pointer
   LACC    DRR             ; Read sample from AIC
   SACL    *+              ; Store to buffer (at n)

   MAR     *,AR6           ; Transmit Pointer
   SAR     AR6, 60h        ; Store Temp
   LACC    *0-, 16         ; Load previous value
                           ; (at n-absdelay)
                           ; (Divide by 1)

   OPL     #8000h, AR6     ; Write 1 for addressing
   NOP
   ADD     *0-, 15         ; Add previous value
                           ; (at n-absdelay-INDX)
                           ; (Divide by 1/2)
   OPL     #8000h, AR6     ; Write 1 for addressing
   NOP
   ADD     *0-, 14         ; Add previous value
                           ; (at n-absdelay-2*INDX)
                           ; (Divide by 1/4)

   OPL     #8000h, AR6
   NOP
   ADD     *0-, 13         ; Add previous value
                           ; (n-absdelay-3*INDX)
   AND     #0FFFCh, 16     ; Mask off lowest 2 bits
   SACH    DXR             ; Transmit to AIC
   LAR     AR6, 60h        ; Load back temp
   MAR     *+, AR6         ; Increment by one sample
   RETE
```

*Figure 2.*