TMS320 DSP
DESIGNER'S NOTEBOOK
Number 5

TMS320C30 Addressing up to 68 Gigawords

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Design Problem

The primary bus has 24 address lines which allow addressing up to 16 megawords of memory. The expansion bus has 13 address lines addressing 8 Kwords. How can they be used together to address a larger memory space?

Solution

This technique uses the expansion bus address lines [XA(12-0)] simultaneously with the primary address lines [A(23-0)], to extend the address to 36 bits. The feature that is used is a power-saving feature of the 'C3x family that holds the past address bits on an external bus until a new external access occurs (i.e., the A-Bus works as a latch). The following parallel instruction accomplishes this task:

```
      STI    Rx,*ARn        ; address MSTRB while loading a
                            ; value from STRB memory
   || LDI    *ARp,Rq        ;
```

where:

Rx and Rq designate registers R0 to R7 (but not the same register)
ARn and ARp designate auxiliary registers AR0 to AR7 (but not the same register).

Note: ARn contains the 8-megaword segment address plus 800000h. ARp contains the address within the 8-megaword segment and is between 0 and 7FFFFFh.

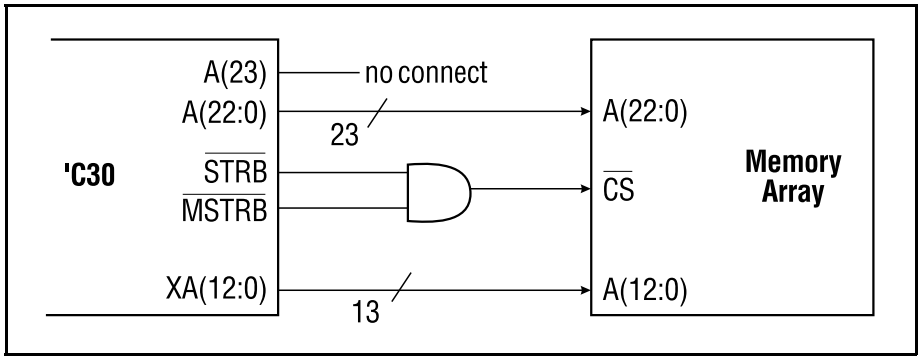

Figure 1. Solution diagram