

DESIGNER'S NOTEBOOK



TMS320C5x Interrupts and the Pipeline

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Design Problem

Given the following situation:

```
; an int is enabled and pending
CLRC    INTM
RETD
LAR     AR1,#2
MAR     *,AR1
```

If an interrupt is pending and is subsequently enabled by a CLRC instruction, where would it be taken and what happens when it returns from the ISR?

Solution

A delayed-instruction and the next two instruction words (in the two delay slots) are uninterruptible. If the delayed instruction happens to be a return-delayed then 'C5x will execute the two instructions following that, execute return and then take the interrupt trap.

Since 'clrc intm' does not enable interrupts until the next instruction is executed, which happens to be a return-delayed, any pending interrupt will be taken AFTER executing the return and the two delayed instructions:

```
CLRC    INTM    ;these 4 instructions uninterruptible
RETD
LAR     AR1,#2
MAR     *,AR1   ;interrupt taken after executing this
                ;instruction
.
.
calling_prog:    ;<-ISR will return here
```