TMS320 DSP
DESIGNER'S NOTEBOOK
Number 27

Hardware UART for TMS320C3x

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Design Problem The TMS320C3X does not offer a UART for asynchronous communication.

Solution On the DSP BBS there is a software UART emulator available. This will allow the TMS320C3x to perform asynchronous communication. There are some instances that a hardware UART may be necessary for a particular application. The following describes one possible solution for a hardware UART. This design was originally done in an FPGA and it can be easily transferred to an ASIC. Modification to this design can be done to accommodate faster data rates or different communication protocols.

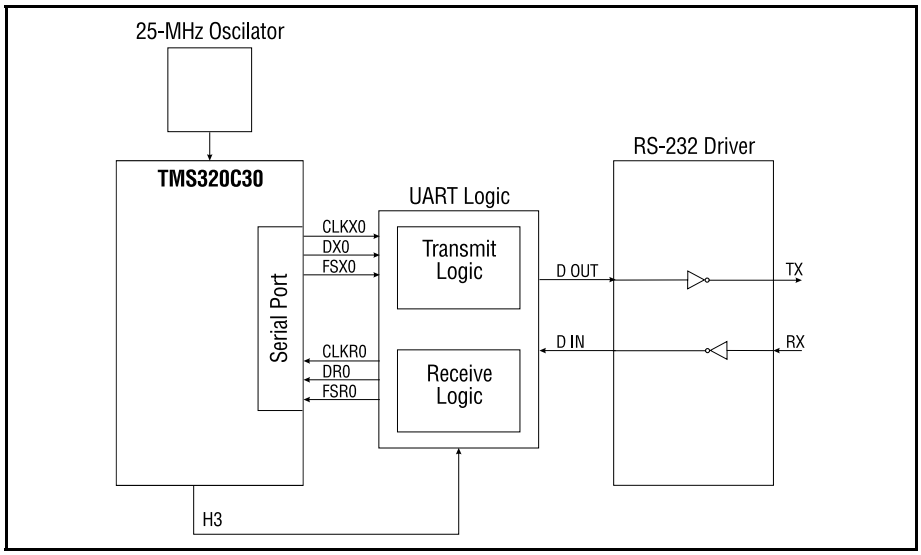

Figure 1.

The following schematic is for a 9600-baud UART with one stop bit and a start bit. The clock signal, H3, is supplied to the circuit from the TMS320C3x. The DSP was running with a 25-MHz clock, which was necessary for a particular application. Modification to the FPGA timing circuit will be necessary to accommodate a higher clock speed for the DSP.

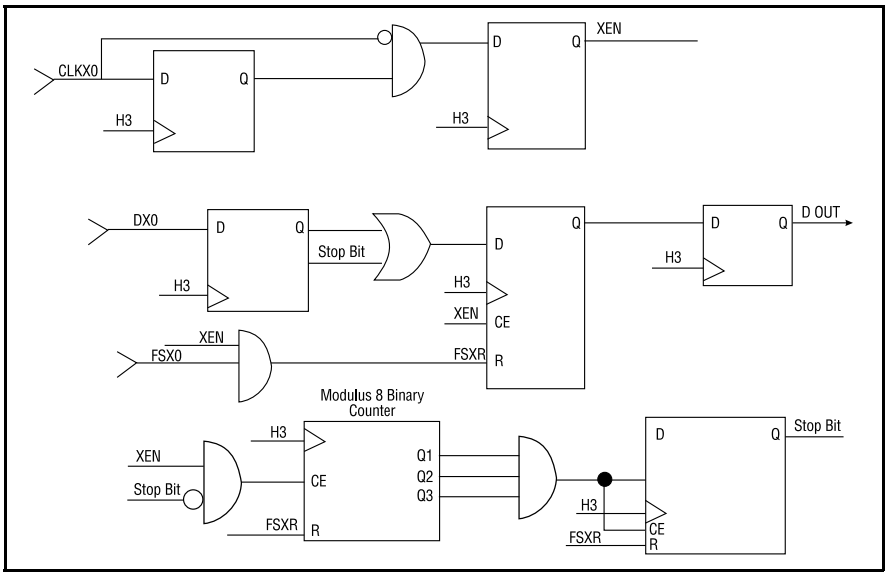

Figure 2. Transmit circuitry

The ’C30 transmit section of the serial port is configured to output eight bits of data at a rate of approximately 9.6 KHz. This is achieved by using one of the ’C30’s internal timers and programming it to the desired 9.6 KHz frequency. The transmitting port is configured in the fixed burst mode. This allows the leading FSX signals to help initiate a start bit for the UART protocols. The stop bit is generated at the end of the eighth bit by the UART circuitry.

The receive section of the UART is activated when the circuitry detects the start bit. The start bit is a logical *zero*. The *delay* circuit is activated on the falling edge of the start bit. The *delay* is used so that sampling of the incoming data bits occur in the middle of the signal level, thus causing the UART to have a higher noise immunity.

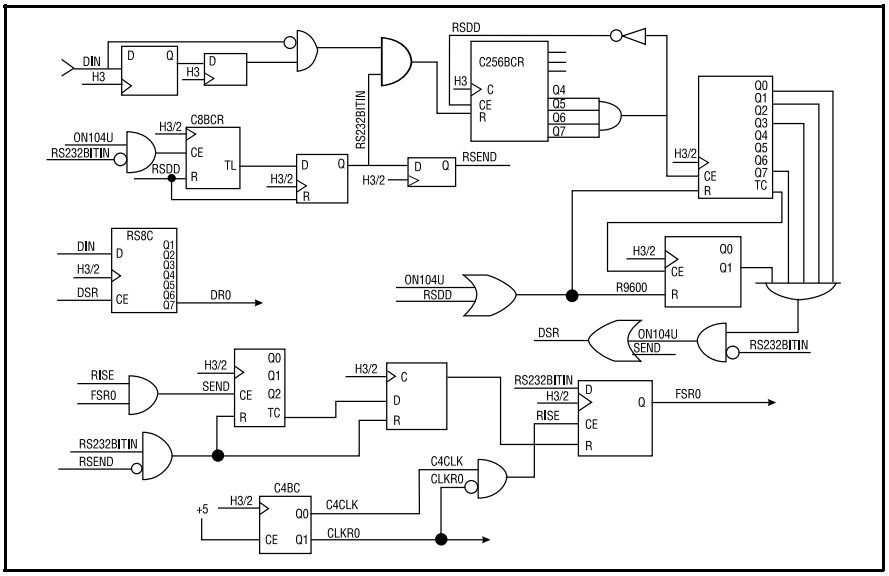

Figure 3. Receive circuitry

After the *delay* is performed, the *timer* is activated. The *timer* has a period of 104 μs, which is approximately 9.6 KHz. At each period, a data is sampled into an eight-bit shift register. After all eight bits are received, the data is passed to the 'C30 at a speed of $\frac{1}{8}$ of the H3 clock. The FPGA circuitry interfaces the 'C30 in the fixed burst mode of operation to the serial port. Both the clock and the frame sync signals are generated by the FPGA circuitry.

This UART circuitry can easily be designed into an ASIC which could also be incorporated into a Configurable Digital Signal Processor (cDSP). Modification to this circuit could be done for different serial communication protocols or even higher baud rates.