TMS320 DSP
DESIGNER'S NOTEBOOK
Number 2

Avoiding False Interrupts on the ’C3x

Contribued by Randy Preskitt

Design Problem TMS320C30 interrupts are internally latched on the falling edge of H1 (see pp. 6-20 and 13-38 of the TMS320C3x User's Guide). If the interrupt is held low for three or more H1 cycles, multiple interrupts may occur.

Solution The solution is to add a PAL clocked by H1 which intercepts the interrupt. This logic will hold the interrupt ($\overline{INTx'}$) low for two H1 cylces. The external interrupt ($\overline{INTx}$) may be held low longer or shorter, but must go high before the interrupt can be reasserted. For four external interrupts, the same logic may be repeated in the same PAL.

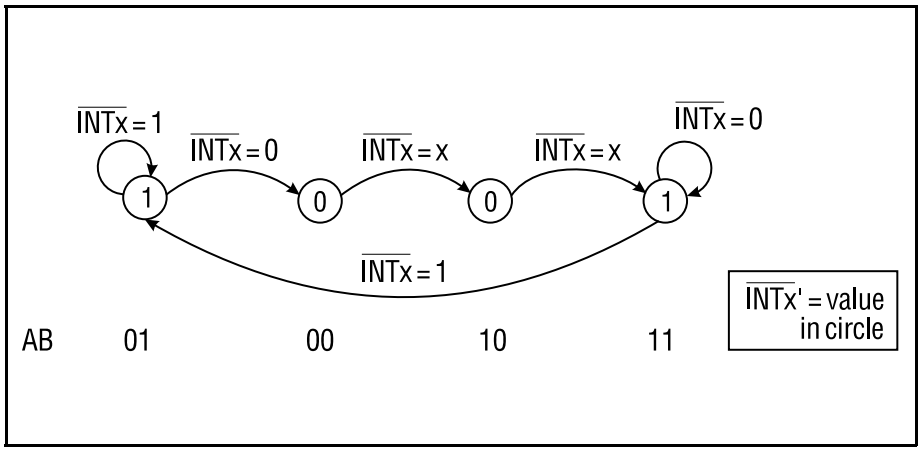

Figure 1. State diagram

(continued on next page)

TMS320 HOTLINE (713) 274-2320 TMS320 FAX (713) 274-2324 TMS320 BBS (713) 274-2323 email=4389750@mcimail.com

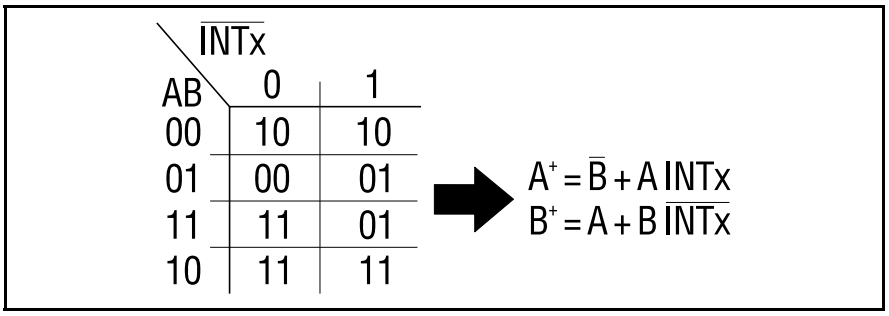

Figure 2. Karnaugh map

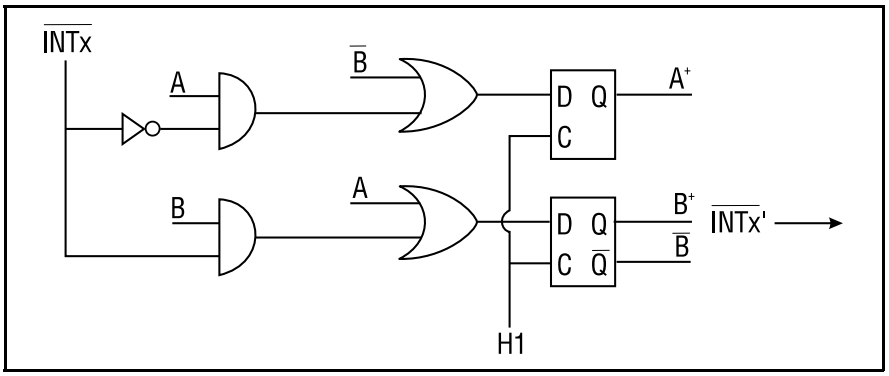

Figure 3. Logic diagram