

details on

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signal processing

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New 'C2000 DSPs provide best price/performance ratio in industry

With the introduction of four new devices, a new architecture, and the best price-to-performance ratio in the industry, TI's powerful and cost-effective TMS320C2000 DSPs are offering designers of cost-sensitive applications a better way to implement their systems and future innovations.

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New 'C2000 DSPs

Continued from page 1

For applications historically implemented with 8-, 16-, or 32-bit microcontrollers, the 'C2000 processor platform provides substantially more processing power, an easy-to-use development environment, and wide-ranging system flexibility with numerous peripherals. The highly-integrated 'C2000 DSPs deliver cost savings at both the device and system levels, enabling manufacturers of price-sensitive applications to efficiently incorporate the high performance of DSPs while maintaining the flexibility and functionality of traditional microcontrollers (MCUs).

New 'C24x DSPs optimized for digital control applications

'C24x DSPs are optimized for digital control systems (DCS), as well as power conversion and motion control

systems. In addition to the original 'C240 [read-only memory (ROM)] and 'F240 (Flash) generation members, TI has now added the 'C241, 'C242, 'F241, and 'F243 DSPs to cost-effectively address systems with reduced memory requirements. The 'F241 and 'F243 are the only DSP controllers that offer industrial motor designers 8K of reprogrammable Flash memory and control area networking (CAN). The 'C241 offers 8K of ROM and CAN.

A breakthrough in price/performance

"The combination of TI's powerful DSP processors and comprehensive digital motor control peripherals creates the industry's most integrated and versatile DSP controller solutions for closed-loop motor control applications," says Pradeep Bardia, product marketing manager for the 'C24x family of DSPs.

'C24x devices are based on TI's industry-leading DSP cores and on-chip peripherals. This combination provides flexibility, improved system

price/performance ratios, and an affordable, easy-to-use alternative to traditional MCUs.

'C24x tools and support

Design tools for these devices include TI's optimized DSP compiler, IEEE 1149.1 JTAG-based emulation tools, and evaluation module (EVM) boards. Also offered are high-level language programming options, flash-based utility programs, and source compatibility with other TMS320 fixed-point DSPs. TI's third-party network offers emulation tools, motion control kit/application support packages, and a real-time DSP operating system/kernel library for this new family of DSP controllers.

Availability

- ❑ 'F241 and 'F243 sampling scheduled to begin 2Q98.
- ❑ 'C241 and 'C242 sampling scheduled to begin 3Q98.

For more information, fill out the enclosed reply card or visit www.ti.com/sc/details51

		On-Chip Memory							Timers				Serial Ports			
									General-Purpose Timers	Watchdog Timers	Real-Time Interrupt Timers					
Device	MIPS	RAM	ROM	Flash	Dat/Pro	A/D	PWM Channels	Compares/ Captures				CAN	SPI	UART	I/O Pins	Packaging
TMS320F240	20	544	—	16K	64K/64K	Dual 10-bit	12	9/4	3	1	1	N/A	1	1	28	132 PQFP
TMS320C240	20	544	16K	—	64K/64K	Dual 10-bit	12	9/4	3	1	1	N/A	1	1	28	132 PQFP
TMS320F241	20	544	—	8K	—	10-bit	8	5/3	2	1	—	✓	1	1	26	68 PLCC, 64 PQFP
TMS320F243	20	544	—	8K	64K/64K	10-bit	8	5/3	2	1	—	✓	1	1	32	144 TQFP
TMS320C241	20	544	8K	—	—	10-bit	8	5/3	2	1	—	✓	1	1	26	68 PLCC, 64 PQFP
TMS320C242	20	544	4K	—	—	10-bit	8	5/3	2	1	—	N/A	—	1	26	68 PLCC, 64 PQFP

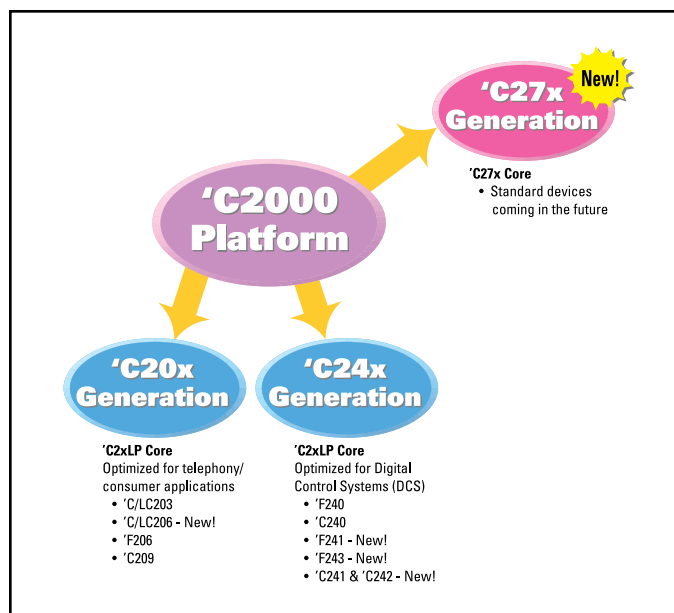
Revolutionary 'C27x architecture combines the best of DSP and MCU technologies

With the new TMS320C27x architecture, TI introduces a breakthrough that unites the flexibility, ease of use, and cost-efficiency of an MCU with the high performance of a DSP—all in a single device.

At 100 MIPS, TI's 'C27x technology

provides 10 times the performance of traditional MCUs. The architecture was custom built from the ground up to address the specific requirements of high-performance, high-precision embedded control applications. For the first time, TI will combine the high-speed multiply-and-accumulate (MAC) operations of DSPs together

with the intensive input/output (I/O) operations characteristic of MCUs in one architecture. The integration of signal processing and control functions will enable OEMs to replace multiple processors with one, or to upgrade MCUs to DSP performance while eliminating other system components, such as speed sensors or ASICs.



Industry-leading architecture

Optimized for high-performance embedded control applications, the 'C27x architecture features efficient addressing modes and specialized instructions that combine to produce the highest level of code compactness in the industry. More compact code executes faster, consumes less power, and reduces memory cost.

Development time cut in half

The 'C27x architecture features two innovations that work together to cut application development in half. A highly efficient C compiler reduces the up-front development time, while the real-time emulation component significantly decreases the time spent in debugging.

Highly efficient C compiler—To enhance the ease of use of this new architecture, TI has developed an efficient C compiler that produces compiled code denser than any MCU or DSP currently on the market. The 'C27x architecture and C compiler were designed in tandem, therefore the compiler takes advantage of the system's efficient code features, like the read-modify-write instruction set. The efficiency of the compiler supports the desire of many program-

mers to use C in embedded systems, due to its ease of use, portability, and maintenance, and enables even the most time-critical code to be written in a high-level language.

Advanced emulation capability—An important innovation for system debug and development is inclusion of TI's

new real-time debug technology in the 'C27x hardware. Used in conjunction with an integrated JTAG-based visibility port, this unique technology enables developers to see and modify internal registers and memory while the processor continues to operate at full speed in its normal mode. Designers can service real-time interrupts while single-stepping through non-time-critical code. (See RTDX sidebar.)

Roadmap for future growth

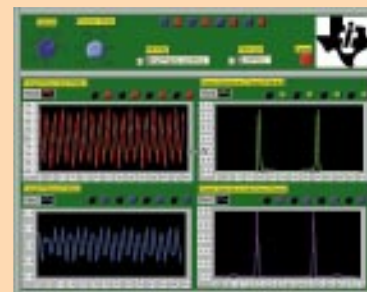
The 'C27x DSP core is designed using a 0.25-micron CMOS process operating at speeds up to 100 MHz, with a roadmap for migration to 0.18 microns and 150+ MHz. 'C27x standard products are planned for the first half of 1999.

To enable faster time to market, the 'C27x is supported by TI's extensive third-party network which offers a wide range of software and hardware tools. This network provides a wide range of software and hardware tools, including debuggers, emulators, development boards, and real-time operating systems, from both the DSP and MCU industries. For the latest on tools availability and 'C27x, visit www.ti.com/sc/details51 or to receive information by mail, fill out the enclosed reply card.

RTDX eases system analysis

Real-Time Data Exchange (RTDX™) is an advanced DSP analysis technology that provides a real-time visibility port, or window, into device performance. With RTDX, developers can monitor, analyze, and modify code executing at 100 MHz without impacting results or halting applications.

Through the RTDX window, users can display the state of the system graphically or save the data to a file while the processor is running at full speed. With greater visibility into system operations, developers can easily optimize their designs and maximize their system performance in a shorter time.



The emulation logic built into TI DSP cores allows users to transmit and receive data between the host and target DSP at a rate of 8 kilobytes per second, sufficient for running control, servo and audio applications at full speed. Transfer rates for future devices, including DSPs based on the 'C27x, will feature RTDX bandwidth increases of 10 times or more.

For more information, fill out the enclosed reply card or visit www.ti.com/sc/details51

TMS320C32 priced to win!



Available today. The lowest-cost floating-point processor on the market today, the 'C32, is available in any quantity for US \$9.95.

The 40-MHz TMS320C32 is now priced at US \$9.95 for any quantity.

This price reduction, along with the easy-to-use development tools, enables design engineers to develop cost-effective products and introduce them to the marketplace in record time. TI's continued commitment to provide DSP Solutions is reflected in the new US \$9.95 flat pricing of the 'C32 DSP.

The 'C32 debuted in 1995, breaking the US \$10 barrier for floating-point DSPs in 250,000 unit quantities. Today, the sub \$10 cost for the 40-MHz 'C32 is available regardless of volumes. In addition to being the lowest cost floating-point processor on the market, the 'C32 offers a highly-efficient optimizing C compiler, flexible 8-/16-/32-bit memo-

ry interface, and up to 60 MFLOPS performance, making it a powerful platform for embedded designs.

TI is committed to maintaining the ease-of-use and low-cost advantage for which its floating-point processors are known. TI's extensive value-added third-party network offers unmatched support of hardware, software, and tools for the TMS320 family.

TI created the floating-point DSP market 10 years ago with the intro-

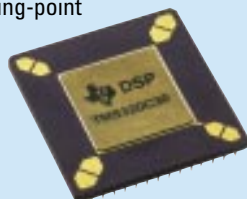
duction of the first floating-point device, the TMS320C30. The debut of the 'C30 floating-point DSP in 1988 marked the beginning of TI's leadership in the floating-point market. Today, that leadership continues with the TMS320C3x and TMS320C4x representing the largest floating-point DSP base in the world. TI extends its performance leadership in floating-point with the new 'C67x core. For more information on TI's floating-point products, visit www.ti.com/sc/details51

TMS320C32 key features

- Lowest cost floating-point processor on the market
- Fast time-to-market
- Easy-to-use development environment
- Up to 60-MFLOPS performance
- Flexible memory interface—8-/16-/32-bit

Celebrating 10 years of floating-point DSP excellence

'C30—First dual-bus architecture and TI's first floating-point DSP



1988

1990

'C40—First multi-processor support of any DSP; First chip designed specifically for parallel DSP applications



1993

'LC31—First low-power 32-bit DSP



1994

'C44—First multiprocessing-focused DSP under \$100



1994

New TMS320 applications make DSP development easier

Two new applications for the TMS320 floating-point family of processors are available today. The Logarithmic Differential Compression and Sliding Fast Fourier Transform evolve two new DSP concepts as tools for enabling tomorrow's power-intensive innovations.

Logarithmic Differential Compression (LDC)

A simple method of compressing audio signals is now available for the TMS320 floating-point processors which exhibits very little processor overhead for impressive audio quality.

LDC dramatically enhances the quality per bit of audio, video, and other natural signals by differentially encoding signals using a short floating-point format.

The bit trade-off for precision and quality exhibits a surprisingly high quality for the number of bits used. This effect occurs since floating-point representations are logarithmic by nature, which happens to match closely to how humans perceive sight and sound.

Playback of high-quality audio is possible using only 8 bits, but additional bits will greatly improve the quality. In this case, the US \$9.95 'C32, which is capable of external 16-bit

short float formats, becomes very cost and performance effective.

In addition to being a simple compressor and decompressor, LDC is also a linear process. This allows an LDC data stream to be filtered, processed, or further compressed by more traditional methods.

A patent application has been filed covering LDC as a new technology.

Sliding Fast Fourier Transform (SFFT)

The SFFT is a continuous time Fourier Transform which differentiates itself from block transform operations like the Discrete and Fast Fourier Transform (DFT) and (FFT). The SFFT requires only the frequency bins of interest to be calculated, making it particularly useful for narrow-band filtering, analysis, modulation, and demodulation, or when phase information is important.

SFFT applications include:

- Continuous time spectral analysis
- Narrow band filter banks
- Hilbert transforms
- Synchronous modulation and demodulation
- Constant phase filters

DSP beginners and veterans will also find that SFFT derivation leads

to the DFT, without using a rigorous DSP math approach. This may help in understanding where a Fourier Transform can be applied in an application.

The SFFT computes the frequency response of a signal, which is the summation of a series of impulses, from the response of individual impulses. Since the response of each impulse within a signal is simple, with each impulse having a flat response across all frequencies, it is also a simple process to sum the responses in the frequency domain.

Long standing problems concerning the stability of each frequency bin, non-rectangular windowing functions, and signal reconstruction have also been solved. The forward and reverse transform including a non-rectangular window, performed as a convolution in frequency, takes only 6 cycles per frequency bin of interest to calculate. Also, the SFFT can easily be distributed among multiple processors without requiring any external memory.

For more information

Please fill out the enclosed reply card if you would like an expanded explanation of the benefits and features of these applications. Demonstration code for both can be found at www.ti.com/sc/details51

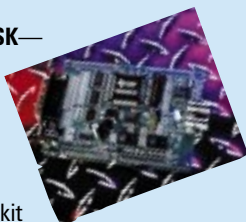
Excellence (1988–1998)

'C32—First floating-point DSP under US \$10 in quantities of 250,000



1996

'C3x DSK—First floating-point DSP starter kit



1997

'C67x core—World's most powerful floating-point CPU core at 1 GFLOPS



1998

'C32—Lowest cost floating-point DSP for US \$9.95 in any quantity



Look for more floating-point announcements in the coming months.

TI's 'C54x family extends reach from low cost to high performance

'C541 now available for less than US \$10

TI is making history with the 'C54x family of DSPs, now being offered at sub US \$10 for the first time.

MIPS	VOLUME	PRICE
'C541-40	1k units	US \$9.75
'C541-40	25k units	US \$8.36
'C541-50	25k units	US \$8.95

The 'C541 is available for less than US \$10 for 40 or 50 MIPS at quantities of 25,000 units, and below US \$11 for 66 MIPS at quantities of 25,000 units. Designed to maximize performance while enabling low-power implementation of a wide variety of telecom and telephony algorithms, the sub US \$10 'C541 is priced to win the attention of designers.

Features include:

- 15-/20-/25-ns instruction cycles
- 28K 16-bit words of ROM
- 5K 16-bit words of RAM

- two synchronous serial ports
- low active-mode power dissipation
- 100-pin TQFP package

The combination of sub US \$10 pricing and powerful features makes this highly-integrated 'C541 DSP an ideal choice for use in internet telephony applications like IP phones and wireless communications applications such as digital cellular phones, pagers, personal digital assistants, and wireless modems. For more information please fill out the enclosed reply card or visit www.ti.com/sc/details51

Experience power-efficient performance with 100-MIPS 'C549

TI's TMS320C549 is meeting the need for power efficient performance in the demanding telecommunications market.

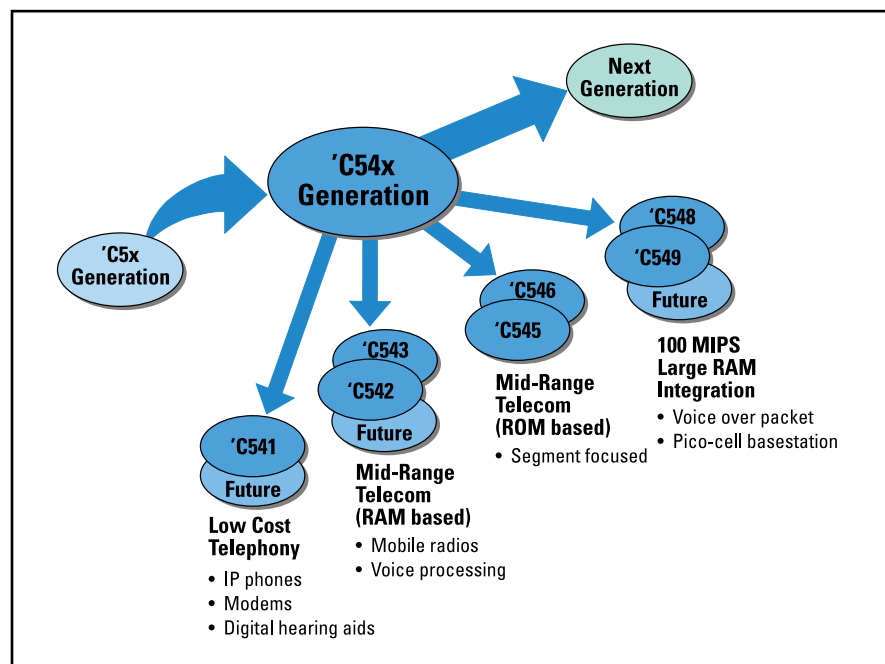
Today, TI is shipping 100-MIPS 'C549 samples with full qualification for all speeds (60/80/100 MIPS) planned for 3Q98. In addition to the 100 MIPS of high performance, the 'C549 offers extremely low power dissipation, ultra small packaging, 32K words of on-chip SRAM, and low cost (US \$25 for quantities of 10,000 units). All of these features make the 'C549 a powerful choice for manufacturers of high-performance telecommunications end equipment.

'C549 architecture offers efficient MIPS

According to independent industry reports, the 'C549 has some of the

most efficient MIPS of any fixed-point DSP offered in the industry today. The

MIPS efficiency is equivalent to that of a 24-bit DSP, but without the



extra cost of interfacing to 24-bit memories. The 'C549 architecture enables other tasks, traditionally handled by ASICs or microcontrollers, to be integrated onto the DSP, thus lowering overall system cost.

The combination of an enhanced Harvard architecture, parallel bus structure, and optimized core empowers a sophisticated instruction set. The set utilizes many single-cycle and parallel instructions.

Low dissipation minimizes power consumption

The 'C549 DSPs dissipate only 0.45 mA/MIPS for their core supply. Therefore, a 100-MIPS 'C549 operating at 2.5 volts would dissipate less than 115 mW using on-chip resources. The 'C549 has three power-down modes: IDLE1, IDLE2, and IDLE3. These three power-down modes enable the power dissipation to be reduced much further than the active power. For instance, in IDLE3 power down mode, the 'C549 has a current draw of less than 1 μ A.

Ultra small packaging enables increased density

The 'C549 is available in two configurations, the Thin Quad Flat Pack (TQFP) and the ultra-small microStar BGA™ package. The TQFP measures $20 \times 20 \times 1.4$ mm (see chip on left in above photo). It is offered in the same 144-pin package as the 'C542 which allows for easy migration.

The microStar BGA is smaller than a dime (see chip on right in above photo). This space-saving package measures at $12 \times 12 \times 1$ mm, thereby limiting the overall board size requirements and increasing channel density to manufacturers of end equipment.

Greater functionality though 32K on-chip RAM

The 'C549 features 32K words of on-chip RAM and 16K of ROM. This large amount of on-chip memory will enable designers to bring software functions from multiple DSPs together onto a



Turning on a dime. The 'C549 offers extremely low power dissipation, packaging smaller than a dime, 32K words of on-chip RAM, and low cost.

single chip. In addition, the 'C549 can address up to 8M words of code. With such a large address space, the 'C549 can reconfigure itself in operation to run a wide variety of software algorithms available to it off-chip, using an enormous external memory pool.

The 'C549 incorporates a host port interface (HPI), a time-division multiplexed (TDM) serial port, a timer, and two buffered serial ports (BSP). Combining two BSPs with the performance and large on-chip memory of the 'C549 allows designers of telecommunications equipment to handle multiple channels with a single DSP.

Applications

Targeted at manufacturers of high-performance telecommunications end equipment, the 'C549 is an optimum solution for applications like modems, cellular handsets, and dedicated subsystems. The 'C549 is best at performing a single specific algorithm or small sets of algorithms like those that may be present within modems or cellular phones requiring 50–100 MIPS. These types of applications demand very low power dissipation, are space-conscious, and must be low cost. Examples of applications using the 'C549 include:

Wireless Voice Communications

- ☐ Wireless local loop and PBX
- ☐ PCS/PCN equipment
- ☐ Fixed cellular
- ☐ Digital mobile radios
- ☐ Digital cordless phones

Wireline Voice Communications

- ☐ Digital loop carriers
- ☐ Voice processing boards
- ☐ Internet telephony
- ☐ Digital PBXs
- ☐ Computer telephony integration
- ☐ Voice-over-data in networking

Wireless Data Communications

- ☐ 2-way paging (narrowband PCS)
- ☐ Wireless and satellite modems
- ☐ Digital mobile radios

Wireline Data Communications

- ☐ Traditional analog modems
- ☐ Sub-rate DSL
- ☐ T1/E1 lines
- ☐ ATM/LAN networking (switches, routers, hubs)

Summary

The combination of high performance, low power, small packaging, and low cost of the 'C549 represents yet another example of TI's commitment and leadership in DSP Solutions. For more information, please complete the enclosed reply card or visit www.ti.com/sc/details51

ICASSP show salutes 50th anniversary of IEEE

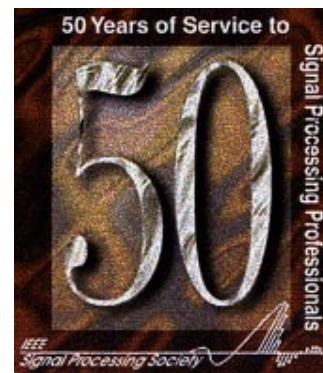
TI DSP Challenge winners showcased

The International Conference on Acoustics, Speech and Signal Processing will honor and celebrate the 50th anniversary of the Institute of Electrical and Electronic Engineers (IEEE). The conference, targeting engineers, scientists, professors, and DSP industry representatives, will be held May 12–15 at the Convention Center in Seattle, Washington. TI will be sponsoring a reception honoring IEEE's 50th anniversary. In addition, TI's CEO, Tom Engibous, will serve as keynote speaker.

The winners of the TI DSP Solutions Challenge, a worldwide competition showcasing over 270 entries from academic teams striving for \$100,000 grand prize, will be announced at the conference. University students, along with an advising professor, create and submit an original design using a TI DSP and an original software program. The professor representing the worldwide grand prize team will receive a cash prize of \$15,000 and an offer to work at TI for a six-month sabbatical program.

At the conference, judges will evaluate the designs of the top three finalists representing the three geographic regions: the Americas, Europe, and Asia. Projects are judged on their merit, creative use of DSP, education level of the team's members, and how the application can be utilized in today's marketplace. The previous winner developed a DSP-based system that restores old motion pictures at a rate 10 times faster than previous methods. Drop by the winner's presentation arena to see what tomorrow's DSP innovators have created.

Or, to learn more, visit www.ti.com/sc/details51



Educating our future. TI recently hosted University Day at Texas A&M to share ideas on the future of technology. In addition to hosting campus University Days, TI assists with engineering education by supporting the creation of DSP labs, providing teaching kits and research funding, and sponsoring design competitions. To see the many ways TI can help your university nurture the DSP innovators of the future, please fill out the enclosed reply card.

Registration opens for DSPS Fest '98

The annual meeting of TI DSP educators and third-party companies will be held August 6–8 at The Houstonian hotel in Houston, TX. The event will feature TI speakers, research paper presentations, and tailored seminars for university and third-party representatives. Members of TI's research and development division will act as symposium moderators and share their vision of the future of DSP.

Presentations at the event will include teaching workshops and product demonstrations. TI has expanded the scope of the program to be of interest to a broader group of professionals including individuals engaged in management, sales, marketing, and engineering.

If you're a TI third party or educator, register for DSPS Fest today as some seminars are limited ... www.ti.com/sc/details51

Quad codec-filter combo brings multi-channel capabilities to CO line cards

TI's latest innovation in mixed-signal technology is a highly integrated pulse-code-modulated (PCM) codec-filter combo that supports four channels on a single chip.

The device, TCM38C17 QCombo™, complements TI's existing advanced DSP-interface codec solutions in the central office (CO) switching and modem product areas. It incorporates the industry's leading idle-channel noise performance resulting from sigma-delta analog-to-digital (A/D) and digital-to-analog (D/A) signal conversion, a unique feature among today's non-programmable combos. The QCombo's architecture is expected to be reused in many future advanced codec designs from TI.

Low cost, low noise, low power

The 'C17 QCombo brings lower cost, extremely low noise, and low power consumption to a wide variety of applications that connect analog voiceband signals to digital communications systems. Among these applications are line cards, private branch exchanges, and digital telephone answering devices.

The 'C17 QCombo integrates the functionality of four TI TCM29C13 combos on a single device, lowering chip counts and reducing costs for original equipment manufacturers. The device provides increased voice and data line card capacity over the existing voiceband telecommunications infrastructure. This increased line card channel capacity is key for future voice and data transmission protocols over twisted-pair systems such as digital subscriber line (DSL).

The 'C17 QCombo typically displays transmit-channel idle channel noise of

10 dBmCO/-80 dBmOp or better. Inter-channel crosstalk, a potential concern for a multichannel codec, is typically less than -100 dB. The Qcombo gives designers the flexibility to use single-ended or differential receiver output, allowing maximum voltage swings of 8 Vpp. This eliminates the need for external amplification and allows direct connection to a transformer.

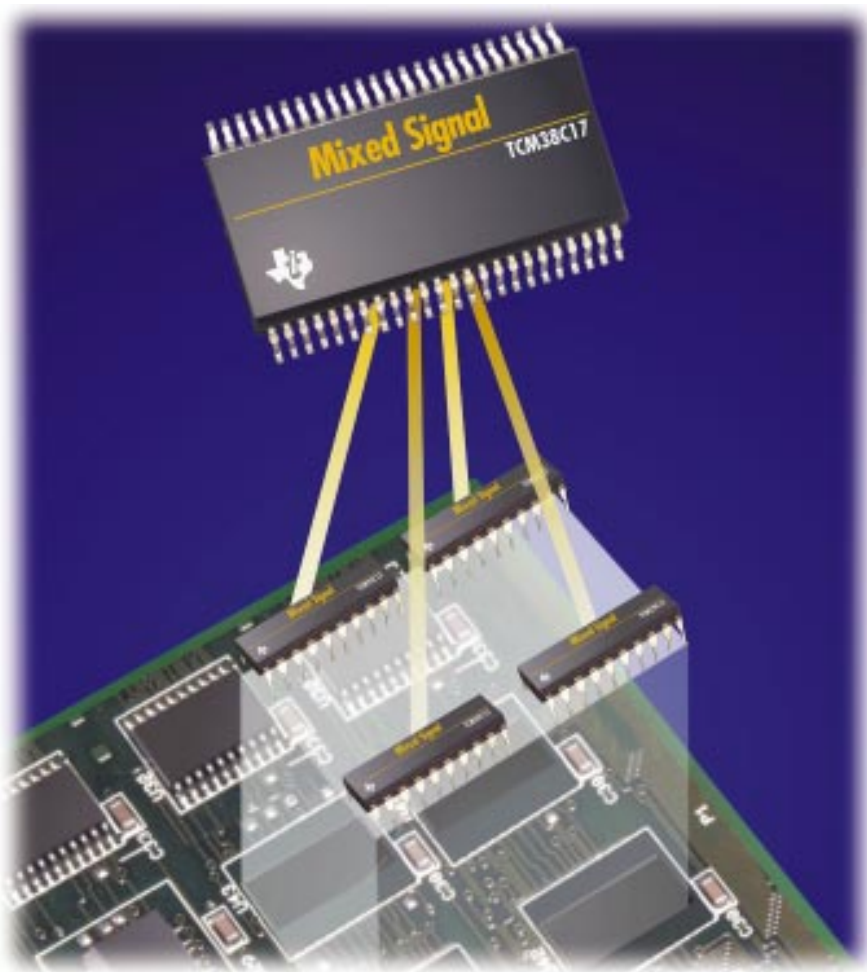
The device requires only a single-rail +5-V power supply, contributing to low-power consumption and eliminating the need for the second power supply required by first-generation

combos. A differential output drives a transformer load directly and provides an extremely wide signal swing from a single-rail codec.

ITU standards compliance

The QCombo's compliance with ITU standards assures virtually universal interoperability in line cards and other equipment with functions performed by the device.

The QCombo is now available from TI and its authorized distributors. For more information, visit www.ti.com/sc/details51



TI's 'C17 Qcombo. TI's TCM38C17 Qcombo provides multi-channel capability with negligible crosstalk, large voltage swing, and idle-channel noise.

DSP Solutions

Texas Instruments



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This section features new development and application support available through TMS320 Third Parties.

Design Studio software supports 'C67x

Hyperception Inc., an innovator in visual design software for DSPs, now supports TI's 'C67x floating-point device with its Object Oriented Real-Time Visual Language (OORVL) DSP Design Studio software. OORVL DSP Design Studio makes efficient use of the 'C67x processor by offering direct-to-DSP-chip graphical programming. The graphical compiler streamlines the algorithm design and test process by eliminating the source code creation and debug steps. The combination of DSP speed and graphical programming software lowers the technical barriers associated with DSP applications. It enables development of prototype systems in a matter of minutes, leaving engineers to focus on developing application-specific algorithms. The OORVL DSP Design Studio Standard Edition is priced at US \$1,495 and will be available April 4, 1998. Discounted sites are available.

Hyperception

- Phone: (214) 343-8525
- e-mail: info@hyperception.com
- www.hyperception.com

New vocoders for 'C54x

DSP Software Engineering, Inc. (DSPSE) recently introduced its three vocoder software component products for the TI TMS320C54x processor series. These new vocoders have numerous applications in products that require high-quality speech coding with low delay at 16 kbps, including video conferencing, digital telephony, and multimedia products.

DSPSE designed the G.728 vocoders to work easily as re-entrant, C-callable functions. G.728, also called LD-CELP (Low Delay-Code Excited Linear Prediction), is a bit exact implementation of ITU G.728 for the TMS320C54x. It provides near-toll-quality performance under clean channel conditions, and is a robust coder

providing excellent performance in tandem applications and in the presence of random bit errors. Both source and object licenses for the G.728 vocoders are now available for the price of US \$50,000 each. Versions of G.728 are also available on TI's 'C3x and 'C5x processors.

Another set of vocoders, the ITU G.729 and ITU G.729A, work easily as C-callable functions. DSPSE's G.729A, also called CS-ACELP (Conjugate-Structure Algebraic Code Excited Linear Prediction), is a bit exact implementation of ITU G.729 and G.729A for the TMS320C54x. The data between G.729 and G.729A is interchangeable, allowing G.729A to decode a G.729 packet.

DSP Software Engineering

- Phone: (781) 275-3733
- e-mail: info@dspse.com
- www.dspse.com

HotHaus algorithms for 'C54x applications

HotHaus Technologies has introduced a wide variety of telecommunications algorithms for TI's 'C54x applications, including voice and data over network, multi-function feature phones, wireless local loop, computer telephony, and more. The suite features general telephony algorithms, such as DTMF detection/generation, call progress tone monitoring, line echo cancellation; fax and data modem algorithms (T.30, V.27ter, V.29, V.17, V.22bis, and V.32bis); and G.726, G.723.1, and HotHaus-CELP speech compression algorithms. All of the algorithms operate within HotHaus' HausWare multi-channel, multi-tasking, object-oriented, DSP software framework to ease DSP system engineering. Additional vocoders and modems will be available soon.

HotHaus Technologies

- Phone: (604) 278-4300
- e-mail: info@hothaus.com
- www.hothaus.com

New 'C24x-based power module

Technosoft SA has released the new power module ACPM750E comprising a three-phase inverter with insulated gate bipolar transistors (IGBTs) for the control of AC induction motors, brushless AC servo motors, or switched reluctance motors. The output voltage is 220 V and the nominal output current is 5 A with 15 A in peak.

The ACPM750E measurement system offers galvanic isolated feedback signals for motor phase currents and DC circuit voltage and all the protections required in motor control applications.

This new power module is directly compatible with both MCK240 and the IMMC240 boards. The combination of the MCK240 and the ACPM750E allows fast motor control system prototype and debugging of the application.

Once the application and the DSP algorithms are running you can go into production by using the optimized IMMC240 controller board associated with the ACPM750E module. The price of the ACPM750E is US \$1500.



Technosoft SA

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- www.technosoft.ch

'C2000/C5x modem software

AlgoTron has unveiled DSP software solutions using TI TMS320C2x, 'C2000, and 'C5x families of processors for the data pump functions of several ITU telephone modem standards. The software supports ITU modem standards, including R.38, CV.17, V.21, V.22, V.23, V.26, V.27, V.29, and V.32. V.34 will also be available soon. The software has been developed for excellent performance and implementation efficiency. It operates at near optimum

capacity in the presence of noise, when the telephone channel is poor, and usage of the DSP processor is low in terms of MIPS, program, and data memory.

AlgoTron Ltd.

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- www.algotron.demon.co.uk

Spectrum 'C32-based ISA processor board

Available now, Indy is a two-thirds length IBM PC-AT™-compatible card based on TI's TMS320C32 floating-point processor.

With its flexible memory, DSP, and I/O configurability, Indy can be tailored for different control applications and cost requirements.



It also provides real-time DSP processing for embedded control applications such as data acquisition, motion control, and instrumentation for both OEM and research applications.

Key features include a 40- or 50-MHz 'C32, 16-bit ISA bus interface, Comprehensive tech support, Mezzanine I/O site for Spectrum or custom I/O, DSP~LINK3™ secondary bus, embedded stand-alone configurations, and up to 1 MB 0-wait-state memory.

Software support includes tools such as debuggers, and DSP operating systems. Software development includes DSP libraries and application development products such as Matlab.

Indy has an unbeatable price/performance ratio for a high-density single-board control solution. It is compatible with industry standard environments and supported by more than 130 IndustryPack™ I/O modules.

The Indy is available today in single units for US \$500 to \$1000, depending on memory configuration. OEM pricing is available.

Spectrum Signal Processing

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HOT NEWS

TI leads the digital age of electronics with strategic acquisitions and alliances

Since November 1997, TI has acquired five innovative companies, thus better positioning itself to offer DSP Solutions to a variety of markets.

Spectron Microsystems

TI acquired Spectron, a wholly-owned subsidiary of Dialogic Corp. that develops and markets advanced system software, such as real-time operating systems for use in DSP applications. The company is a leader in products that ease software development and eliminate low-level programming tasks. With this transaction, TI extends its leadership position in DSP Solutions by offering the most complete software development environment and simplifying the DSP development process.

Amati Communications Corp.

The strategic acquisition of Amati will enable TI to strengthen its role in providing DSP Solutions for high-speed internet connectivity. Amati is a world leader in Digital Subscriber Line (xDSL) technology which allows ordinary phone lines to transmit data up to 200 times faster than today's typical analog voiceband modems.

The acquisition broadens the cooperative relationship to build an xDSL chipset using TI's TMS320C6x core technology and precision MSP components as well as Amati's discrete multi-tone technology software. The chipset will be the industry's first fully software-programmable xDSL solution. It will enable customers to upgrade their modems through a software download as new standards become available.

GO DSP Corp.

TI has announced its plans to acquire GO DSP. As a leading provider of fully integrated, advanced DSP software tools, GO DSP allows system developers to improve productivity and reduce time to market. GO DSP products include Code Composer™ and Code Explorer™. The company also owns the only fully integrated programming environment with a graphical user interface. This technology complements TI's strong DSP performance and extends its ease-of-use advantage. The integration of the two companies allows TI to develop a substantial lead in establishing a framework for building software applications for DSPs.

Continued on page 12

Acquisitions

Continued from page 11

Westell Technologies, Inc.

TI and Westell have formed a strategic alliance that will accelerate the development and deployment of TI's DSP-based xDSL technologies with Westell's DSL Systems. This alliance

will provide Westell early access to leading TI DSP technologies. The results of these efforts are expected to provide mass volume deployment of broadband multimedia services such as high-speed internet access and work-at-home and real-time video communications. The combination of TI and Westell capabilities will accelerate the emerging industry with cost-effective standard compliant systems.

TMS320 DEVELOPMENT TOOLS

Device	Development Tool	Platform	Current Rev Level
TMS320C1x	Simulator	PC	2.00
TMS320C1x	EVM	PC	1.00
TMS320C2x/C2000/C5x	COMP/ASM/LNK	PC/SPARC™	6.60
TMS320 Fixed-pt	ASM/LNK ('C1x/2x/2000/5x)	PC	6.60
TMS320C2x	Simulator	PC/SPARC	3.00
TMS320C2x	EVM	PC	6.40
TMS320C2000	Simulator	PC/SPARC	1.30
TMS320C2000	XDS510/EPK	PC/SPARC	1.00
TMS320C3x/C4x	COMP/ASM/LNK	PC/SPARC	5.00
TMS320C3x/C4x	ASM/LNK	PC	5.00
TMS320C3x	Simulator	PC/SPARC	2.20
TMS320C3x	XDS510/EPK	PC/SPARC	5.20
TMS320C30	EVM	PC	5.20
TMS320C4x	Simulator	PC/SPARC	1.30/1.31
TMS320C4x	XDS510/EPK	PC/SPARC	2.50
TMS320C5x	XDS510/EPK	PC/SPARC	7.40
TMS320C5x	EVM	PC	7.20
TMS320C5x	Simulator	PC/SPARC	1.30
TMS320C54x	COMP/ASM/LNK	PC/SPARC/HP 9000	1.20
TMS320C54x	ASM/LNK	PC	1.20
TMS320C54x	XDS510	PC/SPARC/HP 9000	1.70
TMS320C54x	Simulator	PC/SPARC/HP 9000	2.20
TMS320C54x	EVM	PC	1.30
TMS320C6x	COMP/ASM/LNK	PC/SPARC	2.00
TMS320C6x	Simulator	PC/SPARC	2.00
TMS320C6x	XDS510	PC	2.00
TMS320C8x	COMP/ASM/LNK/SIM	PC/SPARC	2.00
TMS320C8x	XDS510/EPK	PC/SPARC	2.00

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