

F206 device flash Terminology

- **Flash memory array** - *Physical addressable memory within flash core*
- **Flash Module** - *Flash core and interface circuit (Wrapper)*
- **Flash Core** - *Memory Arrays, I/O buffers, read and program data path and associated control logic*
- **Flash segment** - *Contiguous blocks of memory cells which, when added together, create the memory array*
- **Wrapper** - *Interface circuitry between Flash core and cDSP*
- **Charge pump** - *Voltage generators and associated control logic*

Flash Memory Features

Flash array Organization : Flash0 16k word - 0000h -3FFFFh
Flash1 16k word - 4000h -7FFFFh

Power supply : 5v only(4.9v to 5.10v)

Erase segment size : 8 segments maximum
2k byte minimum segment size

Access time : 1clock cycle

Instruction time : 50ns

Memory functions : Read/ Erase/ Program/ controlled by cDSP core

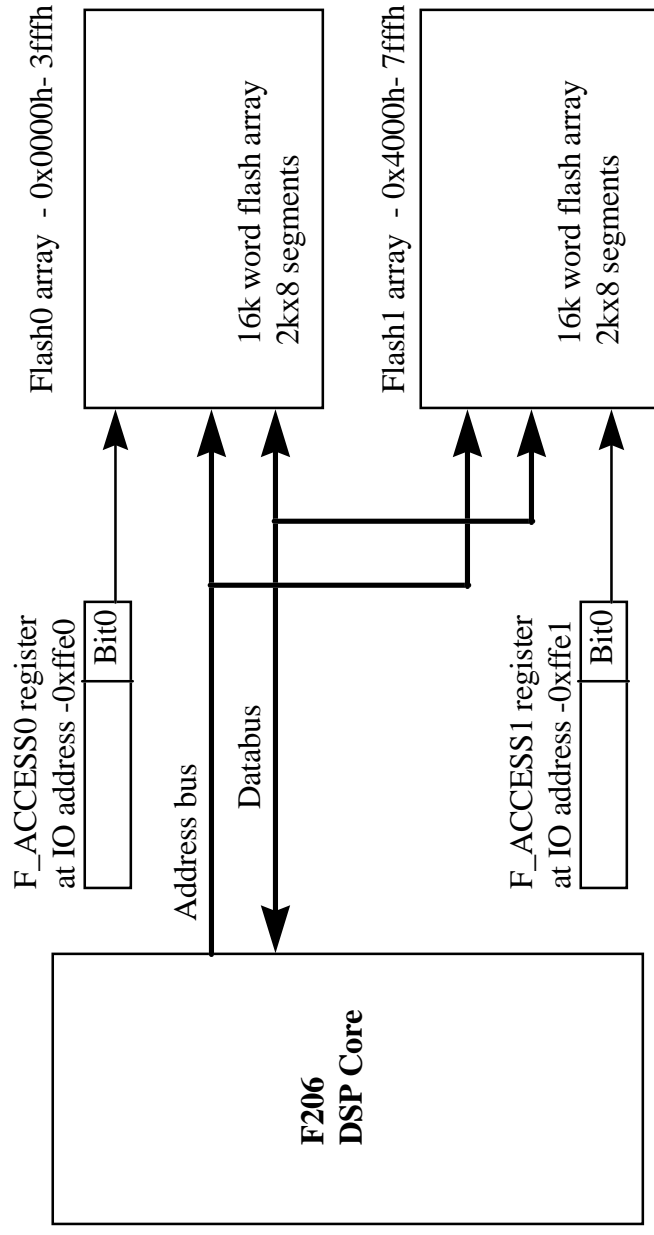
Algorithm length : 1K words of DSP code
(Clear, Erase, Writing)

Flash Programming Sequence

Stages of Flash bit programming

1. **Clearing**
 - Write 0 in all bits
2. **Erasing**
 - Write 1 in all bits
3. **Write/Coding**
 - Write 0 in selected bits

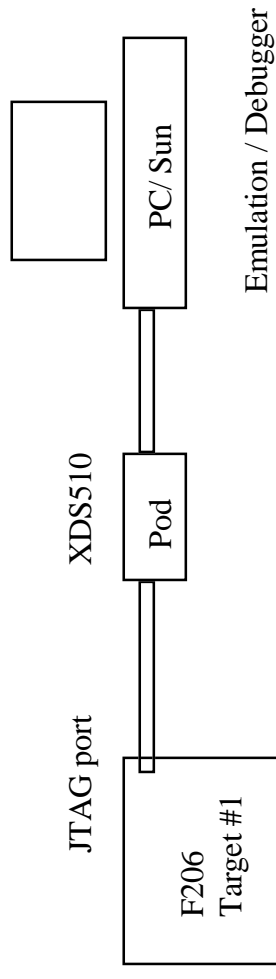
32kx16 Flash Array control logic



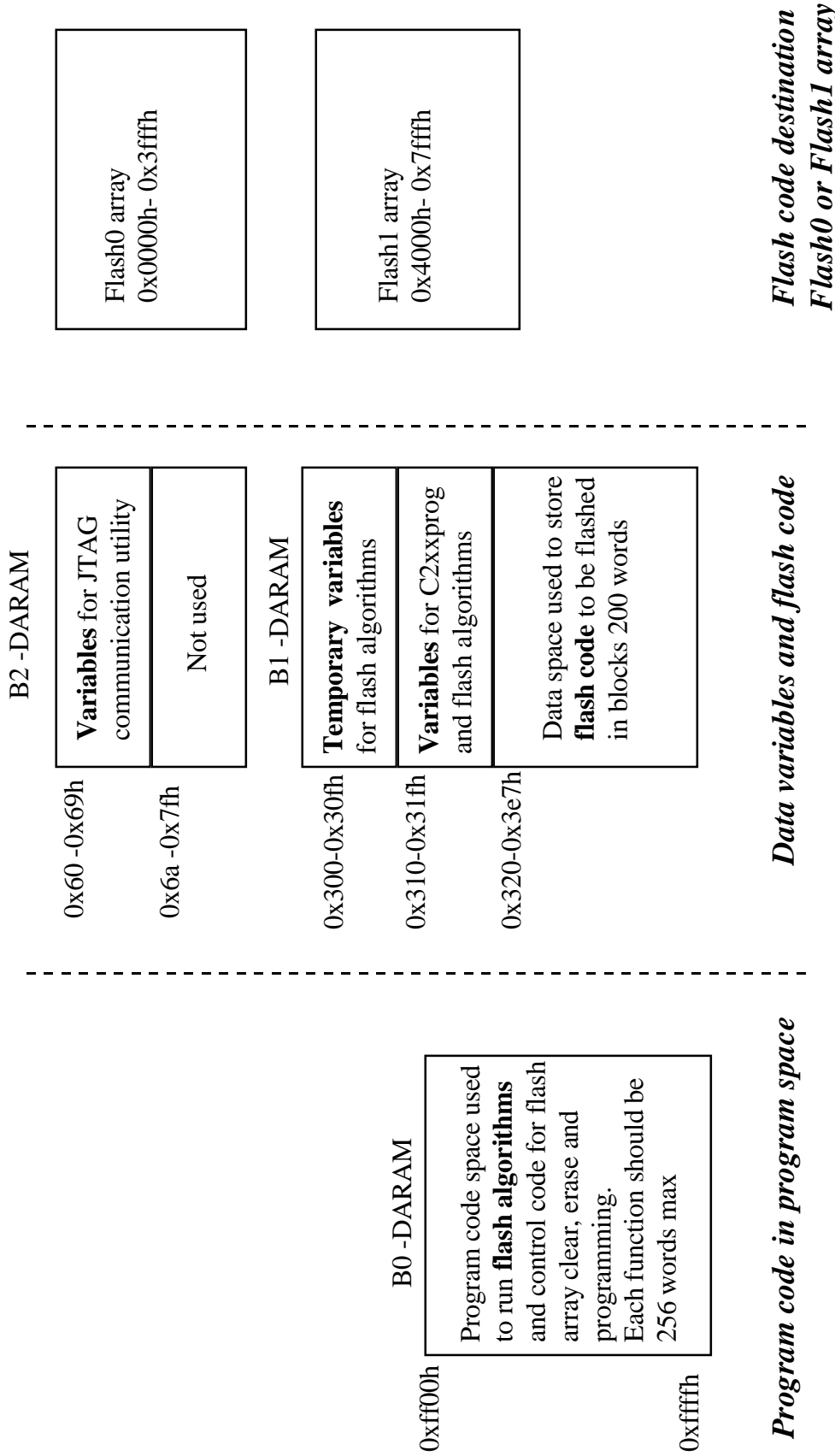
F_ACCESS register control functions

Bit0	Flash Mode	Function	Reset value
1	Array mode	Normal memory access	1
0	Register mode	Flash array programming	

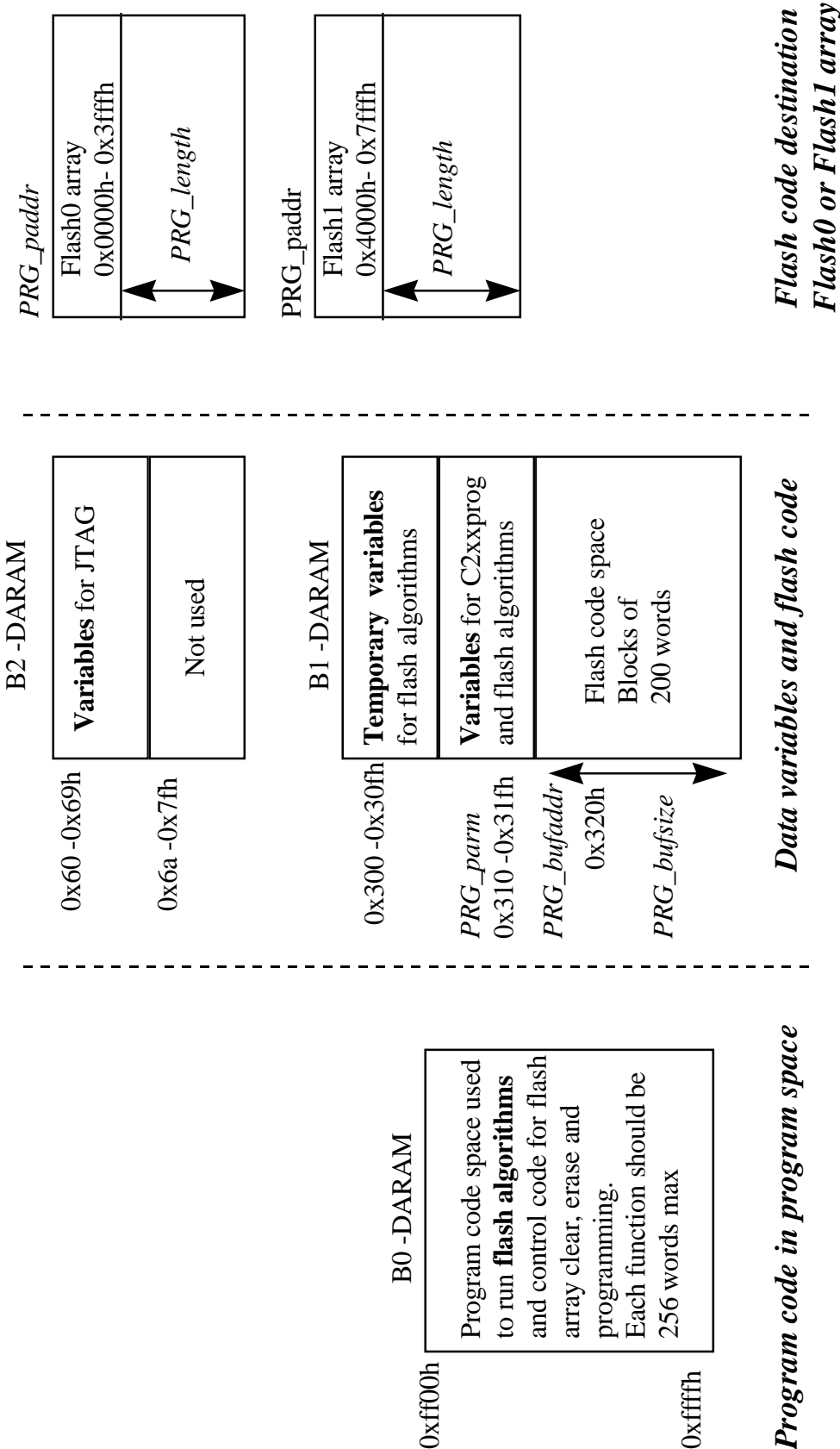
On_chip Flash programming interface



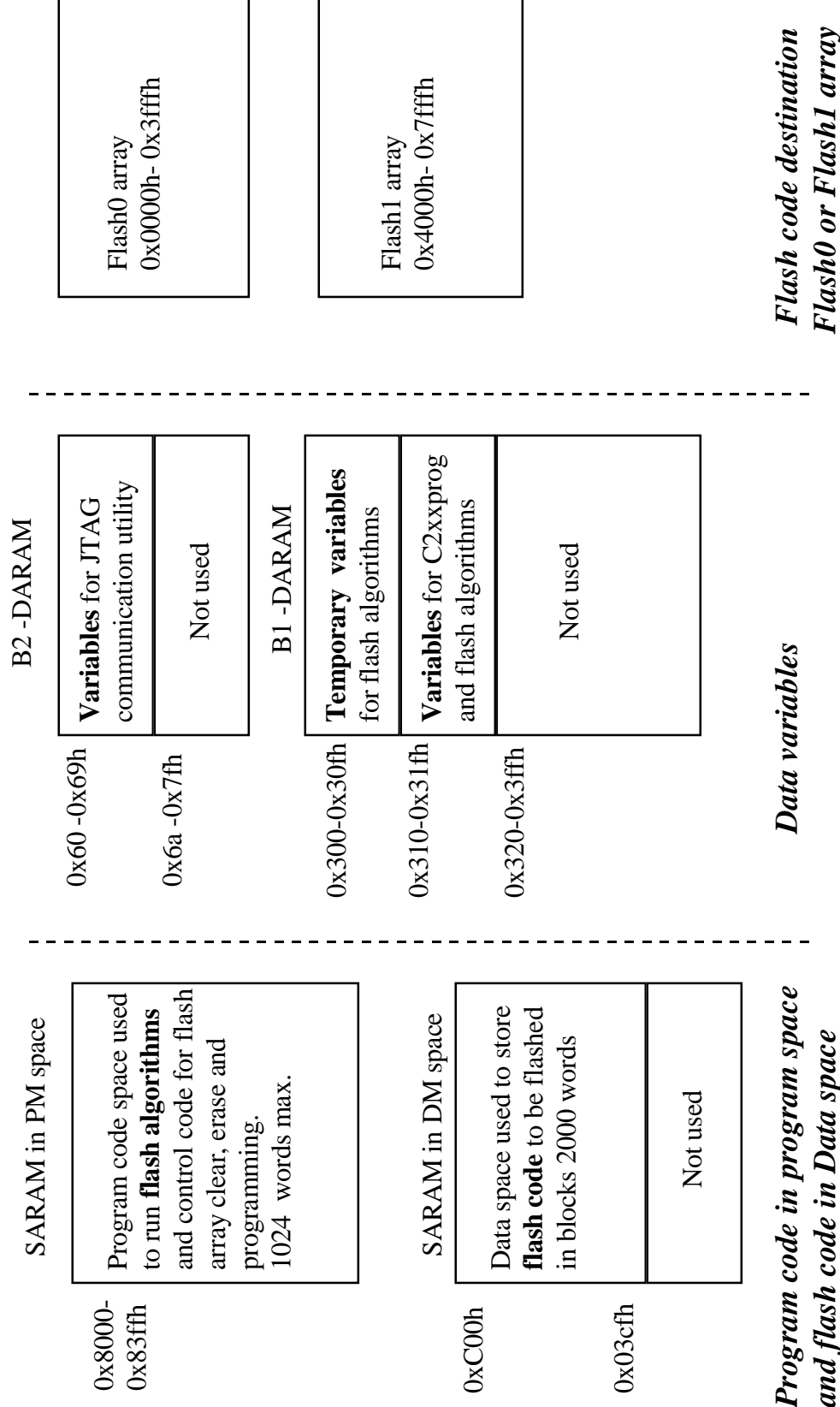
B0 - Memory map used for Flash programming using JTAG loader PRG2XXW.EXE



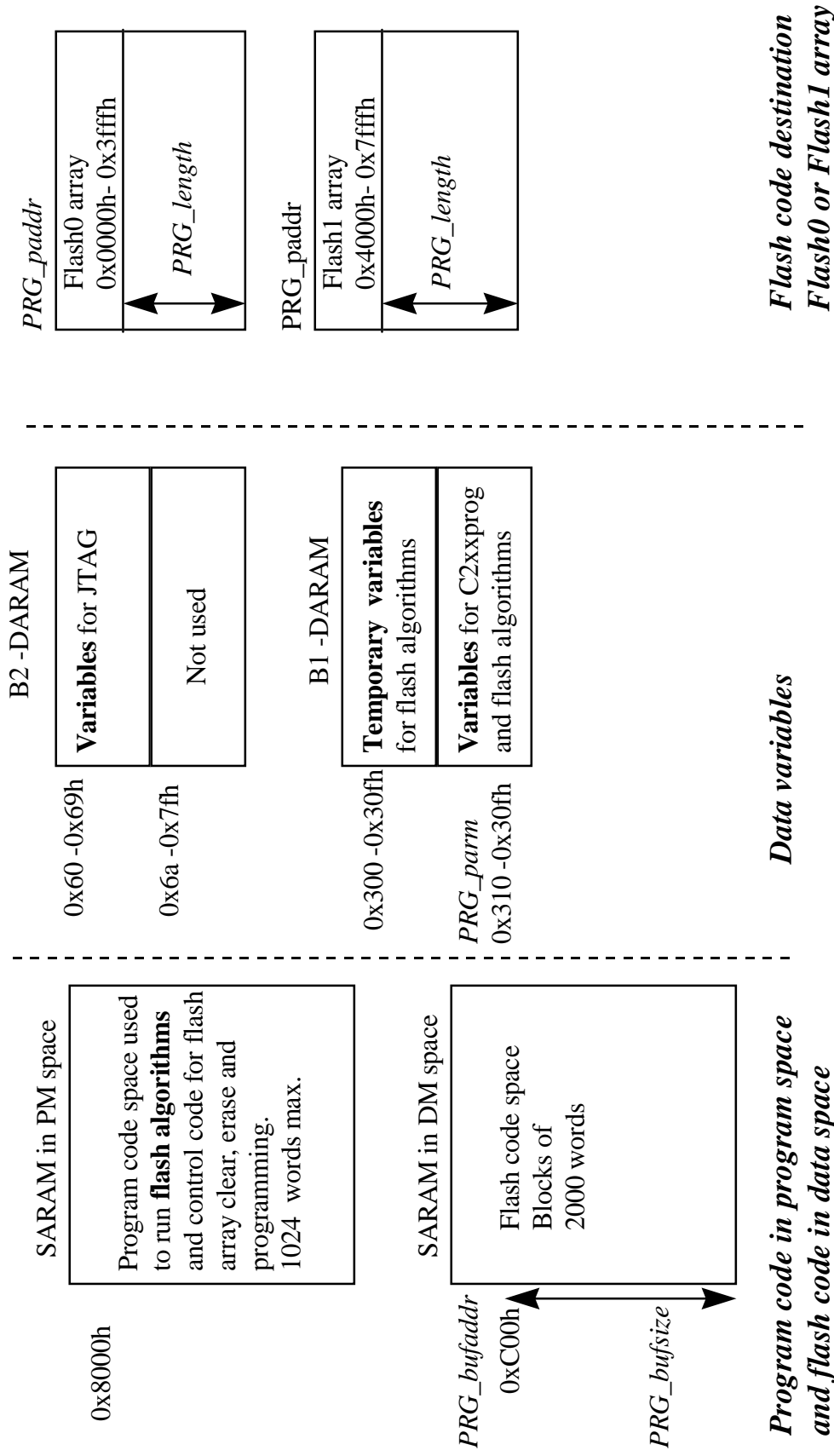
B0 Memory variables and functions used in Flash programming using JTAG loader PRG2XXW.EXE



SARAM - Memory map used for Flash programming using



SARAM Memory variables and functions used in Flash programming using JTAG loader PRG2XXW.EXE



Flash array variables used by Flash algorithms and JTAG loader

B2 -DARAM

0x60 -0x69h	Variables for JTAG
0x6a -0x7fh	Not used

B1 -DARAM

0x300 -0x30fh	Temporary variables for flash algorithms
PRG_parm 0x310 -0x30fh	Variables for C2xxprog and flash algorithms

PRG_parm at 0x310 -0x30fh	

0x0310h - PRG_bufaddr	- Used by JTAG loader
0x0311h - PRG_bufsize	- Used by JTAG loader
0x0312h - PRG_devsize	- Used by JTAG loader
0x0313h - PRG_paddr	- Defined and used by JTAG loader
0x0314h - PRG_page	- Reserved
0x0315h - PRG_length	- Defined and used by JTAG loader
0x0316h - PRG_status	- Used by JTAG loader

0x0317h - Temp	- Reserved
0x0318h - PROTECT	- Segment protect used by algorithms
0x0319h - FL_ST	- Segment start address used by algorithms
0x031ah - FL_END	- Segment end address used by algorithms
0x031bh - FL_LEN	- Segment length used by algorithms
0x0310ch - PRG_END	- Reserved

Flash control registers in register mode

Control Registers	Address	Description
SEG_CTR	0	Segment control register. The most significant 8- bits enable specific segments for erasure or programming. Setting a bit to 1 enables the segment. The least significant bits control the program, erase and verify operations of the segments
TST	1	Reserved for test.
WADRS	2	Write address. Holds address during write operation
WDATA	3	Write data. Hold data during write operation

Segment control register SEG_CTR

<i>Name</i>	<i>Bit address</i>	<i>Active</i>	<i>Description</i>
EXE	0	1	Execute. This bit initiates and ends programming and erasing of the flash array. EXE and KEY 0/1 bits must be written in the same write access. This protocol is to be followed for programming to occur. After the required programming time the EXE bit should be cleared in the same write as KEY0/1 bits. The data and address latches are locked whenever the EXE bit is set and all attempts to read from or write to the array will be ignored.
ERASE	1	1	Initiates erasure setup. Set this bit to perform the erase operation. The ERASE bit must be set prior to setting EXE bit.
WRITE	2	1	Enable write logic. Set this bit to perform a write operation. The WRITE bit must be set prior to setting EXE bit.
VER1	3	1	Verify 1 mode. Proper erasure and programming levels are achieved by monitoring these bits
VER0	4	1	Verify 0 mode
KEY0 KEY1	5 6	0 1	Execute key bits .These bits must be written as 01 in the same access as EXE bit for EXE operation to start. These bits are used as additional protection against inadvertent programming or erasure of the flash. These bits are read as zeros.
BUSY	7		Reserved
SEG7-0	15-8	1	Segment enable bits. Each segment enable bit individually protects or enables write and erase operation for each of the segments in the flash array. Bit 8 controls segment 0 and bit 15 controls the segment 7 of the flash array

16k word Flash core interface

