SONY

CX20133

Dual 16 bit 44 kHz Multiplexed D/A Converter

Description
The CX20133 is a 16 bit D/A converter IC for PCM audio using the integrating formula. Analog signal is reproduced from the 16 bit digital signal by combining an integrator, analog switch and low-pass filter to the IC exterior. Following circuits are also built-in.

- Integrating current output
- Two channels of discharge signal output
- Level shifting for interface direct with TTL/MOS LSIs.
- Analog switch drive.

Features
- Miniature flat package requires only small mounting area.
- Conversion frequency of 44.1 kHz.
- Serial data input.
- Low distortion factor typically at 0.003%.

Structure
- Bipolar Silicon Monolithic IC

Absolute Maximum Ratings (Ta = 25°C)
- Supply voltage \( V_{CC} \) to \( V_{EE} \) 12 V
- Operating temperature \( T_{opr} \) -10 to +75 °C
- Storage temperature \( T_{stg} \) -50 to +125 °C
- Allowable power dissipation \( P_{D} \) 1.1 W

Recommended Operating Conditions
- Supply voltage \( V_{CC} \) 5 ± 0.25 V
  \( V_{EE} \) -5 ± 0.25 V
Fig. 1
## Pin Description

<table>
<thead>
<tr>
<th>No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DVEE</td>
<td>Power supply pin for the digital circuit. Applied with $-5 \text{ V}$.</td>
</tr>
<tr>
<td>2</td>
<td>SUB</td>
<td>IC substrate. Always connected to 1 pin.</td>
</tr>
<tr>
<td>3</td>
<td>TEST 1</td>
<td>Test pin, normally open.</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>Power supply pin for the digital circuit. Applied with $+5 \text{ V}$.</td>
</tr>
<tr>
<td>5</td>
<td>TEST 2</td>
<td>Test pin, normally open.</td>
</tr>
<tr>
<td>6</td>
<td>LATCH</td>
<td>Clock pin of D-type clutch.</td>
</tr>
<tr>
<td>7</td>
<td>LRCK</td>
<td>LRCK input pin.</td>
</tr>
<tr>
<td>8</td>
<td>WCLK</td>
<td>WCLK input pin.</td>
</tr>
<tr>
<td>9</td>
<td>BCLK</td>
<td>BCLK input pin.</td>
</tr>
<tr>
<td>10</td>
<td>DIN</td>
<td>DIN (data input pin).</td>
</tr>
<tr>
<td>11</td>
<td>LRCK OUT</td>
<td>LRCK output pin.</td>
</tr>
<tr>
<td>12</td>
<td>CC</td>
<td>CC input pin.</td>
</tr>
<tr>
<td>13</td>
<td>DGND</td>
<td>Ground pin for the digital circuit.</td>
</tr>
<tr>
<td>14</td>
<td>DVEE</td>
<td>Power supply pin for the digital circuit. Applied with $-5 \text{ V}$.</td>
</tr>
<tr>
<td>15</td>
<td>DCR</td>
<td>Output pin of R-channel discharge driving signal.</td>
</tr>
<tr>
<td>16</td>
<td>ISET</td>
<td>Pin for setting integration current.</td>
</tr>
<tr>
<td>17</td>
<td>IOUTR</td>
<td>Output pin for R-channel current.</td>
</tr>
<tr>
<td>18</td>
<td>IOUTL</td>
<td>Output pin for L-channel current.</td>
</tr>
<tr>
<td>19</td>
<td>NC</td>
<td>No connection.</td>
</tr>
<tr>
<td>20</td>
<td>AVEE</td>
<td>Power supply pin for the analog circuit.</td>
</tr>
<tr>
<td>21</td>
<td>AGND</td>
<td>Ground pin for the analog circuit.</td>
</tr>
<tr>
<td>22</td>
<td>DGND</td>
<td>Ground pin for the digital circuit.</td>
</tr>
<tr>
<td>23</td>
<td>DCL</td>
<td>Output pin for L-channel discharge driving signal.</td>
</tr>
<tr>
<td>24</td>
<td>DCBIAS</td>
<td>Bias pin for the discharge circuit.</td>
</tr>
<tr>
<td>25</td>
<td>COUT</td>
<td>Output pin for the clock oscillator.</td>
</tr>
<tr>
<td>26</td>
<td>CIN</td>
<td>Positive input pin for the clock oscillator.</td>
</tr>
<tr>
<td>27</td>
<td>CIN</td>
<td>Negative input pin for the clock oscillator.</td>
</tr>
<tr>
<td>28</td>
<td>DGND</td>
<td>Ground pin for the digital circuit.</td>
</tr>
</tbody>
</table>
### Electrical Characteristics

(Ta = 25°C, VEE = -5.0V, VCC = 1.0V)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit current</td>
<td>IEE</td>
<td>1, 2, 14, 20</td>
<td>-112</td>
<td>-85</td>
<td></td>
<td>mA</td>
<td>1</td>
</tr>
<tr>
<td>Circuit current</td>
<td>ICC</td>
<td>4</td>
<td>9.5</td>
<td>12.5</td>
<td></td>
<td>mA</td>
<td>1</td>
</tr>
<tr>
<td>Input threshold voltage</td>
<td>VTH</td>
<td>6, 7, 8, 9, 10, 12</td>
<td>2.1</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>VIH</td>
<td>6, 7, 8, 9, 10, 12</td>
<td>2.8</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>VIL</td>
<td>6, 7, 8, 9, 10, 12</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High-level input current</td>
<td>IHI</td>
<td>6, 7, 8, 9, 10, 12</td>
<td>500</td>
<td></td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Low-level input current</td>
<td>ILI</td>
<td>6, 7, 8, 9, 10, 12</td>
<td>500</td>
<td></td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>VLRCKH</td>
<td>1 Pin 7 = 4.5V IOH = -100μA</td>
<td>2.7</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>VLRCKL</td>
<td>1 Pin 7 = 0V IOI = 100μA</td>
<td>-2.7</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Clock input bias voltage</td>
<td>VCIIN</td>
<td>26, 27</td>
<td>-1.3</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Clock high-level output voltage</td>
<td>VCCR</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Clock low-level output voltage</td>
<td>VCOL</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Current output pin leak</td>
<td>I0</td>
<td>17, 18</td>
<td>1.5</td>
<td></td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IOUT output current</td>
<td>IOUT</td>
<td>17, 18</td>
<td>2.008</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Current ratio*1</td>
<td>I0/I0</td>
<td>17, 18</td>
<td>255.0</td>
<td>256.0</td>
<td>257.5</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Discharge circuit current dissipation</td>
<td>IDC</td>
<td>24</td>
<td>1.35</td>
<td>1.9</td>
<td>2.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Discharge circuit high-level output voltage</td>
<td>VDCOH</td>
<td>15, 23</td>
<td>0.27</td>
<td>0.45</td>
<td>0.77</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Discharge circuit low-level output voltage</td>
<td>VDCOL</td>
<td>15, 23</td>
<td>-4.2</td>
<td>-3.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum ISET current</td>
<td>ISET</td>
<td>16 IOUT &lt;= 255 I0 &lt; I0 &lt; 257</td>
<td>575</td>
<td></td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Distortion factor</td>
<td>THD</td>
<td>Both right and left, OdB (full scale)</td>
<td>0.003</td>
<td>0.005</td>
<td>%</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Operating clock frequency</td>
<td>fCLK</td>
<td>Self-activating/Activated</td>
<td>36</td>
<td></td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1)** Ground Pins 13, 17, 18, 21, 22, 24 and 28. Connect Pin 16 via a resistor of 5.1 kΩ and keep other pins open.

**Note 2)** I0 and I0 must satisfy the relation below in the Current Ratio Test Circuit (Fig. 3):
- 3.9 (mV) < 1 (kΩ) × I0 (μA) - 256 (kΩ) × I0 (μA) < 5.9 (mV)

**Note 3)** See the Test Circuit (Fig. 2).
Conversion frequency: 44.1 kHz
Input data: Use the 16 bit full-scale data (0 dB) generated by the data generator.
Distortion meter: Use the HP339A (with all filters on) or the like provided with 80 kHz LPF, 30 kHz LPF and 400 Hz HPF.

*1 In the Current Ratio Test Circuit (Fig. 3),
- 3.9(mV) < 1(kΩ) × I0(μA) - 256(kΩ) × I0(μA) < 5.9(mV)
Description of the Conversion Operation

(1) Data call (BCLK, DIN, WCLK, LRCK). Refer to Fig. 1.

The data comes in 16 bit serial signal with 2’s compliment. The data is sent sequentially into the IC beginning from MSB in sync with the rise of the bit clock (BCLK). (The data change represents the BCLK fall).

When the word clock (WCLK) is changed from the high-level to low-level at the 17th fall of BCLK, the 16 bit data is transferred from the shift register to the latch by the fall signal.

When the CX20133 is used in the stereo mode, data from other channels are sent in from the 17th BCLK.

In the stereo mode, Rch data is called when LRCK at the low level and Lch data is called in when the LRCK is at the high level. IOUTL and DCL operate only when LRCK is at the low level and IOUTR and DCR operate only when LRCK is at the high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are input from the clock input (CIN) with conversion command at the high level, all inner timing circuits are reset.

After resetting, the inner timing circuit starts operation when a clock is input from CIN with CC at the low level. The three signal generated this way are the discharge signal, counter set signal and integrating signal. Time of these three signals is determined depending on the clock cycle and their number of quantity:

\[
\begin{align*}
CC & \\
\text{Discharge signal} & \quad t_1, t_2 \\
\text{Counter set signal} & \quad t_1, t_2 \\
\text{Integrating current start signal} & \quad t_4, t_5
\end{align*}
\]

\[
\begin{align*}
t_1 &= 34 \times \tau_0 \\
t_2 &= 67 \times \tau_0 \\
t_3 &= 31 \times \tau_0 \\
t_4 &= 65 \times \tau_0 \\
t_5 \text{ Min} &= 45 \times \tau_0 \quad \text{(input data 01 to 1)} \\
t_5 \text{ Max} &= 302 \times \tau_0 \quad \text{(input data 10 to 0)}
\end{align*}
\]

The counter set signal is to set the data input to the latch to the counter and it is not output externally.

The discharge signal is output from DCL and DCR and it is controlled by LRCK. It is output from DCL when LRCK is at the low level and from the DCR when LRCK is at the high level.

By the integrating current start signal, the upper current \(I_o\) and lower current \(I_o\) start flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, measures the 11 offsets after completion of counting and outputs a signal to stop the integrating current.

The \(t_5\) value is varied between 0 and 255 by the preset input data in the counter.

Therefore, the conversion time from the start of low CC level to the completion of integrating requires \(t_4 + t_5\) sec max.

The integrating current, like the discharge signal, is controlled by LRCK; IOUTL is output when LRCK is at the low level and IOUTR is output when LRCK is at the high level.
The Relation between Sampling Frequency $f_s$ and Clock

The maximum and minimum values of the integration voltage output, $V_o\text{ Max}$ and $V_o\text{ Min}$, are expressed as follows:

$$V_o\text{ Max} = \frac{i_0}{C} \cdot \tau_0 \cdot 267 + \frac{i_0}{C} \cdot \tau_0 \cdot 266 \quad (t_4 + t_5 \text{ Max})$$

$$V_o\text{ Min} = \frac{i_0}{C} \cdot \tau_0 \cdot 12 + \frac{i_0}{C} \cdot \tau_0 \cdot 11 \quad (t_4 + t_5 \text{ Min})$$

where $f_{CLK}$ is a clock frequency and $\tau$ is a period.

The integration voltage is held by the capacitor $C$ in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period $T$ which is given according to the settling time of the deglitching circuit.

The relation between the conversion frequency $f_s$ and the clock frequency $f_{CLK}$ is given as below assuming that the conversion time and deglitching period are equivalent:

$$f_s = \frac{f_{CLK}}{2 \times (t_4 + t_5 \text{ Max})} = \frac{f_{CLK}}{734}$$

where $f_s = 44.1 \text{ kHz}$ results in $32.4 \text{ MHz}$ of $f_{CLK}$.

It is, however, recommendable to specify $f_s$ as the follow for the practical use because a settling time of 0.5 to $1.0 \mu s$ is required for the integrator after the current for $t_5$ disappears:

$$f_s = \frac{f_{CLK}}{2(t_4 + t_5 \text{ Max} + 1.0 (\mu s)) + 1}$$

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(3) Integration current setting (ISET, IOUTL, LOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

\[
I_{\text{OUTL}}(R) = I_0 + i_0
= \left(4 + \frac{1}{64}\right) I_{\text{SET}}
\]

where \(i_0\) and \(I_0\) are integration currents corresponded to the ILSB and 2<sup>8</sup>-LSB, respectively.

If \(D_0\) and \(D_{15}\) are specified as MSB and LSB, respectively, integrator output voltage \(V_0\) is given by the following equation:

\[
V_0 = \frac{i_0}{C} \left( D_0 \cdot 2^7 + D_1 \cdot 2^7 + \ldots + D_7 \cdot 2^0 + 12 \right) \tau_0
+ \frac{i_0}{C} \left( D_8 \cdot 2^7 + D_9 \cdot 2^6 + \ldots + D_{15} \cdot 2^0 + 11 \right) \tau_0
\]

where \(I_{\text{SET}} = 500 \mu\text{A}, \tau_0 = \frac{1}{35 \text{ (MHz)}} = 28.6\) (ns) and \(C = 2000\) pF result in the maximum output voltage \(V_{0\text{ Max}}\) of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

\[
I_0 = 4 \cdot I_{\text{SET}}
\]

\[
i_0 = \frac{1}{64} \cdot I_{\text{SET}}
\]

\(V_{0\text{ Max}}\) is calculated as the follow:

\[
V_{0\text{ Max}} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} \cdot 267 \cdot 28.6 \times 10^{-9}
+ \frac{500 \cdot 10^{-6} / 64}{2000 \times 10^{-12}} \cdot 266 \cdot 28.6 \times 10^{-9}
= 7.67\) (V)

(4) Operation of LRCK OUT

The LRCK OUT is an output for the analog switch IC (equivalent to MC14053B) drive to clip the output converted by the CX20133 and integrator as a PAM wave.

A PAM wave jitter may cause a conversion error and a D-type flip-flop is incorporated to eliminate this jitter; the LATCH input is used as a clock for the flip-flop.

This D-type flip-flop changes the output status in sync with the clock rise. The LRCK OUT operates only when +5 V is applied to Vcc. The output voltage level ranges from −2.7 V to +2.7 V enough to drive the CMOS analog switch effectively.

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Timing of LATCH, LRCK and LRCKO
(5) Clock input/output pin (COUNT, CIN, CIN)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased by the internal bias circuit. The ($\approx -1.3$ V) output amplitude level is 0.8 V.

(6) Bias pin (DVEE, SUB, DGND, VCC, AVEE, AGND, DC BIAS)

SUB is used at the common potential with DVEE. A standard value for the DVEE and AVEE is $-5.0$ V.

The CX20133 is devised so that it can operate when voltage at the digital input pin has a value between either $0$ to $-5$ V or $0$ to $+5$ V. When operated with an input between $0$ and $+5$ V, $+5$ V must be applied to Vcc. In this case, LRCK OUT is output as mentioned above.

When operated with an input between $0$ to $-5$ V, Vcc must be set open.

DC BIAS is for the bias circuit of the discharge signal output circuit. Supply current of $(2.5$ mA $+\alpha)$ from a power supply of $+5$ V or above, because this pin requires approx. $2.5$ mA current as a standard value. The potential at the pin is biased at $2$ Vf.

A value $\alpha$ can be determined according to the following procedures. Approx. $0.5$ mA current is necessary to retain $2$ Vf (approx. $1.4$ V) at this pin. The maximum current that flows through the load resistor RL attached to DCR (15 Pin) and DCL (23 Pin) is calculated as the follow:

$$1/RL \times (V_{DCH} + |DVEE|)$$

The above equation results in $1.15$ V where $RL=4.7\,k\Omega$, $V_{DCH}=0.4$ V and $DVEE=-5$ V are specified. Then $\alpha$ is calculated as

$$\alpha = 0.5 + 1.15 = 1.65\, (mA),$$

and required current is then obtained as $4.15$ mA. Recommended value is $5$ mA for $RL=4.7\,k\Omega$.

Timing Chart in the Stereo Mode

![Timing Chart](image)

* When LATCH input is used as BCLK.
Application Circuit and Test Circuit

1000pF is of a polystyren capacitor.

Murata Mfg. Co. Ltd.: AFLB9W82000C5

HC-43/U (American KSS), etc.

Fig. 2
Sample/Hold Circuit for Deglitching

Current Ratio Test Circuit

1 kΩ: 16 kΩ ± 0.5%, 16 resistors connected in parallel.
256 kΩ: Above resistors connected in series.
Voltmeter: Use a 5-digit meter (4 1/2).

<table>
<thead>
<tr>
<th>LCH</th>
<th>SW1</th>
<th>SW2</th>
<th>SW3</th>
<th>SW4</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0</td>
<td>a</td>
<td>a</td>
<td>a</td>
<td>a</td>
</tr>
<tr>
<td>L0</td>
<td>b</td>
<td>b</td>
<td>b</td>
<td>b</td>
</tr>
<tr>
<td>RCH</td>
<td>L0</td>
<td>a</td>
<td>a</td>
<td>a</td>
</tr>
<tr>
<td>L0</td>
<td>b</td>
<td>b</td>
<td>b</td>
<td>b</td>
</tr>
</tbody>
</table>
**Temperature characteristics of $I_{OUT} (I_0 + I_d)$**

(R, Lch common)

- **$I_0/I_0$ vs. $I_{SET}$**
  - $T_a = 25^\circ C$
  - $V_{EE} = -5$ V

- **Output current vs. Supply voltage ($V_{EE}$)**
  - $I_{SET} = 500 \mu A$
  - $I_{OUT} = I_0 + I_d$, $1.33 \mu A/V$

- **Distortion factor**
  - $-20$ dB
  - Full scale

$V_{EE} = $ Supply voltage (V)

Frequency (Hz)