BCM1250 FEATURES

- Two 64-bit MIPS CPUs, scalable from 600 MHz–1 GHz
  - Quad-issue in order pipeline; dual execute, dual memory pipes
  - Enhanced skew pipeline enables zero load-to-use penalty
  - 32-KB instruction cache, 32-KB data cache
  - Advanced branch predictors

- Fast, on-chip multiprocessor bus
  - Connects the CPUs, L2 cache, memory controller and I/O bridges
  - Runs at half the CPU core frequency; 256 bits wide

- DDR memory controller
  - Two channels, each with a 64-bit data bus plus optional ECC
  - Runs up to 200 MHz clock rate, 400 MHz data rate
  - Support for DDR SDRAM, SGRAM, and FCRAM

- High-speed packet interfaces
  - Three 10/100/1000 Ethernet MACs; 802.3 compliant
    - Option to configure MACs into packet FIFOs
  - Up to two packet FIFOs each capable of OC-48 data rates

- PCI interface
  - 32 bits, 33/66 MHz (PCI 2.2)
  - Host bridge or target device

- HyperTransport™ (formerly LDT) I/O interface
  - Complies with HyperTransport™ standard for high-speed I/O fabric
    - 500-MHz clock rate, double data rate, for 600 MHz CPUs;
      600-MHz clock rate for 800 MHz CPUs
  - Peak bandwidth of 9.6 Gbps in each direction @ 600 MHz
  - Supports double-ended fabrics (to link two BCM1250s)

- Integrated system I/O
  - Generic I/O for direct connect to boot ROM, flash
    - Two SMBus serial configuration interfaces
    - PCMCIA control interface
    - Two serial interfaces

- Extensive, on-chip debug features

- 8–10W power dissipation @ 800 MHz

- Support for leading operating systems including VxWorks®, Linux® and NetBSD

- Evaluation board platform available with tools, firmware and software drivers

SUMMARY OF BENEFITS

- Industry-leading performance
  - Processing speed of up to 10 Mpps*
    - 128 Gbps on-chip bus bandwidth; 50 Gbps memory bandwidth, 30 Gbps total I/O bandwidth

- Low power dissipation of 8–10W (@ 800 MHz)

- High functional integration

- Programming ease and flexibility based on MIPS64 Instruction Set Architecture (ISA)

- Scalable multiprocessor chip and system architecture

- Broad tools and system software support

- For additional information on the BCM1250 evaluation boards, refer to the BCM91250A and BCM91250E product briefs

*Based on internal Broadcom benchmark, using BCM1250 for standard IPv4 L3 look-up/switching.

TARGET APPLICATIONS

Due to the BCM1250’s world-class performance, power efficiency and integration, the processor is ideal for a broad variety of applications including:

- Enterprise workgroup and backbone switches
- VPN switches/routers
- Multiservice access concentrators
- SAN routers/gateway/switches
- IP services/subscriber management platforms
- Web-server switches
- High-end firewall/intrusion detection devices
- Wireless basestations

Example: Packet Processing Blade
Broadcom’s first SiByte™ processor, the BCM1250, is a state-of-the-art multiprocessor solution targeted at the fast-growing networking and communications markets.

The BCM1250 is the first MIPS64™ processor to offer the industry-leading performance, high functional integration, and low power levels required by next-generation networking applications.

The BCM1250 is an intelligent on-chip multiprocessor system (CMP) consisting of two Broadcom SB-1 high performance MIPS64™ CPUs, a shared 512-KB L2 cache, a DDR memory controller, and integrated I/O. All major blocks of the processor are connected together via the ZBbus, a high-speed, split-transaction multiprocessor bus. The bus implements the standard MESI protocol to ensure coherency between the two CPUs, L2 cache, I/O agents, and memory. Three Gigabit Ethernet MACs (10/100/1000) enable easy interfacing to LANs. To enable higher data rates, or in cases where Ethernet protocol processing is not required, the MACs can be configured as either three 8-bit or two 16-bit packet FIFOs. The high-speed I/O is provided using HyperTransport™ (HT) I/O fabric and a 32-bit PCI (rev 2.2) local bus. Two serial ports are available to use as UARTs for console ports or asynchronous interface for WAN connections at up to T3/OC-1 rates (55 Mbps).

To enable low chip-count systems, the BCM1250 also includes a configurable generic bus that allows glueless connection of a boot ROM or flash memory and simple I/O peripherals. On-chip debug, trace, and performance monitoring functions assist both hardware and software designers in debugging and tuning the system. The system can be run in either big- or little-endian mode. The BCM1250 is manufactured in TSMC’s 0.13µ process and is available in an 860 BGA package.

**Implementation of MIPS64™ ISA**

The SB-1 CPU core is a high-performance implementation of the standard MIPS64™ instruction set architecture (ISA), and incorporates the MIPS-3D and MIPS-MDMX application specific extensions (ASEs). The core supports a four-issue enhanced skew pipeline and can dispatch up to two memory and two ALU (Integer, Floating Point, MDMX or MIPS-3D) instructions per cycle.