SX48/52 are members of the powerful family of SX configurable communications controllers fabricated in an advanced CMOS process technology. The advanced process, combined with a RISC-based architecture, allows high-speed computation, flexible I/O control, and efficient data manipulation. In addition, the SX architecture is deterministic and totally reprogrammable.

50 MIPS PERFORMANCE
- DC - 50 MHz operation
- 1 instruction per clock (branches 3)
- 20 ns instruction cycle, 60 ns internal interrupt response at 50 MHz

EE/FLASH PROGRAM MEMORY
- In-system programming via oscillator pins
- Access time of <10 ns provides single cycle access
- EE/Flash rated for 10,000 rewrite cycles

FAST AND DETERMINISTIC INTERRUPT
- Hardware context save/restore of PC, W, STATUS, and FSR within the 3-cycle interrupt response time
- Jitter-free 3-cycle internal interrupt response
- External wakeup/interrupt capability on Port B (8 pins)

FLEXIBLE I/O
- All pins individually programmable as I/O
- Inputs are TTL or CMOS level selectable
- All pins have selectable internal pull-ups
- Selectable Schmitt Trigger inputs on Ports B, C, D, and E
- All outputs capable of sinking/sourcing 30 mA
- Port A outputs have symmetrical drive
- Analog comparator on Port B (RB0 out, RB1 in-, RB2 in+)
- I/O operation synchronous to the oscillator clock

COMPONENT REDUCTION
- On-board brown-out detector
- Power-on-reset
- Multi-input wakeup
- Watchdog Timer

FAST TIME TO PRODUCTION
- On-chip in-system programming
- On-chip in-system debug
- Library of Virtual Peripheral™ modules
- Eval Kits for communication intensive applications

GENERAL
- 4096 words of EE/Flash program memory
- 262 bytes of SRAM
- Two 16-bit multi-function timers with 8-bit prescalers
- One 8-bit Real Time Clock/Counter (RTCC) with programmable 8-bit prescaler
- Operating voltage—2.7V to 5.5V
- Fast table lookup capability through run-time readable code
- User selectable clock modes
- TO FP-48, PQFP-52
- Complete third party development tools support
Virtual Peripheral™ concept enables the “software system on a chip” approach. Virtual Peripheral, the software that replaces traditional hardware peripherals, takes advantage of the Scenix architecture’s high clock speeds and deterministic nature to produce same results as hardware peripheral, with much greater flexibility.

With 50 MIPs performance and deterministic architecture, the SX52BD device allows implementation of the entire TCP/IP protocols, physical interface, and other relevant communication interfaces as Virtual Peripheral modules.

**Examples of Virtual Peripheral Modules**

<table>
<thead>
<tr>
<th>Virtual Peripheral</th>
<th>Program Memory Words</th>
<th>Data Memory Bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>UDP/IP/PPP</td>
<td>1700</td>
<td>61</td>
</tr>
<tr>
<td>HTTP/TCP/IP/PPP</td>
<td>3200</td>
<td>100</td>
</tr>
<tr>
<td>SMTP/TCP/IP/PPP</td>
<td>3000</td>
<td>90</td>
</tr>
<tr>
<td>POP3/TCP/IP/PPP</td>
<td>2800</td>
<td>127</td>
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<tr>
<td>DTMF Detection</td>
<td>295</td>
<td>52</td>
</tr>
<tr>
<td>DTMF Generation</td>
<td>89</td>
<td>15</td>
</tr>
<tr>
<td>FSK Detection</td>
<td>42</td>
<td>6</td>
</tr>
<tr>
<td>FSK Generation</td>
<td>47</td>
<td>8</td>
</tr>
<tr>
<td>Caller ID</td>
<td>369</td>
<td>70</td>
</tr>
<tr>
<td>Ring Detect</td>
<td>19</td>
<td>3</td>
</tr>
<tr>
<td>UART</td>
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<td>10</td>
</tr>
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</table>

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