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Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation
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Charles E. Sporck
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Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation
Programmable Logic Devices
DATABOOK AND DESIGN GUIDE

1990 Edition

PART I — DATA BOOK
Product Line Overview
Data Sheets

PART II — DESIGN GUIDE
Designing with PLDs
PLD Design Methodology
PLD Design Development Tools
Fabrication of Programmable Logic
Application Examples
Appendices/Physical Dimensions
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Introduction

HOW TO USE THIS BOOK

This Data Book and Design Guide is intended for use by system designers and manufacturers who wish to take advantage of the opportunities created with National's Programmable Logic Devices (PLDs). The book goes beyond a collection of available data sheets by adding selected application examples and background information on design techniques and benefits of programmable logic products.

The book is laid out to permit users of varying familiarity with PLDs to find the information they need. It should be used as a reference work at all levels and as an introductory tutorial for those areas which require review. While PLDs provide a level of simplicity, flexibility and compactness beyond that offered by other off-the-shelf parts, their optimal use requires the designer to be familiar with design methodologies, development tools and design testing as well as the details of the products themselves.

Experienced users will find reference information in Part I (Data Book). Part I contains two sections which will aid the designer during actual system design and development process. Section 1 provides an overview of the entire programmable logic product line available from National to aid in device selection. Section 2 presents complete data sheets for all listed devices.

For the user new to PLD design, it is recommended that the introductory Section 3 is read first, followed by careful study of Section 4 on design methodology, with reference to PLD Tools in Section 5 and PLD Fabrication (technology and quality) in Section 6 as required. Following this, a review of available products in Section 1 and examination of a few data sheets of interest in Section 2 will provide background for a study of concrete design examples enumerated in Section 7.
### Product Status Definitions

#### Definition of Terms

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PART I
DATA BOOK

Product Line Overview
Data Sheets
Section 1
Product Line Overview
Section 1 Contents

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1.2 Ordering Information ............................................ 1-7
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Section 1 is provided as a reference guide to National Semiconductor’s programmable logic product line. The product selection tables in Section 1.1 and the collection of product block diagrams in Section 1.3 can be used to compare the features and architectures of the various PLD families and to aid in the selection of the appropriate devices which best suit the designer’s application.

1.1 Selection Tables

The product selection tables which follow are organized by technology group (TTL, E²CMOS and ECL), then by “family”, then by “series” within each family. The term “family” refers to a set of one or more “device types” which are variations on the same basic architecture. The term “device type” refers to a specific device architecture (regardless of performance characteristics). The term “series” refers to a particular speed/power version in which the devices of a PLD family are available. Thus as technology advancements provide for improved speed/power performance, a new series is added to selected product families.

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Note 1: Maximum tPD for combinatorial outputs (commercial operating range). Denotes characteristic speed of family where product has all non-registered outputs.
TABLE 1-1. Programmable Logic Product Selection Guide (Continued)

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Note 1: Maximum I_{PD} for combinatorial outputs (commercial operating range). Denotes characteristic speed of family where product has all non-registered outputs.
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**Note 1:** Maximum t\textsubscript{PD} for combinatorial outputs (commercial operating range). Denotes characteristic speed of family where product has all non-registered outputs.
### TABLE 1-1. Programmable Logic Product Selection Guide (Continued)

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**Note 1:** Maximum \( t_{PD} \) for combinational outputs (commercial operating range). Denotes characteristic speed of family where product has all non-registered outputs.
1.2 Ordering Information

The ordering information diagram below defines the product-number nomenclature used throughout National’s programmable logic product line. This nomenclature is based on that used by the original industry-standard PAL products, and are therefore very similar to the product numbers used by other PLD manufacturers. Refer to the corresponding “Ordering Information” diagrams in the individual product datasheets to determine the valid combinations of attributes describing actual PLD products.

- **Technology Family:**
  - PAL = Programmable Array Logic (TTL)
  - GAL = Generic Array Logic (E2CMOS)
  - PAL10 = 10 kHz ECL PAL
  - PAL100 = 100 kHz ECL PAL
  - PL = Factory Programmed PAL
  - NL = National Masked Logic

- **Number of Array Inputs**

- **Output Type:**
  - L = Active Low
  - H = Active High
  - C = Complementary
  - R = Registered
  - X = Exclusive-OR Registered
  - P = Programmable Polarity
  - RA = Registered Asynchronous
  - V = Variable (GAL only)
  - Z = In-System Re-Programmable (GAL only)
  - RD = Registered, Dual Clock (ECL only)
  - RM = Registered, Multiple Clocks (ECL only)

- **Number of Registered/Registered Outputs**
  (or total outputs if non-registered)

- **Speed/Power Series:**
  - No Symbol = 35 ns (TTL); 6 ns (ECL)
  - A = 25 ns (TTL); 4 ns (ECL)
  - A2 = 35 ns, Half-power (TTL)
  - B = 15 ns (TTL)
  - B2 = 25 ns, Half-power (TTL)
  - D = 10 ns (TTL, vertical fuse)
  - 7 = 7 ns
  - 20L = 20 ns, Half-power (GAL)
  - 25L = 25 ns, Half-power (GAL)
  - 25Q = 25 ns, Quarter-power (GAL)
  - 35Q = 30 ns, Quarter-power (GAL)
  - A = 10 ns, Half-power (GAL)
  - A = 12 ns, Half-power (GAL)
  - A = 15 ns, Half-power (GAL)
  - A = 20 ns, Half-power (GAL)

- **Package Type:**
  - N = Plastic DIP
  - J = Ceramic DIP
  - V = Plastic Leaded Chip Carrier
  - W = Quad Cerpak (ECL only)

- **Temperature Range:**
  - C = Commercial
  - M = Military
  - I = Industrial (GAL only)

**FIGURE 1-1. PLD Part-Number Nomenclature and Ordering Information**
1.3 Block Diagrams

The following collection of block diagrams provides a graphic representation of all product architectures ("device types") in National's programmable logic product line. The block diagrams may be used in conjunction with the selection tables in Section 1.1 to identify the most appropriate PLD products to suit the system's application requirements.

20-Pin Small PAL Family

![Block Diagrams for PAL10H8, PAL12H6, PAL14H4, and PAL16H2]
20-Pin Small PAL Family (Continued)

PAL10L8

PAL12L6

PAL14L4

PAL16L2

TL/L/9986-6

TL/L/9986-7

TL/L/9986-8

TL/L/9986-9
20-Pin Small PAL Family (Continued)
24-Pin Small PAL Family

- **PAL12L10**
- **PAL14L8**
- **PAL16L6**
- **PAL18L4**
24-Pin Small PAL Family (Continued)

PAL20L2

PAL20C1

TL/L/9986-19

TL/L/9986-20
24-Pin Exclusive-OR PAL Family

PAL20L10

PAL20X4

PAL20X8

PAL20X10

Product Line Overview
Registered Asynchronous PAL Devices

PAL16RA8

PAL20RA10
Generic Array Logic Family

GAL16V8

AND ARRAY

TL/L/9995-35

1-18
Generic Array Logic Family (Continued)

GAL20V8

AND ARRAY

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC

OLMC
Generic Array Logic Family (Continued)

GAL22V10

AND ARRAY

1 - 24
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24

AR

TL/L/9986-48
Generic Array Logic Family (Continued)

GAL6001 Block Diagram—DIP Connections
Section 2
Data Sheets
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Programmable Array Logic (PAL®) 20-Pin Small PAL Family

General Description

The 20-pin Small PAL family contains nine popular PAL architectures. The devices in the Small PAL family draw only 90 mA maximum supply current for standard power versions, and as little as 45 mA for Series A2 as compared to 180 mA in the 20-pin Medium PAL devices. These devices offer speeds as fast as 25 ns maximum propagation delay. National Semiconductor’s Schottky TIL process with titanium tungsten fusible links provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fusible links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

Device Types

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Dedicated Inputs</th>
<th>Combinatorial Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAL10H8/PAL10L8</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>PAL12H6/PAL12L6</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>PAL14H4/PAL14L4</td>
<td>14</td>
<td>4</td>
</tr>
<tr>
<td>PAL16H2/PAL16L2</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>PAL16C1</td>
<td>16</td>
<td>1 Pair</td>
</tr>
</tbody>
</table>

Speed/Power Versions

<table>
<thead>
<tr>
<th>Series</th>
<th>Example</th>
<th>Commercial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>( t_{PD} )</td>
<td>( I_{CC} )</td>
</tr>
<tr>
<td>Standard</td>
<td>PAL10H8</td>
<td>35 ns</td>
<td>90 mA</td>
</tr>
<tr>
<td>A</td>
<td>PAL10H8A</td>
<td>25 ns*</td>
<td>90 mA</td>
</tr>
<tr>
<td>A2</td>
<td>PAL10H8A2</td>
<td>35 ns*</td>
<td>45 mA</td>
</tr>
</tbody>
</table>

*Except PAL16C1A \( t_{PD} = 30 \) ns Commercial, 35 ns Military. PAL16C1A2 \( t_{PD} = 40 \) ns Commercial.

The Small PAL logic array has between 10 and 16 complementary input pairs and up to 8 combinatorial outputs generated by a single programmable AND-gate array with fixed OR-gate connections. The Small PAL family offers a variety of input/output combinations as shown in the Device Types table below. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- As fast as 25 ns maximum propagation delay
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment available
- Fully supported by National PLAN™ development software
- Security fuse prevents direct copying of logic patterns
### Standard Series (PAL10H8, PAL12H8, PAL14H4, PAL16H2, PAL10L8, PAL12L6, PAL14L4, PAL16L2, PAL16C1)

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Military / Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC) (Note 2)</td>
<td>-0.5 to +7.0V</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Notes 2 and 3)</td>
<td>-1.5 to +5.5V</td>
<td>V</td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>-1.5 to +5.5V</td>
<td>V</td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>-30.0 mA to +5.0 mA</td>
<td></td>
</tr>
</tbody>
</table>

Output Current (IOH) +100 mA
Storage Temperature -65°C to +150°C
Ambient Temperature with Power Applied -65°C to +125°C
Junction Temperature -65°C to +150°C

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>Min 4.5</td>
<td>Nom 5</td>
<td>Max 5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min 4.75</td>
<td>Nom 5</td>
<td>Max 5.25</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>Min -55</td>
<td>Nom 0</td>
<td>Max 75</td>
</tr>
<tr>
<td>TC</td>
<td>Operating Care Temperature</td>
<td>Min 125</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Conditions (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 5)</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 5)</td>
<td></td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Input Clamp Voltage</td>
<td></td>
<td>Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VCC = Max, VI = 0.4V</td>
<td>-0.02</td>
<td>-0.25</td>
<td>mA</td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current</td>
<td></td>
<td>25</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VCC = Max, VI = 5.5V</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Low Level Output Voltage</td>
<td></td>
<td>Min, IOL = 8 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td></td>
<td>Min, IOH = -2 mA</td>
<td>MIL 2.4</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min, IOH = -3 mA</td>
<td>COM -30</td>
<td>70</td>
<td>mA</td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current</td>
<td></td>
<td>Min, VCC = 5V, VO = 0V</td>
<td>-30</td>
<td>-130</td>
<td>mA</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td></td>
<td>Min, VCC = Max, Outputs Open</td>
<td>55</td>
<td>90</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.

**Note 4:** All typical values are for VCC = 5.0V and TA = 25°C.

**Note 5:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Note 6:** To avoid invalid readings in other parameter tests, it is preferable to conduct the IOS test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.
Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>tPD</td>
<td>Input to Output</td>
<td>(C_L = 50 \text{ pF})</td>
<td>25</td>
<td>45</td>
<td></td>
</tr>
</tbody>
</table>

Test Load

\[
\begin{align*}
\text{OUTPUT} & \quad 5V \\
\text{R1} & \quad \text{MIL/COM} \\
\text{R1} = 560 \\
\text{R2} = 1.1K \\
\text{C_L} & \quad \text{OUTPUT}
\end{align*}
\]

Test Waveform

Schematic of Inputs and Outputs

Notes:
- \(V_T = 1.5V\)
- \(C_L\) includes probe and jig capacitance.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
- Supply Voltage (VCC) (Note 2) - 0.5 to +7.0V
- Input Voltage (Notes 2 and 3) - 1.5 to +5.5V
- Off-State Output Voltage (Note 2) - 1.5 to +5.5V
- Input Current (Note 2) - 30.0 mA to +5.0 mA
- Output Current (IOL) +100 mA
- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -65°C to +125°C
- Junction Temperature -65°C to +150°C

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Nom</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>-55</td>
<td>0</td>
</tr>
<tr>
<td>TC</td>
<td>Operating Case Temperature</td>
<td>125</td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics Over Recommended Operating Conditions (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 5)</td>
<td>VCC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>High Level Input Voltage (Note 5)</td>
<td>VCC = Max, VI = 0.4V</td>
<td>-0.02</td>
<td>-0.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>VIIC</td>
<td>Input Clamp Voltage</td>
<td>VCC = Min</td>
<td>-0.8</td>
<td>5 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UIH</td>
<td>High Level Input Current</td>
<td>VCC = Max, VI = 2.4V</td>
<td>-0.2</td>
<td>25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Maximum Input Current</td>
<td>VCC = Max, VI = 5.5V</td>
<td>-0.02</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min</td>
<td>2.4</td>
<td>2.9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 6)</td>
<td>VCC = 5V, VO = 0V</td>
<td>-30</td>
<td>-70</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IIC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>55</td>
<td>90</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: All typical values are for VCC = 5.0V and TA = 25°C.

Note 5: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 6: To avoid invalid readings in other parameter tests, it is preferable to conduct the Ios test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.
Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Input to Output</td>
<td>$C_L = 50 \text{ pF}$ Except 16C1A</td>
<td>15</td>
<td>30</td>
<td></td>
<td>15</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16C1A</td>
<td>35</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Test Load

- **5V**
- **R1**
- **OUTPUT**
- **$C_L$**
- **R2**

**Test Waveform**

**Propagation Delay**

- **INPUT**
- **IN-PHASE OUTPUT**
- **OUT OF PHASE OUTPUT**

**Notes:**
- $V_T = 1.5V$
- $C_L$ includes probe and jig capacitance.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Schematic of Inputs and Outputs
Series A2 (PAL10H8A2, PAL12H6A2, PAL14H4A2, PAL16H2A2, PAL10L8A2, PAL12L6A2, PAL14L4A2, PAL16L2A2, PAL16C1A2)

Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2) \(-0.5\) to \(+7.0\) V
Input Voltage (Notes 2 and 3) \(-1.5\) to \(+5.5\) V
Off-State Output Voltage (Note 2) \(-1.5\) to \(+5.5\) V
Input Current (Note 2) \(-30.0\) mA to \(+5.0\) mA

Output Current (I_{OL}) +100 mA
Storage Temperature \(-65^\circ\text{C}\) to \(+150^\circ\text{C}\)
Ambient Temperature with Power Applied \(-65^\circ\text{C}\) to \(+125^\circ\text{C}\)
Junction Temperature \(-65^\circ\text{C}\) to \(+150^\circ\text{C}\)

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Nom</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>V_{CC}</td>
<td>Supply Voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>T_{A}</td>
<td>Operating Free-Air Temperature</td>
<td>-55</td>
<td>0</td>
<td>75</td>
</tr>
<tr>
<td>T_{C}</td>
<td>Operating Case Temperature</td>
<td>125</td>
<td>*C</td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics Over Recommended Operating Conditions (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IL}</td>
<td>Low Level Input Voltage (Note 5)</td>
<td>V_{CC} = Min, I = -18 mA</td>
<td>-0.8</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{IH}</td>
<td>High Level Input Voltage (Note 5)</td>
<td>V_{CC} = Max, V_{I} = 0.4V</td>
<td>-0.02</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Low Level Input Current</td>
<td>V_{CC} = Max, V_{I} = 2.4V</td>
<td>25</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{I}</td>
<td>Maximum Input Current</td>
<td>V_{CC} = Max, V_{I} = 5.5V</td>
<td>1</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Low Level Output Voltage</td>
<td>V_{CC} = Min, I_{OL} = 8 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>High Level Output Voltage</td>
<td>V_{CC} = Min, I_{OH} = -2 mA</td>
<td>2.4</td>
<td>2.9</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
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<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OS}</td>
<td>Output Short-Circuit Current (Note 6)</td>
<td>V_{CC} = 5V, V_{O} = 0V</td>
<td>-30</td>
<td>-70</td>
<td>-130</td>
<td>mA</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Supply Current</td>
<td>V_{CC} = Max, Outputs Open</td>
<td>28</td>
<td>45</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: All typical values are for V_{CC} = 5.0V and T_{A} = 25°C.

Note 5: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 6: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.
Switching Characteristics

Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Input to Output</td>
<td>$C_L = 50 , \text{pF}$ Except 16C1A2</td>
<td>25</td>
<td>45</td>
<td></td>
<td>25</td>
<td>35</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16C1A2</td>
<td>45</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Test Load

![Test Load Diagram]

Test Waveform

![Test Waveform Diagram]

Notes:

- $V_T = 1.5\, \text{V}$
- $C_L$ includes probe and jig capacitance.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Schematic of Inputs and Outputs

![Schematic Diagram]
20-Pin Small PAL Family Block Diagrams—DIP Connections (Continued)

20-Lead PLCC Connection Conversion Diagram*

*Series-A parts are not available in this package.
Functional Description
The 20-pin Small PAL logic arrays consist of between 10 and 16 complementary input lines and 16 product-term lines with a programmable fuse link at each intersection (up to 512 fuses). The family consists of nine device types with different numbers of combinatorial outputs. The 20-pin Small PAL Family Block Diagrams show the number of product terms allocated to each output for each device. All product terms allocated to each output connect into an OR-gate to produce the sum-of-products output logic function.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, $V_{OL}$, $V_{OH}$, or resistively to $V_{CC}$. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

Security Fuse
Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses.

Design Development Support
A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible “fuse maps”. The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 20-pin Small PAL family are provided for direct map editing and diagnostic purposes. Contact your local National Semiconductor sales representative or distributor for a list of current software and programming support tools available for these devices. Contact the National Semiconductor Programmable Device Support Department if detailed specifications of PAL programming algorithms are needed.

Ordering Information

<table>
<thead>
<tr>
<th>Programmable Array Logic Family</th>
<th>Number of Array Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Type:</td>
<td>H = Active High</td>
</tr>
<tr>
<td></td>
<td>L = Active Low</td>
</tr>
<tr>
<td></td>
<td>C = Complementary</td>
</tr>
<tr>
<td></td>
<td>R = Registered</td>
</tr>
<tr>
<td></td>
<td>X = Exclusive-OR Registered</td>
</tr>
<tr>
<td></td>
<td>P = Programmable Polarity</td>
</tr>
<tr>
<td>Speed/Power Version:</td>
<td>No Symbol = 35 ns</td>
</tr>
<tr>
<td></td>
<td>A = 25 ns</td>
</tr>
<tr>
<td></td>
<td>A2 = 35 ns, Half Power</td>
</tr>
<tr>
<td>Package Type:</td>
<td>N = 20-Pin Plastic DIP</td>
</tr>
<tr>
<td></td>
<td>J = 20-Pin Ceramic DIP</td>
</tr>
<tr>
<td></td>
<td>V = 20-Lead Plastic Chip Carrier</td>
</tr>
<tr>
<td>Temperature Range:</td>
<td>C = Commercial (0°C to +75°C)</td>
</tr>
<tr>
<td></td>
<td>M = Military (-55°C to +125°C)</td>
</tr>
</tbody>
</table>

*Series-A is not available in the V-package.*
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL14H4

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

TL/L/9995-18
Logic Diagram PAL16H2

DIP PIN NUMBERS
PRODUCT LINE FIRST FUSE NUMBERS
0 2 4 6 8 10 11 13 15 17 19 21 23 25 27 29 31
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31

INPUT LINE NUMBERS
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30

VCC

DIP PIN NUMBERS
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL10L8

DIP PIN NUMBERS
PRODUCT LINE FIRST FUSE NUMBERS

INPUT LINE NUMBERS
DIP PIN NUMBERS

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL12L6

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL16L2

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Programmable Array Logic (PAL®)
20-Pin Medium PAL Family

General Description
The 20-pin Medium PAL family contains four of the most popular PAL architectures used in industry. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the standard, Series-A, Series-A2, Series-B and Series-B2 devices. Series-D devices are manufactured using National Semiconductor's isoplanar "FAST-Z" TTL process with highly reliable "vertical-fuse" programmable cells. Vertical fuses are implemented using avalanche-induced migration ("AIM") technology offering very high programming yields and is an extension of National's FAST logic family. The 20-pin Medium PAL Family provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL logic array has a total of 16 complementary input pairs and 8 outputs generated by a single programmable AND-gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passed through D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The medium PAL family offers a variety of combinatorial and registered output mixtures, as shown in the Device Types table below.

Features
- As fast as 7 ns maximum propagation delay (combinatorial)
- User-programmable replacement for TTL logic
- High programming yield and reliability of vertical-fuse technology for Series-D/-7 products. (Programming equipment with certified vertical-fuse algorithm required.)
- Extension of FAST product line
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLAN™ development software
- Power-up reset for registered outputs
- Register preload facilitates device testing
- Security fuse prevents direct copying of logic patterns

Device Types

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Dedicated Inputs</th>
<th>Registered Outputs (with Feedback)</th>
<th>Combinatorial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>I/Os</td>
<td>Outputs</td>
</tr>
<tr>
<td>PAL16L8</td>
<td>10</td>
<td>---</td>
<td>6 2</td>
</tr>
<tr>
<td>PAL16R4</td>
<td>8</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>PAL16R6</td>
<td>8</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>PAL16R8</td>
<td>8</td>
<td>8</td>
<td>---</td>
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</tbody>
</table>

Speed/Power Versions

<table>
<thead>
<tr>
<th>Series</th>
<th>Example</th>
<th>Commercial</th>
<th>Military</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>tpD</td>
<td>tPD</td>
</tr>
<tr>
<td>Standard</td>
<td>PAL16L8</td>
<td>35 ns</td>
<td>45 ns</td>
</tr>
<tr>
<td>A</td>
<td>PAL16L8A</td>
<td>25 ns</td>
<td>30 ns</td>
</tr>
<tr>
<td>A2</td>
<td>PAL16L8A2</td>
<td>35 ns</td>
<td>50 ns</td>
</tr>
<tr>
<td>B</td>
<td>PAL16L8B</td>
<td>15 ns</td>
<td>20 ns</td>
</tr>
<tr>
<td>B2</td>
<td>PAL16L8B2</td>
<td>25 ns</td>
<td>30 ns</td>
</tr>
<tr>
<td>D</td>
<td>PAL16L8D</td>
<td>10 ns</td>
<td>30 ns</td>
</tr>
<tr>
<td>-7</td>
<td>PAL16L8-7</td>
<td>7 ns</td>
<td></td>
</tr>
</tbody>
</table>

*For the registered devices Icc = 100 mA.

Block Diagram—PAL16R8

[Diagram showing PAL16R8 block diagram]
Standard Series (PAL16L8, PAL16R4, PAL16R6, PAL16R8)

Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) (Note 2)  
Input Voltage (Notes 2 and 3)  
Off-State Output Voltage (Note 2)  
Input Current (Note 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min  Nom Max</td>
<td>Min  Nom Max</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.5 5 5.5</td>
<td>4.75 5 5.25</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>-55</td>
<td>0 75</td>
</tr>
<tr>
<td>TC</td>
<td>Operating Case Temperature</td>
<td>125</td>
<td>*C</td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width</td>
<td>Low 25 25 ns</td>
<td>High 25 25 ns</td>
</tr>
<tr>
<td>tSU</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>45 35 ns</td>
<td></td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time of Input after Clock</td>
<td>0 -15</td>
<td>0 -15</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency</td>
<td>With Feedback 12.2 MHz</td>
<td>Without Feedback 20 MHz</td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>VCC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 6)</td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIC</td>
<td>Input Clamp Voltage</td>
<td>VCC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current (Note 7)</td>
<td>VCC = Max, VI = 0.4V</td>
<td>-0.02</td>
<td>-0.25 mA</td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current (Note 7)</td>
<td>VCC = Max, VI = 2.4V</td>
<td>25</td>
<td>*A</td>
<td></td>
</tr>
<tr>
<td>IM</td>
<td>Maximum Input Current</td>
<td>VCC = Max, VI = 5.5V</td>
<td>100</td>
<td>*A</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min</td>
<td>IOL = 12 mA</td>
<td>MIL</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min</td>
<td>IOH = -2 mA</td>
<td>MIL</td>
<td></td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>VCC = Max</td>
<td>V0 = 0.4V</td>
<td>-100</td>
<td>*A</td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>VCC = Max</td>
<td>V0 = 2.4V</td>
<td>100</td>
<td>*A</td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>VCC = 5V, V0 = 0V</td>
<td>-30</td>
<td>-70</td>
<td>-130</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>120</td>
<td>180</td>
<td>mA</td>
</tr>
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</table>

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>VCC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 6)</td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIC</td>
<td>Input Clamp Voltage</td>
<td>VCC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current (Note 7)</td>
<td>VCC = Max, VI = 0.4V</td>
<td>-0.02</td>
<td>-0.25 mA</td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current (Note 7)</td>
<td>VCC = Max, VI = 2.4V</td>
<td>25</td>
<td>*A</td>
<td></td>
</tr>
<tr>
<td>IM</td>
<td>Maximum Input Current</td>
<td>VCC = Max, VI = 5.5V</td>
<td>100</td>
<td>*A</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min</td>
<td>IOL = 12 mA</td>
<td>MIL</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min</td>
<td>IOH = -2 mA</td>
<td>MIL</td>
<td></td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>VCC = Max</td>
<td>V0 = 0.4V</td>
<td>-100</td>
<td>*A</td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>VCC = Max</td>
<td>V0 = 2.4V</td>
<td>100</td>
<td>*A</td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>VCC = 5V, V0 = 0V</td>
<td>-30</td>
<td>-70</td>
<td>-130</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>120</td>
<td>180</td>
<td>mA</td>
</tr>
</tbody>
</table>
**Standard Series** (PAL16L8, PAL16R4, PAL16R6, PAL16R8) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** f_{CLK} with feedback is derived as (f_{CLK} + 1/\tau_W)^{-1}.

f_{CLK} without feedback is derived as (2/\tau_W)^{-1}.

**Note 5:** All typical values are for V_{CC} = 5.0V and T_A = 25°C.

**Note 6:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Switching Characteristics** Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>t_{PD}</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>C_L = 50 pF, S1 Closed</td>
<td>25</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>t_{CLK}</td>
<td>Clock to Registered Output or Feedback</td>
<td>C_L = 50 pF, S1 Closed</td>
<td>15</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>t_{PZXG}</td>
<td>Pin to Registered Output Enabled</td>
<td>C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>15</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>t_{PXZG}</td>
<td>Pin to Registered Output Disabled</td>
<td>C_L = 50 pF, From V_OH: S1 Open, From V_OL: S1 Closed</td>
<td>15</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>t_{PXZI}</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>25</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>t_{PXZI}</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>C_L = 50 pF, From V_OH: S1 Open, From V_OL: S1 Closed</td>
<td>25</td>
<td>45</td>
<td></td>
</tr>
</tbody>
</table>

**Test Load**

**Schematic of Inputs and Outputs**

---

TL/L9391-2
### Series-A (PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A)

#### Absolute Maximum Ratings (Note 1)

- **Military/Aerospace** specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
- **Supply Voltage** ($V_{CC}$) (Note 2): $-0.5V$ to $+7.0V$
- **Input Voltage** (Notes 2 and 3): $-1.5V$ to $+5.5V$
- **Off-State Output Voltage** (Note 2): $-1.5V$ to $+5.5V$
- **Input Current** (Note 2): $-30.0 mA$ to $+5.0 mA$

- **Output Current** ($I_{OL}$): $100 mA$
- **Storage Temperature**: $-65°C$ to $+150°C$
- **Ambient Temperature with Power Applied**: $-65°C$ to $+125°C$
- **Junction Temperature**: $-65°C$ to $+150°C$
- **ESD**: $1500V$

#### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Military Min</th>
<th>Nom</th>
<th>Max</th>
<th>Commercial Min</th>
<th>Nom</th>
<th>Max</th>
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<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
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</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td>$-55$</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>75</td>
<td>°C</td>
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<tr>
<td>$T_C$</td>
<td>Operating Case Temperature</td>
<td>125</td>
<td></td>
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<td>25</td>
<td>125</td>
<td>°C</td>
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<tr>
<td>$t_W$</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>20</td>
<td>10</td>
<td>15</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
<td>20</td>
<td>10</td>
<td>15</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>30</td>
<td>16</td>
<td>25</td>
<td>16</td>
<td>ns</td>
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<tr>
<td>$t_H$</td>
<td>Hold Time of Input after Clock</td>
<td>0</td>
<td>$-10$</td>
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<td>$-10$</td>
<td>ns</td>
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<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback</td>
<td>20</td>
<td></td>
<td></td>
<td>25</td>
<td>MHz</td>
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<td></td>
<td></td>
<td>Without Feedback</td>
<td>25</td>
<td></td>
<td></td>
<td>33.3</td>
<td>MHz</td>
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#### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

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<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>$V_{CC} = \text{Min}, I = -18 mA$</td>
<td>$0.8$</td>
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<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Input Clamp Voltage</td>
<td>$V_{CC} = \text{Max}, V_I = 0.4V$</td>
<td>$-0.02$</td>
<td>$-0.25$</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current (Note 7)</td>
<td>$V_{CC} = \text{Max}, V_I = 5.5V$</td>
<td>100</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current (Note 7)</td>
<td>$V_{CC} = \text{Max}, V_I = 2.4V$</td>
<td>25</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max}, V_I = 5.5V$</td>
<td>100</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_{OL} = 12 mA$</td>
<td>MIL</td>
<td>0.3</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OL} = 24 mA$</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_{OH} = -2 mA$</td>
<td>MIL</td>
<td>2.4</td>
<td>2.9</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OH} = -3.2 mA$</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_O = 2.4V$</td>
<td></td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_O = 0.4V$</td>
<td></td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>$V_{CC} = 5V, V_O = 0V$</td>
<td>$-30$</td>
<td>$-70$</td>
<td>$-130$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC} = \text{Max}, Outputs Open$</td>
<td>120</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>
Series-A (PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

Note 4: $I_{CKL}$ with feedback is derived as $(I_{CLK} + I_F)\times 1$.

$I_{CLK}$ without feedback is derived as $(2I_F)\times 1$.

Note 5: All typical values are for $V_{CC} = 5.0$V and $T_A = 25^\circ$C.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between $I_{IH}$ and $I_{OZH}$ or between $I_{IL}$ and $I_{OZL}$.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{QS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>$C_L = 50$ pF, S1 Closed</td>
<td>Min Typ Max</td>
<td>Min Typ Max</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLK}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>$C_L = 50$ pF, S1 Closed</td>
<td>15 30</td>
<td>15 25</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZXG}$</td>
<td>Pin to Registered Output Enabled</td>
<td>$C_L = 50$ pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>10 20</td>
<td>10 15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PXZG}$</td>
<td>Pin to Registered Output Disabled</td>
<td>$C_L = 50$ pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed</td>
<td>11 25</td>
<td>11 20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZXI}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>$C_L = 50$ pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>10 30</td>
<td>10 25</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PXZI}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>$C_L = 50$ pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed</td>
<td>13 30</td>
<td>13 25</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Test Load

![Test Load Diagram](image)

### Schematic of Inputs and Outputs

![Schematic Diagram](image)
**Series-A2 (PAL16L8A2, PAL16R4A2, PAL16R6A2, PAL16R8A2)**

**Absolute Maximum Ratings (Note 1)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Vcc)</td>
<td>-0.5V to +7.0V</td>
<td>-0.5V to +7.0V</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Notes 2 and 3)</td>
<td>-1.5V to +5.5V</td>
<td>-1.5V to +5.5V</td>
<td>V</td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>-1.5V to +5.5V</td>
<td>-1.5V to +5.5V</td>
<td>V</td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>-30.0 mA to +5.0 mA</td>
<td>-30.0 mA to +5.0 mA</td>
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</tr>
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</table>

**Storage Temperature**

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<tr>
<th>Condition</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
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<tbody>
<tr>
<td>Military/Aerospace specified devices are required</td>
<td>-65°C to +150°C</td>
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<td></td>
</tr>
<tr>
<td>Ambient Temperature with Power Applied</td>
<td>-65°C to +125°C</td>
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</table>

**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td></td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td></td>
<td>-55</td>
<td>125</td>
<td>0</td>
</tr>
<tr>
<td>Tw</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>25</td>
<td>10</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
<td>25</td>
<td>10</td>
<td>25</td>
</tr>
<tr>
<td>tsu</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td></td>
<td>50</td>
<td>25</td>
<td>35</td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time of Input after Clock</td>
<td></td>
<td>0</td>
<td>-15</td>
<td>0</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency</td>
<td>With Feedback</td>
<td>13.3</td>
<td></td>
<td>16.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback</td>
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**Electrical Characteristics** Over Recommended Operating Conditions (Note 5)

<table>
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<th>Symbol</th>
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<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Input Clamp Voltage VCC = Min, I = -18 mA</td>
<td></td>
<td>-0.8</td>
<td>-1.5</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current (Note 7)</td>
<td>VCC = Max, V1 = 0.4V</td>
<td>-0.02</td>
<td>-0.25</td>
<td>mA</td>
</tr>
<tr>
<td>IIH</td>
<td>High Level Input Current (Note 7)</td>
<td>VCC = Max, V1 = 2.4V</td>
<td>25</td>
<td></td>
<td>µA</td>
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<tr>
<td>Ii</td>
<td>Maximum Input Current</td>
<td>VCC = Max, V1 = 5.5V</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min IOL = 12 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOL = 24 mA</td>
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<td></td>
<td>COM</td>
</tr>
<tr>
<td>VDH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min IOH = -2 mA</td>
<td>2.4</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOH = -3.2 mA</td>
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<td>COM</td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>VCC = Max V0 = 0.4V</td>
<td>-100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>IZH</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>VCC = Max V0 = 2.4V</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Ios</td>
<td>Output Short-Circuit Current</td>
<td>VCC = 5V, V0 = 0V</td>
<td>-30</td>
<td>-70</td>
<td>-130</td>
</tr>
<tr>
<td>Icc</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>70</td>
<td>90</td>
<td>mA</td>
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</tbody>
</table>
Nota 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Nota 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Nota 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

Nota 4: \( f_{CL} \) with feedback is derived as \( (t_{CL} + t_{SU})^{-1} \).

Nota 5: All typical values are for \( V_{EE} = 5.0\text{V} \) and \( T_A = 25^\circ\text{C} \).

Nota 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Nota 7: Leakage current for bidirectional I/O pins is the worst case between \( I_{HI} \) and \( I_{OL} \) or between \( I_{HL} \) and \( I_{OH} \).

Nota 8: To avoid invalid readings in other parameter tests it is preferable to conduct the \( I_{OL} \) test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

**Switching Characteristics** Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military Min</th>
<th>Military Typ</th>
<th>Military Max</th>
<th>Commercial Min</th>
<th>Commercial Typ</th>
<th>Commercial Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>( C_L = 50 \text{pF}, S_1 \text{ Closed} )</td>
<td>25</td>
<td>50</td>
<td>25</td>
<td>35</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>Clock to Registered Output or Feedback</td>
<td>( C_L = 50 \text{pF}, S_1 \text{ Closed} )</td>
<td>15</td>
<td>25</td>
<td>15</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PXZG} )</td>
<td>( \bar{G} ) Pin to Registered Output Enabled</td>
<td>( C_L = 50 \text{pF}, \text{Active High: } S_1 \text{ Open, Active Low: } S_1 \text{ Closed} )</td>
<td>15</td>
<td>25</td>
<td>15</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PXZI} )</td>
<td>( \bar{G} ) Pin to Registered Output Disabled</td>
<td>( C_L = 5 \text{pF}, \text{From } V_{OH}: S_1 \text{ Open, From } V_{OL}: S_1 \text{ Closed} )</td>
<td>25</td>
<td>45</td>
<td>25</td>
<td>35</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PXZI} )</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>( C_L = 50 \text{pF}, \text{Active High: } S_1 \text{ Open, Active Low: } S_1 \text{ Closed} )</td>
<td>25</td>
<td>45</td>
<td>25</td>
<td>35</td>
<td>ns</td>
<td></td>
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</tr>
</tbody>
</table>

**Test Load**

**Schematic of Inputs and Outputs**
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC)</td>
<td>–0.5V to +7.0V</td>
<td>–1.5V to +5.5V</td>
</tr>
<tr>
<td>Input Voltage (Notes 2 and 3)</td>
<td>–1.5V to +5.5V</td>
<td>–1.5V to +5.5V</td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>–1.5V to +5.5V</td>
<td>–1.5V to +5.5V</td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>–30.0 mA to +5.0 mA</td>
<td></td>
</tr>
</tbody>
</table>

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>VCC = Min, I = –18 mA</td>
<td>–0.8</td>
<td>–1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td></td>
<td>–55</td>
<td></td>
<td>0</td>
<td>°C</td>
</tr>
<tr>
<td>TC</td>
<td>Operating Case Temperature</td>
<td></td>
<td>0</td>
<td>125</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>12</td>
<td>5</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
<td>12</td>
<td>5</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>tSU</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td></td>
<td>20</td>
<td>10</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time of Input after Clock</td>
<td></td>
<td>0</td>
<td>–5</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback</td>
<td>28.6</td>
<td></td>
<td>40</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback</td>
<td>41.7</td>
<td></td>
<td>50</td>
<td>MHz</td>
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### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 6)</td>
<td></td>
<td>0.8</td>
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<td>V</td>
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<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIC</td>
<td>Input Clamp Voltage</td>
<td>VCC = Min, V = 0.4V</td>
<td>–0.02</td>
<td>–0.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Low Level Input Current (Note 7)</td>
<td>VCC = Max, V = 0.4V</td>
<td>–0.02</td>
<td>–0.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IILH</td>
<td>High Level Input Current (Note 7)</td>
<td>VCC = Max, V = 2.4V</td>
<td>25</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Ii</td>
<td>Maximum Input Current</td>
<td>VCC = Max, V = 5.5V</td>
<td>100</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V0H</td>
<td>High Level Output Voltage</td>
<td>VCC = Min</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOZL</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>VCC = Max</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOZH</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>VCC = Max</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>VCC = 5V, V = 0V</td>
<td>–100</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>120</td>
<td></td>
<td>180</td>
<td>mA</td>
</tr>
</tbody>
</table>
Series-B (PAL16L6B, PAL16R4B, PAL16R6B, PAL16R8B) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** \( t_{\text{CLK}} \text{ with feedback is derived as } (t_{\text{CLK}} + t_{\text{pd}})^{-1} \).

**Note 5:** Absolute maximum ratings are for \( V_{CC} = 5.0 \) V and \( T_A = 25^\circ \) C.

**Note 6:** Those are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Switching Characteristics** Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min Typ Max</td>
<td>Min Typ Max</td>
<td>ns</td>
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<tr>
<td>( t_{\text{PD}} )</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>( C_L = 50 ) pF, S1 Closed</td>
<td>11 20</td>
<td>11 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{CLK}} )</td>
<td>Clock to Registered Output or Feedback</td>
<td>( C_L = 50 ) pF, S1 Closed</td>
<td>8 15</td>
<td>8 12</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{PZXG}} )</td>
<td>G Pin to Registered Output Enabled</td>
<td>( C_L = 50 ) pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>10 20</td>
<td>10 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{PXZG}} )</td>
<td>G Pin to Registered Output Disabled</td>
<td>( C_L = 5 ) pF, From ( V_{OH} ): S1 Open, From ( V_{OL} ): S1 Closed</td>
<td>10 20</td>
<td>10 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{PXZI}} )</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>( C_L = 50 ) pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>11 20</td>
<td>11 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{PXZI}} )</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>( C_L = 5 ) pF, From ( V_{OH} ): S1 Open, From ( V_{OL} ): S1 Closed</td>
<td>11 20</td>
<td>11 15</td>
<td>ns</td>
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**Test Load**

![Test Load Schematic](image)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_1 )</td>
<td>MIL</td>
<td>390</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>MIL</td>
<td>750</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>COM/L</td>
<td>200</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>COM/L</td>
<td>390</td>
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</table>

**Schematic of Inputs and Outputs**

![Schematic of Inputs and Outputs](image)
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
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<tbody>
<tr>
<td>Supply Voltage (VCC)</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>-1.5V to +5.5V</td>
<td></td>
<td></td>
<td>-1.5V to +5.5V</td>
<td></td>
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<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>-1.5V to +5.5V</td>
<td></td>
<td></td>
<td>-1.5V to +5.5V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>-30.0 mA to +5.0 mA</td>
<td></td>
<td></td>
<td>-30.0 mA to +5.0 mA</td>
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<tr>
<td>Output Current (IOL)</td>
<td>100 mA</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>-65°C to +125°C</td>
<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>ESD Tolerance (Note 3)</td>
<td>2000V</td>
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#### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
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<th>Commercial</th>
<th>Units</th>
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<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>Min</td>
<td>Nom</td>
<td>Max</td>
</tr>
<tr>
<td>T_a</td>
<td>Operating Free-Air Temperature</td>
<td>-55</td>
<td>125</td>
<td>0</td>
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<tr>
<td>t_w</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>15</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>t_s_u</td>
<td>Setup Time from Input</td>
<td>25</td>
<td>11</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>or Feedback to Clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_h</td>
<td>Hold Time of Input after</td>
<td>0</td>
<td>-10</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f_c_l_k</td>
<td>Clock Frequency</td>
<td>22.2</td>
<td>28.6</td>
<td>40</td>
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</table>

#### Electrical Characteristics

Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_I_L</td>
<td>Low Level Input Voltage</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_HI_H</td>
<td>High Level Input Voltage</td>
<td></td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_C_C</td>
<td>Input Clamp Voltage</td>
<td>V_CC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td>V</td>
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<tr>
<td>I_I_L</td>
<td>Low Level Input Current</td>
<td>V_CC = Max, V_I = 0.4V</td>
<td>-0.02</td>
<td>-0.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_HI_H</td>
<td>High Level Input Current</td>
<td>V_CC = Max, V_I = 2.4V</td>
<td>25</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_I</td>
<td>Maximum Input Current</td>
<td>V_CC = Max, V_I = 5.5V</td>
<td>100</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_O_L</td>
<td>Low Level Output Voltage</td>
<td>V_CC = Min, I_O_L = 12 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_O_H</td>
<td>High Level Output Voltage</td>
<td>V_CC = Min, I_O_H = 2 mA</td>
<td>2.4</td>
<td>3.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_O_Z_L</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>V_CC = Max, V_O = 0.4V</td>
<td>-100</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_O_Z_H</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>V_CC = Max, V_O = 2.4V</td>
<td>100</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_O_S</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>V_CC = 5V, V_O = 0V</td>
<td>-30</td>
<td>-70</td>
<td>-130</td>
<td>mA</td>
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<tr>
<td>I_C_C</td>
<td>Supply Current</td>
<td>V_CC = Max, Outputs Open</td>
<td>60</td>
<td>90</td>
<td>16L8B2</td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>16R4B2, 16R6B2, 16R8B2</td>
<td>70</td>
<td>100</td>
<td></td>
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</tr>
</tbody>
</table>

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and, although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** 
- $t_{\text{CLK}}$ with feedback is derived as $(t_{\text{CLK}} + t_{\text{SU}})^{-1}$.
- $t_{\text{CLK}}$ without feedback is derived as $(t_{\text{LOW}} + t_{\text{HIGH}})^{-1}$.

**Note 5:** All typical values are for $V_{\text{CC}} = 5.0\text{V}$ and $T_{\text{A}} = 25^\circ\text{C}$.

**Note 6:** Leakage current for bidirectional I/O pins is the worst case between $I_{\text{IL}}$ and $I_{\text{OL}}$, or between $I_{\text{IH}}$ and $I_{\text{OH}}$.

**Note 7:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{\text{OL}}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics

**Over Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{PD}}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>$C_{L} = 50\ \text{pF}, S1\ \text{Closed}$</td>
<td>15</td>
<td>30</td>
<td>15</td>
</tr>
<tr>
<td>$t_{\text{CLK}}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>$C_{L} = 50\ \text{pF}, S1\ \text{Closed}$</td>
<td>10</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>$t_{\text{IPZG}}$</td>
<td>G Pin to Registered Output Enabled</td>
<td>$C_{L} = 50\ \text{pF}, \text{Active High: } S1\ \text{Open, Active Low: } S1\ \text{Closed}$</td>
<td>15</td>
<td>25</td>
<td>15</td>
</tr>
<tr>
<td>$t_{\text{IPXZG}}$</td>
<td>G Pin to Registered Output Disabled</td>
<td>$C_{L} = 50\ \text{pF}, \text{Active High: } S1\ \text{Open, Active Low: } S1\ \text{Closed}$</td>
<td>15</td>
<td>25</td>
<td>15</td>
</tr>
<tr>
<td>$t_{\text{IPXZI}}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>$C_{L} = 50\ \text{pF}, \text{Active High: } S1\ \text{Open, Active Low: } S1\ \text{Closed}$</td>
<td>15</td>
<td>25</td>
<td>15</td>
</tr>
<tr>
<td>$t_{\text{IPXI}}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>$C_{L} = 50\ \text{pF}, \text{Active High: } S1\ \text{Open, Active Low: } S1\ \text{Closed}$</td>
<td>15</td>
<td>25</td>
<td>15</td>
</tr>
</tbody>
</table>

**Test Load**

![Test Load Diagram]

**Schematic of Inputs and Outputs**

![Schematic Diagram]
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC) (Note 2)</td>
<td>-0.5V</td>
<td>+7.0V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>-1.5V</td>
<td>+7.0V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Off-State Output Voltage (VO) (Notes 2 &amp; 3)</td>
<td>-1.5V</td>
<td>+5.5V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>-30.0 mA</td>
<td>+5.0 mA</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Output Current (IO)</td>
<td>+100 mA</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C</td>
<td>+150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Temperature with Power Applied</td>
<td>-65°C</td>
<td>+125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>-65°C</td>
<td>+150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Tolerance</td>
<td>2000V</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>CzAP</td>
<td>100 pF</td>
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<tr>
<td>RzAP</td>
<td>1500Ω</td>
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<td>Test Method: Human Body Model</td>
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<td>Test Specification: NSC SOP-5-028</td>
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### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>0</td>
<td>25</td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width Low</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td></td>
<td>Clock Pulse Width High</td>
<td>7</td>
<td>2</td>
</tr>
<tr>
<td>tSU</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>10</td>
<td>5.5</td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time of Input after Clock</td>
<td>0</td>
<td>-3.7</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency With Feedback</td>
<td>55.5</td>
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<td></td>
<td>Clock Frequency Without Feedback</td>
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<td></td>
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<td>VZ</td>
<td>Register Preload Control Voltage</td>
<td>9.5</td>
<td>9.75</td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 6)</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIC</td>
<td>Input Clamp Voltage</td>
<td>VCC = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Low Level Input Current (Note 7)</td>
<td>VCC = Max, V = 0.4V</td>
<td>-60</td>
<td>-250</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current (Note 7)</td>
<td>VCC = Max, V = 2.4V</td>
<td>0</td>
<td>25</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I1</td>
<td>Maximum Input Current</td>
<td>VCC = Max, V = 5.5V</td>
<td>20</td>
<td>100</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min, IOL = 24 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min, IOH = -3.2 mA</td>
<td>2.7</td>
<td>3.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOZL</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>VCC = Max, VO = 0.4V</td>
<td>0</td>
<td>-50</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IOZH</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>VCC = Max, VO = 2.4V</td>
<td>0</td>
<td>50</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>VCC = 5V, VO = 0V</td>
<td>-50</td>
<td>-77</td>
<td>-130 mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>125</td>
<td>180</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>VCC = 5.0V, V1 = 2.0V</td>
<td>8</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>VCC = 5.0V, VO = 2.0V</td>
<td>8</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>VCC = 5.0V, V1O = 2.0V</td>
<td>8</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>
Series-D (PAL16L8D, PAL16R4D, PAL16R6D, PAL16R8D) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: VO must not exceed VCC + 1V

Note 4: tCLK with feedback is derived as (tCLK + tSU)^-1.

Note 5: All typical values are for VCC = 5.0V and TA = 25°C.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between |IH| and |IOZL| or between |IL| and |IOZH|.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the tQH test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Commercial Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>C_L = 50 pF, S1 Closed</td>
<td>Min</td>
</tr>
<tr>
<td>tCLK</td>
<td>Clock to Registered Output or Feedback</td>
<td>C_L = 50 pF, S1 Closed</td>
<td>7.1</td>
</tr>
<tr>
<td>tPZXG</td>
<td>G Pin to Registered Output Enabled</td>
<td>C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>5.5</td>
</tr>
<tr>
<td>tPXZG</td>
<td>G Pin to Registered Output Disabled</td>
<td>C_L = 5 pF, From VOH: S1 Open, From VOL: S1 Closed</td>
<td>4.0</td>
</tr>
<tr>
<td>tPZXI</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>7.2</td>
</tr>
<tr>
<td>tPXZII</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>C_L = 5 pF, From VOH: S1 Open, From VOL: S1 Closed</td>
<td>5.0</td>
</tr>
<tr>
<td>tRESET</td>
<td>Power-Up to Registered Output High</td>
<td></td>
<td>1000</td>
</tr>
</tbody>
</table>

Test Load

Schematic of Inputs and Outputs
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Supply Voltage** (VCC) (Note 2): 
  - -0.5V to +7.0V
- **Input Voltage** (Note 2): 
  - -1.5V to +7.0V
- **Off-State Output Voltage** (V0) (Notes 2 & 3): 
  - -1.5V to +5.5V
- **Input Current** (Note 2): 
  - -30.0 mA to +5.0 mA
- **Output Current** (IOL): 
  - +100 mA

**Storage Temperature**: 
- -65°C to +150°C

**Ambient Temperature** with Power Applied: 
- -65°C to +125°C

**Junction Temperature** 
- -65°C to +150°C

**ESD Tolerance**
- CZAP = 100 pF
- RZAP = 1500Ω

**Test Method:** Human Body Model

**Test Specification:** NSC SOP-5-028

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.75 5 5.25</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>0 25 75</td>
<td>°C</td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width</td>
<td>Low: 5.0, High: 5.0</td>
<td>ns</td>
</tr>
<tr>
<td>tSU</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>6.5</td>
<td>ns</td>
</tr>
<tr>
<td>th</td>
<td>Hold Time of Input after Clock</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback: 77 MHz, Without Feedback: 100 MHz</td>
<td></td>
</tr>
<tr>
<td>VZ</td>
<td>Register Preload Control Voltage</td>
<td>9.5 9.75 10.0</td>
<td>V</td>
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</table>

### Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 5)</td>
<td>VCC = Min, I = -18 mA</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 5)</td>
<td>VCC = Max, I = 0.4V</td>
<td>-250</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIC</td>
<td>Input Clamp Voltage</td>
<td>I = -18 mA</td>
<td>-1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIL</td>
<td>Low Level Input Current (Note 6)</td>
<td>VCC = Max, I = 0.4V</td>
<td>250</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIH</td>
<td>High Level Input Current (Note 6)</td>
<td>I = 2.4V</td>
<td>25</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ii</td>
<td>Maximum Input Current</td>
<td>VCC = Max, I = 5.5V</td>
<td>100</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min, IOL = 24 mA</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min, IOH = -3.2 mA</td>
<td>2.7</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOLZL</td>
<td>Low Level Off-State Output Current (Note 6)</td>
<td>VCC = Max, VO = 0.4V</td>
<td>-50</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOLZH</td>
<td>High Level Off-State Output Current (Note 6)</td>
<td>VCC = Max, VO = 2.4V</td>
<td>50</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 7)</td>
<td>VCC = 5V, VO = 0V</td>
<td>-50</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>125</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>VCC = 5.0V, I = 2.0V</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>VCC = 5.0V, I = 2.0V</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CI/O</td>
<td>I/O Capacitance</td>
<td>VCC = 5.0V, I/O = 2.0V</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 7 ns Series (PAL16L8-7, PAL16R4-7, PAL16R6-7, PAL16R8-7)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above those limits during programming and preload operations according to the applicable specification.

**Note 4:** If \( t_{CLK} \) with feedback is derived as \( (t_{CLK} + t_{SU})^{-1} \),

\( t_{CLK} \) without feedback is derived as \( (2t_{SW})^{-1} \).

**Note 5:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test those values without suitable equipment.

**Note 6:** Leakage current for bidirectional I/O pins is the worst case between \( I_{L} \) and \( I_{LZ} \) or between \( I_{H} \) and \( I_{ZH} \).

**Note 7:** To avoid invalid readings in other parameter tests it is preferable to conduct the \( I_{OL} \) test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a HIGH output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Commercial Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>( C_L = 50 ) pF, S1 Closed</td>
<td>Min Typ Max</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>Clock to Registered Output or Feedback</td>
<td>( C_L = 50 ) pF, S1 Closed</td>
<td>3.0 6.5 ns</td>
</tr>
<tr>
<td>( t_{PZXG} )</td>
<td>( \bar{G} ) Pin to Registered Output Enabled</td>
<td>( C_L = 50 ) pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>3.0 7.0 ns</td>
</tr>
<tr>
<td>( t_{PXZG} )</td>
<td>( \bar{G} ) Pin to Registered Output Enabled</td>
<td>( C_L = 5 ) pF, From ( V_{OH} ): S1 Open, From ( V_{OL} ): S1 Closed</td>
<td>3.0 7.0 ns</td>
</tr>
<tr>
<td>( t_{PZXI} )</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>( C_L = 50 ) pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>3.0 7.0 ns</td>
</tr>
<tr>
<td>( t_{PXZI} )</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>( C_L = 5 ) pF, From ( V_{OH} ): S1 Open, From ( V_{OL} ): S1 Closed</td>
<td>3.0 7.0 ns</td>
</tr>
<tr>
<td>( t_{SKEW} )</td>
<td>Skew between Registered Outputs</td>
<td></td>
<td>1.0 ns</td>
</tr>
<tr>
<td>( t_{RESET} )</td>
<td>Power-Up to Registered Output High</td>
<td></td>
<td>1000 ns</td>
</tr>
</tbody>
</table>

### Test Load

- **Input:** 5V
- **Output:** 5V
- **Test Load Schematic of Inputs and Outputs**

\( R_1 = 200 \)
\( R_2 = 390 \)

---

**TL/L/9391–29**
Test Waveforms

Set-Up and Hold

CLOCK
DATA
INPUT
V_T
V_T
3V
0V
3V
0V

Propagation Delay

INPUT
IN-PHASE
OUTPUT
(S1 CLOSED)
3V
0V
V_T
V_T
V_T
V_T

OUT OF PHASE
OUTPUT
(S1 CLOSED)
3V
0V
V_T
V_T
V_T
V_T

Notes:
V_T = 1.5V
C_L includes probe and jig capacitance.
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms

Pulse Width

HIGH-LEVEL PULSE INPUT
V_T
V_T
3V
0V

LOW-LEVEL PULSE INPUT
V_T
V_T
3V
0V

Enable and Disable

ENABLING INPUT
V_T
ENABLE
V_T
DISABLE
3V
0V

NORMALLY HIGH OUTPUT
(S1 OPEN)
NORMALLY LOW OUTPUT
(S1 CLOSED)
Z
Z
0.5V
0.5V

Power-Up Reset Waveform

V_CC
5V
90%
V_RESET
V_OH
V_L
INTERNAL REGISTERS RESET TO LOGIC 0
V_H

*The clock input should not be switched from low to high until after time t_RESET.

TL/L/9391-3
TL/L/9391-4
TL/L/9391-5
TL/L/9391-6
TL/L/9391-7
TL/L/9391-8
TL/L/9391-9

2-38
Functional Description

All of the 20-pin Medium PAL logic arrays consist of 16 complementary input lines and 64 product-line terms with a programmable cell at each intersection (2048 cells). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

For the fuse-link PAL devices (all PAL devices excluding D and -7) an unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. In the National Series-D/-7 vertical fuse PAL devices, a programmed vertical fuse cell establishes a connection between an input line and a product term. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses for the fuse-link devices, or by programming the corresponding cells for the vertical fuse devices) are in the high logic state. Therefore, if both the true and complement of at least one array input is connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed fuse-link device). Conversely, if all input lines are disconnected from a product line, the product term and the resulting logic function would be held in the high state (which is the state of all product terms in an unprogrammed PAL device).

The medium PAL family consists of four device types with differing mixtures of combinational and registered outputs. The 16L8, 16R4, 16R6 and 16R8 architectures have 0, 4, 6 and 8 registered outputs, respectively, with the balance of the 8 outputs combinational. All outputs are active-low and have TRI-STATE capability.

Each combinational output has a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinational output is enabled while the TRI-STATE product term is satisfied (true). Combinational outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 16L8). This allows a pin to perform bidirectional I/O or, if the associated TRI-STATE control product term were programmed to remain unsatisfied (always false), the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable (G) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

Series-D/-7 Medium PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

For the National Series-D/-7 PAL device, during power-up, all outputs are held in the high-impedance state until DC power supply conditions are met (VCC approximately 3.0V), after which they may be enabled by the TRI-STATE control product terms (combinational outputs) or the G pin (registered outputs). Whenever VCC goes below 3V (at 25°C), the outputs are disabled as shown in Figure 1 below.

Note: t2 is less than 100 ns.

**FIGURE 1. Series-D Power-Up TRI-STATE Waveform**

In an unprogrammed National Series-D/-7 PAL device, no array inputs are connected to any product-term lines. Therefore, all combinational outputs would be enabled and driving low logic levels (after power-up is completed). All registers would still initialize to the low state, but would become permanently set (low-level outputs, if enabled) following the first clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, VIL, VOH, or resistively to VCC. However, switching any input not connected to a product term or logic function has no effect on its output logic state.
20-Pin Medium PAL Family Block Diagrams—DIP Connections

PAL16L8

PAL16R4

PAL16R6

PAL16R8
20-Lead PLCC Connection Conversion Diagram

20-PIN DIP PIN NUMBERS

20-LEAD PLCC (TOP VIEW)

Typical Registered Logic Function Without Feedback
**Functional Description (Continued)**

**CLOCK FREQUENCY SPECIFICATION**

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_W high + t_W low) and the minimum “data window” period (t_{SU} + t_{DH}). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

**Output Register Preload**

In the 20-pin Medium PAL family, register preload is available on the Series-Of-7 PAL devices only.

The output register preload feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The preload function allows the register to be loaded directly and asynchronously with any desired pattern. These vertical-fuse devices provide two register preload operations:

1. All registers can be reset to the low state (high-level outputs) by applying the elevated control voltage (V_Z) to input Pin 2* for time t_D (Figure 2a).
2. Selected registers can be set to the high state (low-level outputs) as follows (Figure 2b):
   a. All registered outputs are disabled by raising the input Pin 1* to V_H.
   b. After time t_D, the selected registered output pins are raised to the elevated control voltage (V_Z) for time t_D to set the corresponding registers.

*Applies to both DIP and PCC packages for 20-pin PAL devices.

---

**FIGURE 2. Series-D Register Preload Waveforms**

Note: V_Z = 9.5V to 10.0V, t_D min. = 500 ns.
Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be downloaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

In National Series-D/7 PAL devices, logical and physical connections between array input lines and product-term lines are established when vertical fuse cells are programmed. This is opposed to other PAL products based on fusible links in which connections are established when fuses are left unprogrammed (intact). This difference is compensated by the vertical-fuse PAL programming algorithm so that the user's design development process looks the same. (The only functional difference due to vertical-fuse technology is the behavior of "unprogrammed" devices.) The JEDEC programming maps produced by PAL development software for all Medium PAL devices denote a "connection" with a "0", and a "non-connection" with a "1". The programming algorithms for most fuse-link PLDs program fuses where zeroes are located in the map to remove corresponding connections, whereas the algorithm for National Series-D PAL products automatically compensates by programming vertical-fuse cells where zeroes are located in the map to establish connections. Therefore, the same JEDEC map representing the user's desired logic equations produces the same functional results when using either PAL technology. The user need only provide the appropriate device code and/or adapter for the programming equipment to invoke the proper programming algorithm. Only programmers with the certified National Series-D/7 vertical-fuse PAL programming algorithm can be used to program these vertical-fuse devices.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 20-pin Medium PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Ordering Information

<table>
<thead>
<tr>
<th>Programmable Array Logic Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Array Inputs</td>
</tr>
<tr>
<td>Output Type:</td>
</tr>
<tr>
<td>H = Active High</td>
</tr>
<tr>
<td>L = Active Low</td>
</tr>
<tr>
<td>C = Complementary</td>
</tr>
<tr>
<td>R = Registered</td>
</tr>
<tr>
<td>X = Exclusive-OR Registered</td>
</tr>
<tr>
<td>P = Programmable Polarity</td>
</tr>
<tr>
<td>Number of Registered Outputs (or total outputs if non-registered)</td>
</tr>
<tr>
<td>Speed/Power Version:</td>
</tr>
<tr>
<td>No Symbol = 35 ns</td>
</tr>
<tr>
<td>A = 25 ns</td>
</tr>
<tr>
<td>A2 = 35 ns, Half Power</td>
</tr>
<tr>
<td>B = 15 ns</td>
</tr>
<tr>
<td>B2 = 25 ns, Half Power</td>
</tr>
<tr>
<td>D = 10 ns</td>
</tr>
<tr>
<td>-7 = 7 ns</td>
</tr>
<tr>
<td>Package Type:</td>
</tr>
<tr>
<td>N = 20-Pin Plastic DIP</td>
</tr>
<tr>
<td>J = 20-Pin Ceramic DIP</td>
</tr>
<tr>
<td>V = 20-Lead Plastic Chip Carrier</td>
</tr>
<tr>
<td>Temperature Range:</td>
</tr>
<tr>
<td>C = Commercial (0°C to +75°C)</td>
</tr>
<tr>
<td>M = Military (-55°C to +125°C)</td>
</tr>
</tbody>
</table>
JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
Logic Diagram—PAL16R4

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
Logic Diagram—PAL16R6

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
Logic Diagram—PAL16R8

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
Programmable Array Logic (PAL®)
24-Pin Small PAL Family

General Description
The 24-pin Small PAL family contains six popular PAL architectures. The devices in the Small PAL family draw only 100 mA maximum supply current as compared to 210 mA in the 24-pin Medium PAL devices. These devices offer speeds as fast as 25 ns maximum propagation delay. National Semiconductor’s Schottky TTL process with titanium tungsten fusible links provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fusible links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

Device Types

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Dedicated Inputs</th>
<th>Combinatorial Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAL12L10</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>PAL14L8</td>
<td>14</td>
<td>8</td>
</tr>
<tr>
<td>PAL16L6</td>
<td>16</td>
<td>6</td>
</tr>
<tr>
<td>PAL18L4</td>
<td>18</td>
<td>4</td>
</tr>
<tr>
<td>PAL20L2</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>PAL20C1</td>
<td>20</td>
<td>1 Pair</td>
</tr>
</tbody>
</table>

Speed/Power Versions

<table>
<thead>
<tr>
<th>Series</th>
<th>Example</th>
<th>Commercial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>tpD</td>
<td>lcc</td>
</tr>
<tr>
<td>Standard</td>
<td>PAL12L10</td>
<td>40 ns</td>
<td>100 mA</td>
</tr>
<tr>
<td>A</td>
<td>PAL12L10A</td>
<td>25 ns*</td>
<td>100 mA</td>
</tr>
</tbody>
</table>

*Except PAL20C1A tpD = 30 ns Commercial, 35 ns Military.

The Small PAL logic array has between 12 and 20 complementary inputs and up to 10 combinatorial outputs generated by a single programmable AND-gate array with fixed OR-gate connections. The Small PAL family offers a variety of input/output combinations as shown in the Device Types table below. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features
- As fast as 25 ns maximum propagation delay
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment available
- Fully supported by National PLAN™ development software
- Security fuse prevents direct copying of logic patterns

Block Diagram—PAL12L10
**Standard Series** (PAL12L10, PAL14L8, PAL16L6, PAL18L4, PAL20L2, PAL20C1)

**Absolute Maximum Ratings** *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th></th>
<th></th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (<em>V</em>&lt;sub&gt;CC&lt;/sub&gt;) <em>(Note 2)</em></td>
<td></td>
<td></td>
<td>−0.5 to +7.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage <em>(Notes 2 and 3)</em></td>
<td></td>
<td></td>
<td>−1.5 to +5.5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Off-State Output Voltage <em>(Note 2)</em></td>
<td></td>
<td></td>
<td>−1.5 to +5.5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current <em>(Note 2)</em></td>
<td></td>
<td></td>
<td>−30.0 mA to +5.0 mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>V</em>&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Low Level Input Voltage <em>(Note 5)</em></td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><em>V</em>&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>High Level Input Voltage <em>(Note 5)</em></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>V</em>&lt;sub&gt;IC&lt;/sub&gt;</td>
<td>Input Clamp Voltage</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Min, <em>I</em> = −18 mA</td>
<td>−0.8</td>
<td>−1.5</td>
<td>V</td>
</tr>
<tr>
<td><em>I</em>&lt;sub&gt;L&lt;/sub&gt;</td>
<td>Low Level Input Current</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Max, <em>V</em>&lt;sub&gt;I&lt;/sub&gt; = 0.4V</td>
<td>−0.02</td>
<td>−0.25</td>
<td>mA</td>
</tr>
<tr>
<td><em>I</em>&lt;sub&gt;H&lt;/sub&gt;</td>
<td>High Level Input Current</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Max, <em>V</em>&lt;sub&gt;I&lt;/sub&gt; = 2.4V</td>
<td>25</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td><em>I</em></td>
<td>Maximum Input Current</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Max, <em>V</em>&lt;sub&gt;I&lt;/sub&gt; = 5.5V</td>
<td>1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><em>V</em>&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Low Level Output Voltage</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Min, <em>I</em>&lt;sub&gt;OL&lt;/sub&gt; = 8 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td><em>V</em>&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>High Level Output Voltage</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Min,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><em>I</em>&lt;sub&gt;OH&lt;/sub&gt; = −2 mA</td>
<td>MIL</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><em>I</em>&lt;sub&gt;OH&lt;/sub&gt; = −3.2 mA</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>I</em>&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Output Short-Circuit Current <em>(Note 6)</em></td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = 5V, <em>V</em>&lt;sub&gt;O&lt;/sub&gt; = 0V</td>
<td>−30</td>
<td>−70</td>
<td>−130</td>
</tr>
<tr>
<td><em>I</em>&lt;sub&gt;OC&lt;/sub&gt;</td>
<td>Supply Current</td>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt; = Max, Outputs Open</td>
<td>60</td>
<td>100</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Electrical Characteristics** *(Over Recommended Operating Conditions)* *(Note 4)*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>V</em>&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Supply Voltage</td>
<td></td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td><em>T</em>&lt;sub&gt;A&lt;/sub&gt;</td>
<td>Operating Free-Air Temperature</td>
<td></td>
<td>−55</td>
<td></td>
<td>0</td>
<td>75</td>
</tr>
<tr>
<td><em>T</em>&lt;sub&gt;C&lt;/sub&gt;</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td>125</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.
2. Some device pins may be raised above these limits during programming operations according to the applicable specification.
3. It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.
4. All typical values are for *V*<sub>CC</sub> = 5.0V and *T*<sub>A</sub> = 25°C.
5. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
6. To avoid Invalid readings in other parameter tests, it is preferable to conduct the *I*<sub>OS</sub> test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.
Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tpD</td>
<td>Input to Output</td>
<td>CL = 50 pF</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25</td>
<td>40</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Test Load**

![Test Load Diagram]

**Test Waveform**

![Test Waveform Diagram]

Notes:
- VT = 1.5V
- CL includes probe and jig capacitance.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

**Schematic of Inputs and Outputs**

![Schematic Diagram]
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_{CC}) (Note 2)</td>
<td>-0.5 to +7.0V</td>
<td>-0.5 to +7.0V</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>-1.5 to +5.5V</td>
<td>-1.5 to +5.5V</td>
<td>mA</td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>-1.5 to +5.5V</td>
<td>-1.5 to +5.5V</td>
<td>mA</td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>-30.0 mA to +5.0 mA</td>
<td>-30.0 mA to +5.0 mA</td>
<td>mA</td>
</tr>
<tr>
<td>Output Current (I_{OL})</td>
<td>+100 mA</td>
<td>+100 mA</td>
<td>mA</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>Supply Voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>T_{A}</td>
<td>Operating Free-Air Temperature</td>
<td>-55</td>
<td>0</td>
<td>75</td>
</tr>
<tr>
<td>T_{C}</td>
<td>Operating Case Temperature</td>
<td>125</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Conditions (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IL}</td>
<td>Low Level Input Voltage (Note 5)</td>
<td>V_{CC} = Min, I = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{IH}</td>
<td>High Level Input Voltage (Note 5)</td>
<td></td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{IC}</td>
<td>Input Clamp Voltage</td>
<td>V_{CC} = Max, V_{I} = 0.4V</td>
<td>-0.02</td>
<td>-0.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Low Level Input Current</td>
<td>V_{CC} = Max, V_{I} = 0.4V</td>
<td>25</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_{IH}</td>
<td>High Level Input Current</td>
<td>V_{CC} = Max, V_{I} = 5.5V</td>
<td>100</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Low Level Output Voltage</td>
<td>V_{CC} = Min, I_{OL} = 8 mA</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>High Level Output Voltage</td>
<td>V_{CC} = Min</td>
<td>I_{OH} = -2 mA</td>
<td>MIL</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I_{OH} = -3.2 mA</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OS}</td>
<td>Output Short-Circuit Current</td>
<td>V_{CC} = 5V, V_{O} = 0V</td>
<td>-30</td>
<td>-70</td>
<td>-130</td>
<td>mA</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Supply Current</td>
<td>V_{CC} = Max, Outputs Open</td>
<td>60</td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Note 1:** All typical values are for V_{CC} = 5.0V and T_{A} = 25°C.

**Note 5:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or test equipment noise. Do not attempt to test these values without suitable equipment.

**Note 6:** To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.
### Switching Characteristics

**Over Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Test Load</th>
<th>Test Waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{pd}$</td>
<td>Input to Output $C_L = 50$ pF</td>
<td>$12L10A, 14L8A, 16L6A, 18L4A, 20L2A, 20C1A$</td>
<td>$R_L &gt; 100$</td>
<td>Propagation Delay</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$R_L = 560$ $R_2 = 1.1k$</td>
<td>$V_T = 1.5V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_T = 1.5V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$C_L$ includes probe and jig capacitance.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.</td>
</tr>
</tbody>
</table>

---

### Notes:

- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
- $V_T = 1.5V$
24-Pin Small PAL Family Block Diagrams—DIP Connections (Continued)

28-Lead PLCC Connection Conversion Diagram

Note: For availability of old (NON-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor.
Functional Description
The 24-pin Small PAL logic arrays consist of between 12 and 20 complementary input lines and either 16 or 20 product-term lines with a programmable fuse link at each intersection (up to 720 fuses). The family consists of six device types with different numbers of combinatorial outputs. The 24-pin Small PAL Family Block Diagrams show the number of product terms allocated to each output for each device. All product terms allocated to each output connect into an OR-gate to produce the sum-of-products output logic function.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V<sub>OL</sub>, V<sub>OH</sub>, or resistive-ly to V<sub>CC</sub>. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

Security Fuse
Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses.

Design Development Support
A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLANTM software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Small PAL family are provided for direct map editing and diagnostic purposes. Contact your local National Semiconductor sales representative or distributor for a list of current software and programming support tools available for these devices. Contact the National Semiconductor Programmable Device Support Department if detailed specifications of PAL programming algorithms are needed.

Ordering Information

<table>
<thead>
<tr>
<th>Programmable Array Logic Family</th>
<th>Number of Array Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Type:</td>
<td></td>
</tr>
<tr>
<td>H = Active High</td>
<td></td>
</tr>
<tr>
<td>L = Active Low</td>
<td></td>
</tr>
<tr>
<td>C = Complementary</td>
<td></td>
</tr>
<tr>
<td>R = Registered</td>
<td></td>
</tr>
<tr>
<td>X = Exclusive-OR Registered</td>
<td></td>
</tr>
<tr>
<td>P = Programmable Polarity</td>
<td></td>
</tr>
<tr>
<td>Number of Outputs</td>
<td></td>
</tr>
<tr>
<td>Speed Version:</td>
<td></td>
</tr>
<tr>
<td>No Symbol = 40 ns</td>
<td></td>
</tr>
<tr>
<td>A = 25 ns</td>
<td></td>
</tr>
<tr>
<td>Package Type:</td>
<td></td>
</tr>
<tr>
<td>N = 24-Pin Plastic DIP</td>
<td></td>
</tr>
<tr>
<td>J = 24-Pin Ceramic DIP</td>
<td></td>
</tr>
<tr>
<td>V = 28-Lead Plastic Chip Carrier</td>
<td></td>
</tr>
<tr>
<td>Temperature Range:</td>
<td></td>
</tr>
<tr>
<td>C = Commercial (0°C to +75°C)</td>
<td></td>
</tr>
<tr>
<td>M = Military (-55°C to +125°C)</td>
<td></td>
</tr>
</tbody>
</table>
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL14L8

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL 18L4

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL20C1

Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Programmable Array Logic (PAL®)
24-Pin Exclusive-OR PAL Family

General Description
The 24-pin Exclusive-OR PAL family contains four industry-standard PAL architectures optimized for a specific class of applications. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fusible links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL logic array has a total of 20 complementary inputs and 10 outputs generated by a single programmable AND-gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passed through exclusive-OR gates and D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. The exclusive-OR functions provide easy implementation of the "hold" operation used in counters and other state sequences. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The exclusive-OR PAL family offers a variety of combinatorial and registered output mixtures, as shown in the Device Types table below.

Series-A devices have power-up reset and register preload features available. On power-up, all registers are reset to simplify sequential circuit design and testing. Direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features
- As fast as 30 ns maximum propagation delay (combinatorial)
- Exclusive-OR function facilitates design of counters and state sequences
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLANTM development software
- Power-up reset for registered outputs (Series-A)
- Register preload facilitates device testing (Series-A)
- Security fuse prevents direct copying of logic patterns

<table>
<thead>
<tr>
<th>Device Types</th>
<th>Registered Outputs (With Feedback)</th>
<th>Combinatorial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Type</td>
<td>Dedicated Inputs</td>
<td>I/Os</td>
</tr>
<tr>
<td>PAL20L10</td>
<td>14</td>
<td>6</td>
</tr>
<tr>
<td>PAL20X4</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>PAL20X8</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>PAL20X10</td>
<td>12</td>
<td>8</td>
</tr>
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</table>

Speed/Power Versions
<table>
<thead>
<tr>
<th>Series</th>
<th>Example</th>
<th>Commercial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>tpD</td>
<td>ICC</td>
<td>tpD</td>
</tr>
<tr>
<td>Standard</td>
<td>PAL20L10</td>
<td>50 ns</td>
<td>165 mA</td>
</tr>
<tr>
<td></td>
<td>PAL20L10A</td>
<td>30 ns</td>
<td>165 mA</td>
</tr>
</tbody>
</table>

Block Diagram—PAL20X10
## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage ($V_{CC}$) (Note 2): $-0.5V$ to $+7.0V$
- Input Voltage (Notes 2 and 3): $-1.5V$ to $+5.5V$
- Off-State Output Voltage (Note 2): $-1.5V$ to $+5.5V$
- Input Current (Note 2): $-30mA$ to $+5.0mA$
- Output Current ($I_{OL}$): $+100mA$
- Storage Temperature: $-65°C$ to $+150°C$
- Ambient Temperature with Power Applied: $-65°C$ to $+125°C$
- Junction Temperature: $-65°C$ to $+150°C$

## Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$T_{A}$</td>
<td>Operating Free-Air Temperature</td>
<td>$T_{A}$</td>
<td>-55</td>
<td></td>
<td>0</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{C}$</td>
<td>Operating Case Temperature</td>
<td>$T_{C}$</td>
<td>125</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$I_{W}$</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>40</td>
<td>20</td>
<td>35</td>
<td>20 ns</td>
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<tr>
<td></td>
<td></td>
<td>High</td>
<td>30</td>
<td>10</td>
<td>25</td>
<td>10 ns</td>
</tr>
<tr>
<td>$I_{SU}$</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>$I_{SU}$</td>
<td>60</td>
<td>38</td>
<td>50</td>
<td>38 ns</td>
</tr>
<tr>
<td>$I_{H}$</td>
<td>Hold Time of Input after Clock</td>
<td>$I_{H}$</td>
<td>0</td>
<td>-15</td>
<td>0</td>
<td>-15 ns</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 4)</td>
<td>$f_{CLK}$</td>
<td>17.2</td>
<td>10.0</td>
<td>17.2</td>
<td>12.5 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>33.3</td>
<td>14.3</td>
<td>33.3</td>
<td>16.7 MHz</td>
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## Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>$V_{CC}$</td>
<td>$I_{OL} = 12mA$</td>
<td>MIL</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage (Note 6)</td>
<td>$V_{CC}$</td>
<td>$I_{OH} = -2mA$</td>
<td>MIL</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Input Clamp Voltage</td>
<td>$V_{CC}$ = Min,</td>
<td>0.8</td>
<td>-</td>
<td>-1.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current (Note 7)</td>
<td>$V_{CC}$ = Max,</td>
<td>$I_{IL} = 0.4mA$</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current (Note 7)</td>
<td>$V_{CC}$ = Max,</td>
<td>$I_{IH} = 2.4mA$</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Maximum Input Current</td>
<td>$V_{CC}$ = Max,</td>
<td>$I_{I} = 5.5V$</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC}$</td>
<td>$I_{OL} = 24mA$</td>
<td>COM</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC}$</td>
<td>$I_{OH} = -3.2mA$</td>
<td>COM</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>$V_{CC}$ = Max</td>
<td>$V_{O} = 0.4V$</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>$V_{CC}$ = Max</td>
<td>$V_{O} = 2.4V$</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>$V_{CC}$ = 5V,</td>
<td>$V_{O} = 0V$</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC}$ = Max,</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Outputs Open</td>
<td>$V_{CC}$ = Max,</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>
Standard Series (PAL20L10, PAL20X4, PAL20X8, PAL20X10) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: t CLK with feedback is derived as (t CLK + t <sub>FU</sub>)<sup>-1</sup>. 

Note 5: All typical values are for V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between I<sub>HI</sub> and I<sub>L</sub> or between I<sub>H</sub> and I<sub>L</sub>.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the I<sub>Q</sub> test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>t PD</td>
<td>Input or Feedback to</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, S1 Closed</td>
<td>35</td>
<td>60</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>Combinatorial Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t CLK</td>
<td>Clock to Registered</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, S1 Closed</td>
<td>20</td>
<td>40</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>Output or Feedback</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t PZXG</td>
<td>G Pin to Registered</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>20</td>
<td>45</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>Output Enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t PXG</td>
<td>G Pin to Registered</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 5 pF, from V&lt;sub&gt;OH&lt;/sub&gt;: S1 Open, from V&lt;sub&gt;OL&lt;/sub&gt;: S1 Closed</td>
<td>20</td>
<td>45</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>Output Disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t PXI</td>
<td>Input to Combinatorial Output</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>35</td>
<td>55</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>Enabled via Product Term</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t PXI</td>
<td>Input to Combinatorial Output</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 5 pF, from V&lt;sub&gt;OH&lt;/sub&gt;: S1 Open, from V&lt;sub&gt;OL&lt;/sub&gt;: S1 Closed</td>
<td>35</td>
<td>55</td>
<td>35</td>
</tr>
</tbody>
</table>

Test Load

Schematic of Inputs and Outputs

MIL COM'L
R1 = 390 R1 = 200
R2 = 750 R2 = 390

TL/L/9998-2

2-64
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Supply Voltage** (VCC) (Note 2): \(-0.5\text{V} \text{ to } +7.0\text{V}\)
- **Input Voltage** (Note 2): \(-1.5\text{V} \text{ to } +5.5\text{V}\)
- **Off-State Output Voltage** (Note 2): \(-1.5\text{V} \text{ to } +5.5\text{V}\)
- **Input Current** (Note 2): \(-30\text{ mA} \text{ to } +5.0\text{ mA}\)
- **Output Current** (IOL): \(+100\text{ mA}\)

<table>
<thead>
<tr>
<th>Absolute Maximum Ratings</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature</td>
<td>(-65^\circ\text{C} \text{ to } +150^\circ\text{C})</td>
</tr>
<tr>
<td>Ambient Temperature with Power Applied</td>
<td>(-65^\circ\text{C} \text{ to } +125^\circ\text{C})</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>(-65^\circ\text{C} \text{ to } +150^\circ\text{C})</td>
</tr>
<tr>
<td>ESD Tolerance (Note 3)</td>
<td>(2000\text{V})</td>
</tr>
<tr>
<td>Test Method: Human Body Model</td>
<td></td>
</tr>
<tr>
<td>Test Specification: NSC SOP-5-028</td>
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### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>Min: 4.5</td>
<td>Nom: 5</td>
<td>Max: 5.5</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>Min: (-55^\circ\text{C})</td>
<td>Nom: 0</td>
<td>Max: 75</td>
</tr>
<tr>
<td>TC</td>
<td>Operating Case Temperature</td>
<td>Min: 125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width</td>
<td>Low: 35</td>
<td>Nom: 15</td>
<td>Max: 25</td>
</tr>
<tr>
<td>tSU</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>Low: 20</td>
<td>Nom: 7</td>
<td>Max: 15</td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time of Input after Clock</td>
<td>Min: 0</td>
<td>Nom: (-15\text{ ns})</td>
<td>Max: 0</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback: 15.4</td>
<td>Nom: 22.2</td>
<td>Max: 25.0</td>
</tr>
<tr>
<td></td>
<td>Without Feedback</td>
<td>18.2</td>
<td></td>
<td></td>
</tr>
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</table>

### Electrical Characteristics

**Over Recommended Operating Conditions (Note 5)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>VCC = Min, I = (-18\text{ mA})</td>
<td>(-0.8\text{ V})</td>
<td>(-1.5\text{ V})</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High Level Input Voltage (Note 6)</td>
<td>VCC = Max, VI = 0.4V</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIC</td>
<td>Input Clamp Voltage</td>
<td>VCC = Min, V = (-18\text{ mA})</td>
<td>(-0.8\text{ V})</td>
<td>(-1.5\text{ V})</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Low Level Input Current (Note 7)</td>
<td>VCC = Max, VI = 2.4V</td>
<td>25</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current (Note 7)</td>
<td>VCC = Max, VI = 5.5V</td>
<td>100</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>Ii</td>
<td>Maximum Input Current</td>
<td>VCC = Min, VI = (-18\text{ mA})</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min, I = 12 mA</td>
<td>MIL</td>
<td>2.4</td>
<td>2.9</td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min, I = (-2\text{ mA})</td>
<td>MIL</td>
<td>2.4</td>
<td>2.9</td>
</tr>
<tr>
<td>I0ZL</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>VCC = Max, V = 0.4V</td>
<td>(-100\text{ (\mu\text{A})}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I0ZH</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>VCC = Max, V = 2.4V</td>
<td>100</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>IOS</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>VCC = 5V, V = 0V</td>
<td>(-100\text{ (\mu\text{A})}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>VCC = Max, Outputs Open</td>
<td>20L10A</td>
<td>115</td>
<td>165</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20X4A, 20X8A, 20X10A</td>
<td>135</td>
<td>180</td>
<td></td>
</tr>
</tbody>
</table>
Series—A (PAL20L10A, PAL20X4A, PAL20X8A, PAL20X10A) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: fCLK with feedback is derived as (fCLK + tSU)⁻¹. fCLK without feedback is derived as (tWLOW + tWHIGH)⁻¹.

Note 5: All typical values are for VCC = 5.0V and TA = 25°C.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between IIL and IOZL or between IH and IOZH.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the ICS test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>CL = 50 pF, S1 Closed</td>
<td>23 35 ns</td>
<td>23 30 ns</td>
<td></td>
</tr>
<tr>
<td>tCLK</td>
<td>Clock to Registered Output or Feedback</td>
<td>CL = 50 pF, S1 Closed</td>
<td>10 25 ns</td>
<td>10 15 ns</td>
<td></td>
</tr>
<tr>
<td>tPZXG</td>
<td>G Pin to Registered Output Enabled</td>
<td>CL = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>11 25 ns</td>
<td>11 20 ns</td>
<td></td>
</tr>
<tr>
<td>tPXZG</td>
<td>G Pin to Registered Output Disabled</td>
<td>CL = 50 pF, S1 Closed, from VOH: S1 Open, from VOL: S1 Closed</td>
<td>10 25 ns</td>
<td>10 20 ns</td>
<td></td>
</tr>
<tr>
<td>tPZXI</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>CL = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>19 35 ns</td>
<td>19 30 ns</td>
<td></td>
</tr>
<tr>
<td>tPXZI</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>CL = 50 pF, S1 Closed, from VOH: S1 Open, from VOL: S1 Closed</td>
<td>15 35 ns</td>
<td>15 30 ns</td>
<td></td>
</tr>
<tr>
<td>tRESET</td>
<td>Power-Up to Registered Output High</td>
<td></td>
<td>600 1000 ns</td>
<td>600 1000 ns</td>
<td></td>
</tr>
</tbody>
</table>

Test Load

Schematic of Inputs and Outputs
Test Waveforms

Set-Up and Hold

CLOCK
DATA INPUT

Propagation Delay

INPUT
IN-PHASE OUTPUT (S1 CLOSED)
OUT OF PHASE OUTPUT (S1 CLOSED)

Notes:

VT = 1.5V
Cf includes probe and jig capacitance.
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms

Enable and Disable

Notes:

Enable ENABLING INPUT
Disable NORMAL HIGH OUTPUT (S1 OPEN)
NORMAL LOW OUTPUT (S1 CLOSED)

Power-Up Reset Waveform (Series-A only)

*The clock input should not be switched from low to high until after time t_RESET.*

TL/L/9998-9
Functional Description

All of the 24-pin Exclusive-OR PAL logic arrays consist of 20 complementary input lines and 40 product-term lines with a programmable fuse link at each intersection (1600 fuses). The product terms are organized into ten groups of four each. Three or four of the product terms in each group connect into OR-gates to produce the output logic function, depending on whether the output is combinatorial or registered.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term would be held in the high state.

The exclusive-OR PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20L10, 20X4, 20X8 and 20X10 architectures have 0, 4, 8 and 10 registered outputs, respectively, with the balance of the 10 outputs combinational. All outputs are active-low and have TRI-STATE capability.

Each combinatorial output has a three product-term logic function, with the fourth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20L10). This allows a pin to perform bidirectional I/O or, if the associated logic function were left unprogrammed, the output driver would remain disabled and the pin could be used as an additional dedicated input.

For the registered outputs, the groups of the four product terms are segmented into two OR-sums of two product terms each; which are then combined by an exclusive-OR gate at the input of the D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable (G) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

The 24-pin Exclusive-OR PAL Series-A devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, VOL, VOH, or resistively to VCC. However, switching any input not connected to a product term or logic function has no effect on its output logic state.
24-Pin Exclusive-OR PAL Family Block Diagrams—DIP Connections

PAL20L10

PAL20X4

PAL20X8

PAL20X10
For availability of old (Non-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor. PAL20L10 (Standard Series) is not available in the JEDEC pinout shown above.
Functional Description (Continued)

CLOCK FREQUENCY SPECIFICATION

The clock frequency (fCLK) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (fCLK−1 without feedback) is defined as the greater of the minimum clock period (tw high + tw low) and the minimum "data window" period (tsu + tH). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (fCLK−1 with feedback) is defined as tCLK + tsu. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the outputs at the registers before the end of each cycle.

Output Register Preload (Series-A)

The preload function allows the registers to be loaded asynchronously from data placed on the output pins. This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The register preload procedure is as follows:

1. VCC is raised to 4.5V.
2. Registered outputs are disabled by raising output enable (G) to VHH.
3. The desired data values are applied to all registered output pins (VIL = set, VIH = reset).
4. DIP pin 10 (PCC pin 12) is pulsed to VP, then back to VIL. (VP = 18.0V ± 0.5V).

5. Data inputs are removed from registered output pins.
6. G is lowered to VIL to enable registered outputs.
7. The desired data values are verified at all registered outputs (VOL = Set, VOH = Reset).

Note: The minimum recommended time delay (tD) between successive input transitions (including the VP pulse width on DIP pin 8) is 100 ns.

Security Fuse

Security fuses are provided on all 24-pin Exclusive-OR PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Exclusive-OR PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.
Ordering Information
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

Programmable Array Logic Family

Number of Array Inputs

Output Type:
H = Active High
L = Active Low
C = Complementary
R = Registered
X = Exclusive-OR Registered
P = Programmable Polarity

Number of Registered Outputs (or total outputs if non-registered)

Speed/Power Version:
No Symbol = 50 ns
A = 30 ns

Package Type:
N = 24-Pin Plastic DIP
J = 24-Pin Ceramic DIP
V = 28-Lead Plastic Chip Carrier JEDEC Standard Pinout*
XV = 28-Lead PLCC Non-JEDEC Standard Pinout*

Temperature Range:
C = Commercial (0°C to +75°C)
M = Military (−55°C to +125°C)

*For availability of PAL20L10 in PLCC package, please contact your sales office.
Logic Diagram PAL20L10

DIP PIN NUMBERS
PRODUCT LINE FIRST FUSE NUMBERS

INPUT LINE NUMBERS

DIP PIN NUMBERS

VCC

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL20X8

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Logic Diagram PAL20X10

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
Programmable Array Logic (PAL®)
24-Pin Medium PAL Family

General Description

The 24-pin Medium PAL family contains four of the most popular PAL architectures with speeds as fast as 10 ns maximum propagation delay. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the Series A and Series B devices. Series D devices are manufactured using National Semiconductor's isoplanar "FAST-Z" TTL process with highly reliable "vertical-fuse" programmable cells. Vertical fuses are implemented using avalanche-induced migration ("AIM") technology offering very high programming yields and is an extension of National's FAST® logic family. The 24-pin Medium PAL family provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL logic array has a total of 20 complementary input pairs and 8 outputs generated by a single programmable AND-gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passed through D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The medium PAL family offers a variety of combinatorial and registered output mixes, as shown in the Device Types table below.

On power-up, Series-D devices reset all registers to simplify sequential circuit design and testing and for Series B devices, the registers are set on power-up. For Series D and Series B devices, direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- As fast as 10 ns maximum propagation delay (combinatorial)
- User-programmable replacement for TTL logic
- High programming yield and reliability of vertical-fuse technology for Series D products. (Programming equipment with certified vertical-fuse algorithm required)
- Extension of FAST product line (Series-D).
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLAN™ software
- Power-up set/reset for registered outputs (Series-B, D)
- Register preload facilitates device testing (Series-B, D)
- Security fuse prevents direct copying of logic patterns

Device Types

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Dedicated Inputs</th>
<th>Registered Outputs (With Feedback)</th>
<th>Combinatorial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>I/Os</td>
<td>Outputs</td>
</tr>
<tr>
<td>PAL20L8</td>
<td>14</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td>PAL20R4</td>
<td>12</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>PAL20R6</td>
<td>12</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>PAL20R8</td>
<td>12</td>
<td>8</td>
<td></td>
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</table>

Speed/Power Versions

<table>
<thead>
<tr>
<th>Series</th>
<th>Example</th>
<th>Commercial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>tpD</td>
<td>ICC</td>
</tr>
<tr>
<td>A</td>
<td>PAL 20L8A</td>
<td>25 ns</td>
<td>210 mA</td>
</tr>
<tr>
<td>B</td>
<td>PAL 20L8B</td>
<td>15 ns</td>
<td>210 mA</td>
</tr>
<tr>
<td>D</td>
<td>PAL20L8D</td>
<td>10 ns</td>
<td>210 mA</td>
</tr>
</tbody>
</table>

Block Diagram—PAL20R8
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage ($V_{CC}$) (Note 2): –0.5V to +7.0V
- Input Voltage (Note 2): –1.5V to +5.5V
- Off-State Output Voltage (Note 2): –1.5V to +5.5V
- Input Current (Note 2): –30 mA to +5.0 mA
- Output Current ($I_{OL}$): +100 mA

#### Storage Temperature
- –65°C to +150°C

#### Ambient Temperature with Power Applied
- –65°C to +125°C

#### Junction Temperature
- –65°C to +150°C

#### ESD Tolerance (Note 3)
- C$\textit{ZAP} = 100 \text{ pF}$
- R$\textit{ZAP} = 1500 \Omega$

Test Method: Human Body Model

Test Specification: NSC SOP-5-028

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td></td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td></td>
<td>55</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>$T_C$</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td>125</td>
<td></td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>20</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
<td>20</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td></td>
<td>30</td>
<td>18</td>
<td>25</td>
</tr>
<tr>
<td>$t_H$</td>
<td>Hold Time of Input after Clock</td>
<td></td>
<td>0</td>
<td>–10</td>
<td>0</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency</td>
<td>With Feedback</td>
<td>20</td>
<td></td>
<td>28.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback</td>
<td></td>
<td>25</td>
<td></td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage (Note 6)</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Input Clamp Voltage</td>
<td>$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$</td>
<td>–0.8</td>
<td>–1.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current (Note 7)</td>
<td>$V_{CC} = \text{Max}, V_I = 0.4V$</td>
<td>–0.02</td>
<td>–0.25</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current (Note 7)</td>
<td>$V_{CC} = \text{Max}, V_I = 2.4V$</td>
<td>25</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max}, V_I = 5.5V$</td>
<td>100</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_{OL} = 12 \text{ mA}$</td>
<td>MIL</td>
<td>0.3</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OL} = 24 \text{ mA}$</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_{OH} = -2 \text{ mA}$</td>
<td>MIL</td>
<td>2.4</td>
<td>3.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OH} = -3.2 \text{ mA}$</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_O = 0.4V$</td>
<td></td>
<td></td>
<td>–100</td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_O = 2.4V$</td>
<td></td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>$V_{CC} = 5V, V_O = 0V$</td>
<td></td>
<td></td>
<td>–30</td>
<td>–70</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC} = \text{Max}, \text{Outputs Open}$</td>
<td></td>
<td></td>
<td>160</td>
<td>210</td>
</tr>
</tbody>
</table>
Series A (PAL20L8A, PAL20R4A, PAL20R6A, PAL20R8A) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: \( f_{CLK} \) with feedback is derived as \( \left( I_{O_{LK}} + I_{O_{UL}} \right)^{-1} \).

Note 5: All typical values are for \( V_{CC} = 5.0 \text{V} \) and \( T_A = 25^\circ \text{C} \).

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between \( I_{IL} \) and \( I_{0L} \) or between \( I_{OH} \) and \( I_{OZH} \).

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the \( I_{OZH} \) test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>( t_{PD} )</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>( C_L = 50 \mu \text{F}, S_1 ) Closed</td>
<td>18</td>
<td>30</td>
<td>25</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>Clock to Registered Output or Feedback</td>
<td>( C_L = 50 \mu \text{F}, S_1 ) Closed</td>
<td>12</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td>( t_{PZXG} )</td>
<td>( G ) Pin to Registered Output Enabled</td>
<td>( C_L = 50 \mu \text{F}, ) Active High: ( S_1 ) Open, Active Low: ( S_1 ) Closed</td>
<td>10</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>( t_{PXZG} )</td>
<td>( G ) Pin to Registered Output Disabled</td>
<td>( C_L = 5 \mu \text{F}, ) From ( V_{OH}: S_1 ) Open, From ( V_{OL}: S_1 ) Closed</td>
<td>11</td>
<td>25</td>
<td>11</td>
</tr>
<tr>
<td>( t_{PZXI} )</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>( C_L = 50 \mu \text{F}, ) Active High: ( S_1 ) Open, Active Low: ( S_1 ) Closed</td>
<td>10</td>
<td>30</td>
<td>10</td>
</tr>
<tr>
<td>( t_{PXZI} )</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>( C_L = 5 \mu \text{F}, ) From ( V_{OH}: S_1 ) Open, From ( V_{OL}: S_1 ) Closed</td>
<td>13</td>
<td>30</td>
<td>13</td>
</tr>
</tbody>
</table>

### Test Load

![Test Load Schematic](image1)

### Schematic of Inputs and Outputs

![Schematic of Inputs and Outputs](image2)
### Series B (PAL20L6B, PAL20R4B, PAL20R6B, PAL20R8B)

#### Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ($V_{CC}$) (Note 2)</td>
<td>$-0.5$ to $+7.0$ V</td>
<td>$-1.5$ to $+5.5$ V</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>$-1.5$ to $+5.5$ V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>$-1.5$ to $+5.5$ V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current (Note 2)</td>
<td>$-30$ mA to $+5.0$ mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Current ($I_{OL}$)</td>
<td>$+100$ mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Storage Temperature: $-65°C$ to $+150°C$
Ambient Temperature: $-65°C$ to $+125°C$
Junction Temperature: $-65°C$ to $+150°C$

ESD Tolerance (Note 3): $C_{ZAP} = 100$ pF
$R_{ZAP} = 1500$ Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

#### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>$4.5$</td>
<td>$5$</td>
<td>$5.5$</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td>$-55$</td>
<td>0</td>
<td>$75$</td>
</tr>
<tr>
<td>$T_C$</td>
<td>Operating Case Temperature</td>
<td>$125$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock Pulse Width</td>
<td>Low $12$</td>
<td>$8$</td>
<td>$10$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High $12$</td>
<td>$8$</td>
<td>$10$</td>
</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>$20$</td>
<td>$10$</td>
<td>$15$</td>
</tr>
<tr>
<td>$t_{H}$</td>
<td>Hold Time of Input after Clock</td>
<td>0</td>
<td>$-5$</td>
<td>0</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback $28.5$</td>
<td></td>
<td>$37$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback $41.7$</td>
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<td>$50$</td>
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#### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>$V_{CC} = \text{Min}, V_i = -18$ mA</td>
<td>$0.8$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage (Note 6)</td>
<td>$V_{CC} = \text{Max}, V_i = 0.4$ V</td>
<td>$2$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Input Clamp Voltage</td>
<td>$V_{CC} = \text{Min}, V_i = 0.4$ V</td>
<td>$2.4$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current (Note 7)</td>
<td>$V_{CC} = \text{Max}, V_i = 0.4$ V</td>
<td>$25$</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current (Note 7)</td>
<td>$V_{CC} = \text{Max}, V_i = 5.5$ V</td>
<td>$100$</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max}, V_i = 5.5$ V</td>
<td>$100$</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_{OL} = 12$ mA</td>
<td>MIL</td>
<td>$0.3$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OL} = 24$ mA</td>
<td>COM</td>
<td>$0.5$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_{OH} = -2$ mA</td>
<td>MIL</td>
<td>$2.4$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{OH} = -3.2$ mA</td>
<td>COM</td>
<td>$3.4$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_O = 0.4$ V</td>
<td>$-100$</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_O = 2.4$ V</td>
<td>$100$</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>$V_{CC} = 5$ V, $V_O = 0$ V</td>
<td>$-30$</td>
<td>$-70$</td>
<td>$-130$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC} = \text{Max}, \text{Outputs Open}$</td>
<td>$160$</td>
<td>$210$</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
**Series B (PAL20L6B, PAL20R4B, PAL20R6B, PAL20R8B) (Continued)**

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

**Note 4:** \( f_{CLK} \) with feedback is derived as \( \frac{1}{(C_{CLK} + \beta_{f})} \).

\( f_{CLK} \) without feedback is derived as \( \frac{1}{2t_{W}} \).

**Note 5:** All typical values are for \( V_{CC} = 5.0 \text{V} \) and \( T_{A} = 25^\circ\text{C} \).

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Note 7:** Leakage current for bidirectional I/O pins is the worst case between \( I_{IL} \) and \( I_{OL} \) or between \( I_{IH} \) and \( I_{OH} \).

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the \( I_{PS} \) test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>( C_{L} = 50 \text{pF}, S1 \text{ Closed} )</td>
<td>Min Typ Max</td>
<td>Min Typ Max</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>Clock to Registered Output or Feedback</td>
<td>( C_{L} = 50 \text{pF}, S1 \text{ Closed} )</td>
<td>8 15</td>
<td>8 12</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PZXG} )</td>
<td>( \bar{G} ) Pin to Registered Output Enabled</td>
<td>( C_{L} = 50 \text{pF}, \text{Active High: S1 Open, Active Low: S1 Closed} )</td>
<td>10 20</td>
<td>10 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PXZG} )</td>
<td>( \bar{G} ) Pin to Registered Output Disabled</td>
<td>( C_{L} = 5 \text{pF}, \text{From VOH: S1 Open, From VOL: S1 Closed} )</td>
<td>8 20</td>
<td>8 12</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PXZI} )</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>( C_{L} = 50 \text{pF}, \text{Active High: S1 Open, Active Low: S1 Closed} )</td>
<td>11 20</td>
<td>11 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PXZI} )</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>( C_{L} = 5 \text{pF}, \text{From VOH: S1 Open, From VOL: S1 Closed} )</td>
<td>11 20</td>
<td>11 15</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SET} )</td>
<td>Power-Up to Registered Output Low</td>
<td></td>
<td>600 1000</td>
<td>600 1000</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Test Load

![Test Load Schematic](image)

**Schematic of Inputs and Outputs**

![Schematic](image)
## Series D (PAL20L8D, PAL20R4D, PAL20R6D, PAL20R8D)

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Supply Voltage** ($V_{CC}$) (Note 2) $-0.5V$ to $+7.0V$
- **Input Voltage** (Note 2) $-1.5V$ to $+7.0V$
- **Off-State Output Voltage** ($V_O$) (Notes 2 & 3) $-1.5V$ to $+5.5V$
- **Input Current** (Note 2) $-30mA$ to $+5.0mA$
- **Output Current** ($I_{OL}$) $+100mA$

**Storage Temperature** $-65°C$ to $+150°C$

**Ambient Temperature with Power Applied** $-65°C$ to $+125°C$

**Junction Temperature** $-65°C$ to $+150°C$

**ESD Tolerance** $2000V$

- **$C_{ZAP} = 100 \text{ pF}$**
- **$R_{ZAP} = 1500Ω$**

**Test Method:** Human Body Model

**Test Specification:** NSC SOP-5-028

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock Pulse Width</td>
<td>Low</td>
<td>7 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
<td>7 ns</td>
</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_H$</td>
<td>Hold Time of Input after Clock</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback</td>
<td>55.5 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback</td>
<td>71.4 MHz</td>
</tr>
<tr>
<td>$V_Z$</td>
<td>Register Preload Control Voltage</td>
<td></td>
<td>V</td>
</tr>
</tbody>
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### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage (Note 6)</td>
<td>$V_{CC} = \text{Min, } I = -18mA$</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage (Note 6)</td>
<td></td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Input Clamp Voltage</td>
<td>$V_{CC} = \text{Max, } V_I = 0.4V$</td>
<td>-1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = \text{Max, } V_I = 2.4V$</td>
<td>-250</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = \text{Max, } V_I = 5.5V$</td>
<td>100</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_I$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max, } V_I = 5.5V$</td>
<td>100</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min, } I_{OL} = 24mA$</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min, } I_{OH} = -3.2mA$</td>
<td>2.7</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Low Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max, } V_O = 0.4V$</td>
<td>-50</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 7)</td>
<td>$V_{CC} = \text{Max, } V_O = 2.4V$</td>
<td>50</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short-Circuit Current (Note 8)</td>
<td>$V_{CC} = 5V, V_O = 0V$</td>
<td>-50</td>
<td>-130 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC} = \text{Max, Outputs Open}$</td>
<td>125</td>
<td>210 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_1$</td>
<td>Input Capacitance</td>
<td>$V_{CC} = 5.0V, V_I = 2.0V$</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_O$</td>
<td>Output Capacitance</td>
<td>$V_{CC} = 5.0V, V_O = 2.0V$</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{I/O}$</td>
<td>I/O Capacitance</td>
<td></td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Series D (PAL20L8D, PAL20R4D, PAL20R6D, PAL20R8D) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $V_O$ must not exceed $V_{CC} + 1V$.

Note 4: $t_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.

$V_{CC}$ without feedback is derived as $(2T_A)^{-1}$.

Note 5: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OL}$ or between $I_{IH}$ and $I_{OH}$.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{DS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>$C_L = 50 \text{ pF}, S_1 \text{ Closed}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLK}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>$C_L = 50 \text{ pF}, S_1 \text{ Closed}$</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZXG}$</td>
<td>Pin to Registered Output Enabled</td>
<td>$C_L = 50 \text{ pF}, \text{Active High: } S_1 \text{ Open, Active Low: } S_1 \text{ Closed}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PXZG}$</td>
<td>Pin to Registered Output Disabled</td>
<td>$C_L = 5 \text{ pF}, \text{From } V_{OH}: S_1 \text{ Open, From } V_{OL}: S_1 \text{ Closed}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZXI}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>$C_L = 50 \text{ pF}, \text{Active High: } S_1 \text{ Open, Active Low: } S_1 \text{ Closed}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PXZI}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>$C_L = 5 \text{ pF}, \text{From } V_{OH}: S_1 \text{ Open, From } V_{OL}: S_1 \text{ Closed}$</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RESET}$</td>
<td>Power-Up to Registered Output High</td>
<td></td>
<td>1000</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Test Load

![Test Load Diagram](image-url)

R1 = 200
R2 = 390

### Schematic of Inputs and Outputs

![Schematic](image-url)
Test Waveforms

Set-Up and Hold

CLOCK
DATA INPUT
3V
0V
3V
0V

Propagation Delay

INPUT
IN-PHASE OUTPUT (S1 CLOSED)
OUT OF PHASE OUTPUT (S1 CLOSED)

Notes:
VT = 1.5V
CL includes probe and jig capacitance.
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms

IN-PHASE OUTPUT
IN-PHASE OUTPUT
IN-PHASE OUTPUT
IN-PHASE OUTPUT

Enable and Disable

ENABLING INPUT
ENABLE
DISABLE

Power-Up Set/Reset Waveform

VCC
0V
5V
90%

*The clock input should not be switched from low to high until after time tRESET of tSET.*
Functional Description

All of the 24-pin Medium PAL logic arrays consist of 20 complementary input lines and 64 product-term lines with a programmable cell at each intersection (2560 cells). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

For the fuse-link PAL devices (all PAL devices prior to National Series D), an unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. In the National Series D vertical fuse PAL devices, a programmed vertical fuse cell establishes a connection between an input line and a product term. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses for the fuse-link devices, or by programming the corresponding cells for the vertical fuse devices) are in the high logic state. Therefore, if both the true and complement of at least one array input is connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed fuse-link device). Conversely, if all input lines are disconnected from a product line, the product term and the resulting logic function would be held in the high state (which is the state of all product terms in an unprogrammed National Series-D PAL device).

The medium PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20L8, 20R4, 20R6 and 20R8 architectures have 0, 4, 6 and 8 registered outputs, respectively, with the balance of the 8 outputs combinatorial. All outputs are active-low and have TRI-STATE capability.

Each combinatorial output has a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20L8). This allows a pin to perform bidirectional I/O or, if the associated TRI-STATE control product term were programmed to remain unsatisfied (always false), the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable (G) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

Series-B Medium PAL devices set all the registers high on power-up (active low outputs assume low logic levels if enabled). Series-D Medium PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up set or reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the set or reset operation. The clock input should also remain stable until after the power-up set or reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

For the National Series D PAL device, during power-up, all outputs are held in the high-impedance state until DC power supply conditions are met (VCC approximately 3.0V), after which they may be enabled by the TRI-STATE control product terms (combinatorial outputs) or the G pin (registered outputs). Whenever VCC goes below 3V (at 25°C), the outputs are disabled as shown in Figure 1 below.

![FIGURE 1. Series-D Power-Up TRI-STATE Waveform](image)

Note: t<sub>z</sub> is less than 100 ns.

**FIGURE 1. Series-D Power-Up TRI-STATE Waveform**

In an unprogrammed National Series D PAL device, no array inputs are connected to any product-term lines. Therefore, all combinatorial outputs would be enabled and driving low logic levels (after power-up is completed). All registers would still initialize to the low state, but would become permanently set (low-level outputs, if enabled) following the first clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V<sub>OL</sub>, V<sub>OH</sub>, or resistively to VCC. However, switching any input not connected to a product term or logic function has no effect on its output logic state.
28-Lead PLCC Connection Conversion Diagram*

Non-JEDEC PLCC Diagram

Typical Registered Logic Function Without Feedback

Typical Registered Logic Function With Feedback

*For availability of old (non-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor.
Functional Description (Continued)

CLOCK FREQUENCY SPECIFICATION

The clock frequency \( f_{\text{CLK}} \) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period \( f_{\text{CLK}}^{-1} \) without feedback is defined as the greater of the minimum clock period \( t_{\text{ClK high}} + t_{\text{ClK low}} \) and the minimum "data window" period \( t_{\text{SU}} + t_{\text{L}} \). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period \( f_{\text{CLK}}^{-1} \) with feedback is defined as \( f_{\text{CLK}} + t_{\text{SU}} \). This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Output Register Preload

This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility. This feature is available on the Series-B and Series-D devices only.

SERIES-D

For the National Series D PAL devices, the preload function allows the registers to be loaded directly and asynchronously with any desired pattern. These vertical-fuse devices provide two register preload operations:

1. All registers can be reset to the low state (high-level outputs) by applying the elevated control voltage \( V_{\text{Z}} \) to input pin \( 2* \) for time \( t_{\text{D}} \) (Figure 2a).
2. Selected registers can be set to the high state (low-level outputs) as follows (Figure 2b):
   a. All registered outputs are disabled by raising the \( \overline{G} \) input pin 1* to \( V_{\text{IL}} \)
   b. After time \( t_{\text{D}} \), the selected registered output pins are raised to the elevated control voltage \( V_{\text{Z}} \) for time \( t_{\text{D}} \) to set the corresponding registers.

*Refers to DIP packages only. For equivalent PCC package refer to the 28-pin PCC connection conversion diagram.

SERIES-B

For Series-B devices in the 24-pin Medium PAL family, the preload function allows the registers to be loaded asynchronously from data placed on the output pins. The register preload procedure is as follows and the waveform is shown in Figure 3:

1. Apply VCC
2. Disable the registered outputs by raising pin 13 to \( V_{\text{IL}} \)
3. Apply \( V_{\text{IL}} \) to inputs corresponding to all non-registered outputs.
4. Apply the desired \( V_{\text{IL}}/V_{\text{IH}} \) to the inputs corresponding to registered outputs. (A high input will force the register high and the output low.)
5. Raise the Preload pins (pin 18 and pin 14) to \( V_{\text{IH}} \) (\( V_{\text{IH}} = 11.75V \pm 0.25V \))
6. Apply a clock pulse.
7. Remove \( V_{\text{IH}} \) from the Preload pins. (The data inputs will return to normal inputs.)
8. Lower pin 13 to \( V_{\text{IL}} \) to enable the outputs.

Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

In National Series D PAL devices, logical and physical connections between array input lines and product-term lines are established when vertical fuse cells are programmed. This is opposite to other PAL products based on fusible links in which connections are established when fuses are left unprogrammed (intact). This difference is compensated by the vertical-fuse PAL programming algorithm so that the user's design development process looks the same. (The only functional difference due to vertical-fuse technology is the behavior of "unprogrammed" devices). The JEDEC programming maps produced by PAL development software for all Medium PAL devices denote a "connection" with a "0", and a "non-connection" with a "1". The programming algorithms for most fuse-link PLDs program fuses where ones are located in the map to remove corresponding connections, whereas the algorithm for National Series D PAL products automatically compensates by programming vertical-fuse cells where zeroes are located in the map to establish connections. Therefore, the same JEDEC map representing the user's desired logic equations produces the same functional results when using either PAL technology. The user need only provide the appropriate device code and/or adapter for the programming equipment to invoke the proper programming algorithm. Only programmers with the certified National Series D vertical-fuse PAL programming algorithm can be used to program these vertical-fuse devices.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Medium PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.
Functional Description (Continued)

a) To Reset All Registers

b) To Set Selected Registers

Note: $V_Z = 9.5V$ to $10.0V$, $t_d$ min. = 500 ns

FIGURE 2. Series-D Register Preload Waveforms (Vertical-Fuse Devices)

FIGURE 3. Series-B Register Preload Waveform (Fuse-Link Devices)
Ordering Information

Programmable Array Logic Family

Number of Array Inputs

Output Type:
- H = Active High
- L = Active Low
- C = Complementary
- R = Registered
- X = Exclusive-OR Registered
- P = Programmable Polarity

Number of Registered Outputs (or total outputs if non-registered)

Speed Version:
- A = 25 ns
- B = 15 ns
- D = 10 ns

Package Type:
- N = 24-Pin Plastic DIP
- J = 24-Pin Ceramic DIP
- V = 28-Lead Plastic Chip Carrier JEDEC Standard Pinout
- XV = 28-Lead PLCC Non-JEDEC Standard Pinout

Temperature Range:
- C = Commercial (0°C to +75°C)
- M = Military (−55°C to +125°C)
JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number
Programmable Array Logic (PAL®)  
24-Pin Polarity PAL Family—Series B

General Description

The PAL family utilizes National Semiconductor’s advanced oxide isolated Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array). In addition, the PAL family offers the options of having variable input/output ratios, programmable TRISTATE® outputs and having registers with feedback.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

Registers consist of D-type flip-flops that are loaded on the low-to-high transition of the clock. The registers power up with a high (V<sub>OH</sub>) at the output pin, regardless of the polarity fuse.

The entire PAL family is programmed on inexpensive conventional programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Features

- 15 ns maximum propagation delay (combinatorial)
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLANTM development software
- Power-up reset for registered outputs
- Register preload facilitates device testing
- Security fuse prevents direct copying of logic patterns
- Skinny DIP packages

Device Types

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Dedicated Inputs</th>
<th>Registered Outputs (With Feedback)</th>
<th>Combinatorial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>I/Os</td>
<td>Outputs</td>
</tr>
<tr>
<td>PAL20P8B</td>
<td>14</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>PAL20RP4B</td>
<td>12</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>PAL20RP6B</td>
<td>12</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>PAL20RP8B</td>
<td>12</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

Speed/Power Versions

<table>
<thead>
<tr>
<th>Series</th>
<th>Example</th>
<th>Commercial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>t&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>B</td>
<td>PAL 20P8B</td>
<td>15 ns</td>
<td>210 mA</td>
</tr>
</tbody>
</table>
### Series-B (PAL20P8B, PAL20RP4B, PAL20RP6B, PAL20RP8B)

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage ($V_{CC}$) (Note 2) $-0.5V$ to $+7.0V$
- Input Voltage (Note 2) $-1.5V$ to $+5.5V$
- Off-State Output Voltage (Note 2) $-1.5V$ to $+5.5V$
- Input Current (Note 2) $-30mA$ to $+5.0mA$
- Output Current ($I_{OL}$) $+100mA$

- Storage Temperature $-65°C$ to $+150°C$
- Ambient Temperature with Power Applied $-65°C$ to $+125°C$
- Junction Temperature $-65°C$ to $+150°C$
- ESD Tolerance 2000V
- $C_{ZAP} = 100 \mu F$
- $R_{ZAP} = 1500\Omega$
- Test Method: Human Body Model
- Test Specification: NSC SOP-5-028

#### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>$4.5$</td>
<td>$5$</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td>$-55$</td>
<td>$0$</td>
</tr>
<tr>
<td>$T_C$</td>
<td>Operating Case Temperature</td>
<td></td>
<td>$125$</td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock Pulse Width</td>
<td>Low $12$</td>
<td>$5$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High $12$</td>
<td>$5$</td>
</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time from Input or Feedback to Clock</td>
<td>$20$</td>
<td>$10$</td>
</tr>
<tr>
<td>$t_H$</td>
<td>Hold Time of Input after Clock</td>
<td>$0$</td>
<td>$-8$</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 3)</td>
<td>With Feedback $28.6$</td>
<td>$37$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback $41.7$</td>
<td>$50$</td>
</tr>
</tbody>
</table>

#### Electrical Characteristics Over Recommended Operating Conditions (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage (Note 5)</td>
<td>$0.8$</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage (Note 5)</td>
<td>$2$</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Input Clamp Voltage</td>
<td>$V_{CC} = Min, I = -18mA$</td>
<td>$-0.8$</td>
<td>$-1.5$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = Max, V_{I} = 0.4V$</td>
<td>$-0.04$</td>
<td>$-0.25$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current (Note 6)</td>
<td>$25$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current (Note 6)</td>
<td>$V_{CC} = Max, V_{I} = 2.4V$</td>
<td>$100$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = Max, V_{I} = 5.5V$</td>
<td>$100$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = Min, I_{OL} = 12mA$</td>
<td>$0.3$</td>
<td>$0.5$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = Max, I_{OL} = 24mA$</td>
<td>MIL</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = Min, I_{OH} = -2mA$</td>
<td>$2.4$</td>
<td>$3.4$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = Max, I_{OH} = -3.2mA$</td>
<td>MIL</td>
<td>COM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Low Level Off-State Output Current (Note 6)</td>
<td>$V_{CC} = Max, V_{O} = 0.4V$</td>
<td>$-100$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current (Note 6)</td>
<td>$V_{CC} = Max, V_{O} = 2.4V$</td>
<td>$100$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short-Circuit Current (Note 7)</td>
<td>$V_{CC} = 5V, V_{O} = 0V$</td>
<td>$-30$</td>
<td>$-70$</td>
<td>$-130$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC} = Max, Outputs Open$</td>
<td>$140$</td>
<td>$210$</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $f_{\text{CLK}}$ with feedback is derived as $(t_{\text{CLK}} + t_{\text{su}})^{-1}$.
$\bar{f}_{\text{CLK}}$ without feedback is derived as $(2t_W)^{-1}$.

Note 4: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

Note 5: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 6: Leakage current for bidirectional I/O pins is the worst case between $I_{LH}$ and $I_{OZH}$ or between $I_{IH}$ and $I_{OH}$. 

Note 7: To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

### Switching Characteristics

Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ Max</td>
<td>Min Typ Max</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>$C_L = 50 , \text{pF}, S1 , \text{Closed}$</td>
<td>11</td>
<td>20</td>
<td>11 15 ns</td>
</tr>
<tr>
<td>$t_{CLK}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>$C_L = 50 , \text{pF}, S1 , \text{Closed}$</td>
<td>8</td>
<td>15</td>
<td>8 12 ns</td>
</tr>
<tr>
<td>$t_{PZXG}$</td>
<td>$G$ Pin to Registered Output Enabled</td>
<td>$C_L = 50 , \text{pF}, \text{Active High: S1 Open, Active Low: S1 Closed}$</td>
<td>10</td>
<td>20</td>
<td>10 15 ns</td>
</tr>
<tr>
<td>$t_{PXZG}$</td>
<td>$G$ Pin to Registered Output Disabled</td>
<td>$C_L = 5 , \text{pF}, \text{from VOH: S1 Open, from VOL: S1 Closed}$</td>
<td>11</td>
<td>20</td>
<td>11 15 ns</td>
</tr>
<tr>
<td>$t_{PZXI}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>$C_L = 50 , \text{pF}, \text{Active High: S1 Open, Active Low: S1 Closed}$</td>
<td>10</td>
<td>20</td>
<td>10 15 ns</td>
</tr>
<tr>
<td>$t_{PXZI}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>$C_L = 5 , \text{pF}, \text{from VOH: S1 Open, from VOL: S1 Closed}$</td>
<td>11</td>
<td>20</td>
<td>11 15 ns</td>
</tr>
<tr>
<td>$t_{RESET}$</td>
<td>Power-Up to Registered Output High</td>
<td></td>
<td>600</td>
<td>1000</td>
<td>600 1000 ns</td>
</tr>
</tbody>
</table>

### Test Load

Schematic of Inputs and Outputs
Test Waveforms

Set-Up and Hold

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>DATA INPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Hold

<table>
<thead>
<tr>
<th></th>
<th>HOLD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Pulse Width

<table>
<thead>
<tr>
<th>HIGH-LEVEL PULSE INPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Low-Level PULSE INPUT

<table>
<thead>
<tr>
<th></th>
<th>3V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0V</td>
</tr>
</tbody>
</table>

Notes:

- \( V_T = 1.5V \)
- \( C_L \) includes probe and jig capacitance.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>VALID INPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CLOCK

<table>
<thead>
<tr>
<th>g</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Registered Outputs

<table>
<thead>
<tr>
<th>ANY INPUT PROGRAMMED FOR TRI-STATE CONTROL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Combinatorial Outputs

<table>
<thead>
<tr>
<th>VALID DISABLE</th>
<th>VALID ENABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Power-Up Reset Waveform

\( V_{CC} \)

\( 5V \)

\( 0V \)

\( t_{RESET} \)

\( 90\% \)

Registered Outputs

\( V_{OH} \)

\( V_{OL} \)

\( V_{IL} \)

\( V_{IH} \)

\( V_{IL} \)

\( t_{RESET} \)

*The clock input should not be switched from low to high until after time \( t_{RESET} \).*
Functional Description

All of the 24-pin Polarity PAL logic arrays consist of 20 complementary input lines and 64 product-term lines with a programmable fuse link at each intersection (2560 fuses). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

The Polarity PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20P8, 20RP4, 20RP6 and 20RP8 architectures have 0, 4, 6 and 8 registered outputs, respectively, with the balance of the 8 outputs combinatorial. All outputs have TRI-STATE capability.

Each combinatorial output has a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20P8). This allows a pin to perform bidirectional I/O or, if the associated logic function were left unprogrammed, the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable (G) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

The programmable polarity feature controls active-high and active-low polarity on individual output pins, eliminating the need for external inverters. When the programmable polarity selection fuse is left unprogrammed, the output pin is active-low. When the fuse is programmed, the output pin is active-high. Polarity inversions occur before any output register.

Series-B Polarity PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled regardless of the state of the polarity fuses). This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, VOL, VOH, or resistively to VCC. However, switching any input not connected to a product term or logic function has no effect on its output logic state.
24-Pin Polarity PAL Family Block Diagrams—DIP Connections

**PAL20P8**

**PAL20RP4**

**PAL20RP6**

**PAL20RP8**
Typical Registered Logic Function Without Feedback

Typical Registered Logic Function With Feedback
Functional Description (Continued)

CLOCK FREQUENCY SPECIFICATION

The clock frequency (f_CLK) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (t_CLK) is defined as the greater of the minimum clock period (t_W high + t_W low) and the minimum "data window" period (t_SU + t_D). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_CLK = 1) is defined as t_CLK + t_SU. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Output Register Preload

The preload function allows the registers to be loaded asynchronously from data placed on the output pins. This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The register preload procedure is as follows:

1. V_CC is raised to 4.5V.
2. Registered outputs are disabled by raising output enable (G) to V_H.
3. The desired data values are applied to all registered output pins (V_L = set, V_H = reset).
4. DIP pin 23 (PCC pin 27) is pulsed to V_P, then back to V_L.
V_P = 18.0V ± 0.5V.

5. Data inputs are removed from registered output pins.
6. G is lowered to V_L to enable registered outputs.
7. The desired data values are verified at all registered outputs (V_OH = set, V_OH = reset).

Note: The minimum recommended time delay (t_D) between successive input transitions (including the V_P pulse width on DIP pin 8) is 100 ns.

Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a large variety of programming equipment. Many software packages and programming units support a variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Polarity PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.
Ordering Information

Programmable Array Logic Family
Number of Array Inputs
Output Type:
R = Registered
P = Programmable Polarity
Number of Registered Outputs
Speed/Power Version:
B = 15 ns
Package Type:
N = 24-Pin Plastic DIP
J = 24-Pin Ceramic DIP
V = 28-Lead Plastic Chip Carrier JEDEC Standard Pinout
XV = 28-Lead PLCC non-JEDEC Standard Pinout
Temperature Range:
C = Commercial (0°C to +75°C)
M = Military (−55°C to +125°C)
Logic Diagram—PAL20P8B

24-Pin Polarity PAL Family—Series B

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
PAL16RA8
Programmable Array Logic (PAL®)

General Description
The PAL16RA8 is a new member of National's broad PAL® family. It provides several new features which will dramatically benefit PAL users. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the RA (Registered Asynchronous) devices.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL16RA8 is made up of eight Output Logic Macro Cells (OLMC). Four AND array outputs feed into the fixed OR-gate for each OLMC to generate the device's output functions. Four other AND array outputs are used for control functions in the OLMC. With a robust mixture of logic derived controlled functions and selectable output data paths, the PAL16RA8 provides an ideal solution for registered random logic applications.

This device is housed in a 20-pin 300 mil DIP. A 20-pin PCC package is also available. It can be programmed by most PAL programmers.

Features
- Programmable asynchronous set and reset
- Individually programmable clocks
- Programmable and hard-wired TRI-STATE® outputs
- Programmable output polarity
- Registers can be bypassed individually
- Register preload guarantees testability
- Outputs can be reconfigured as inputs
- Power-up reset for registered outputs
- Fully supported by National PLANTM development software
- A variety of JEDEC-compatible programming equipment and design development software available
- Security fuse prevents direct copying of logic patterns

Block Diagram—PAL16RA8
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Operating</th>
<th>Programming</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off-State Output Voltage</td>
<td>5.5V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>ESD Tolerance (Note 2)</td>
<td>C_{ZAP} = 100 pF</td>
</tr>
<tr>
<td></td>
<td>R_{ZAP} = 1500Ω</td>
</tr>
<tr>
<td></td>
<td>Test Method: Human Body Model</td>
</tr>
<tr>
<td></td>
<td>Test Specification: NSC SOP-5-028</td>
</tr>
</tbody>
</table>

Supply Voltage V\text{CC} | 7.0V | 12.0V |
Input Voltage | 5.5V | 22.0V |

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{CC}</td>
<td>Supply Voltage</td>
<td></td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
</tr>
<tr>
<td>T_\text{A}</td>
<td>Operating Free-Air Temperature</td>
<td></td>
<td>-55</td>
<td></td>
<td>75</td>
</tr>
<tr>
<td>T_\text{C}</td>
<td>Operating Case Temperature</td>
<td></td>
<td>125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_\text{W}</td>
<td>Pulse Width of Clocking Input (High/Low)</td>
<td></td>
<td>25</td>
<td>13</td>
<td>20</td>
</tr>
<tr>
<td>t_{\text{WP}}</td>
<td>Pulse Width of Preload (PL) Input (Low)</td>
<td></td>
<td>45</td>
<td>15</td>
<td>35</td>
</tr>
<tr>
<td>t_{\text{SU}}</td>
<td>Setup Time from Input or Feedback to Clocking Input</td>
<td></td>
<td>25</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>t_{\text{SUP}}</td>
<td>Setup Time from Input to PL High</td>
<td></td>
<td>30</td>
<td>5</td>
<td>25</td>
</tr>
<tr>
<td>t_\text{H}</td>
<td>Hold Time of Input after Clocking Input</td>
<td></td>
<td>10</td>
<td>-2</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>-6</td>
<td>0</td>
</tr>
<tr>
<td>t_{\text{HP}}</td>
<td>Hold Time of Input after PL High</td>
<td></td>
<td>30</td>
<td>5</td>
<td>25</td>
</tr>
<tr>
<td>f_{\text{CLK}}</td>
<td>Clock Frequency (Note 3)</td>
<td></td>
<td></td>
<td>With Feedback</td>
<td>16.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Without Feedback</td>
<td>20</td>
</tr>
</tbody>
</table>

Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{\text{IL}}</td>
<td>Low-Level Input Voltage</td>
<td>(Note 4)</td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>V_{\text{IH}}</td>
<td>High-Level Input Voltage</td>
<td>(Note 4)</td>
<td>2.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{\text{IC}}</td>
<td>Input Clamp Voltage</td>
<td>V_{\text{CC}} = \text{Min}</td>
<td>I_\text{I} = -18 mA</td>
<td>-0.8</td>
<td>-1.5</td>
</tr>
<tr>
<td>I_{\text{IL}}</td>
<td>Low-Level Input Current</td>
<td>V_{\text{CC}} = \text{Max}</td>
<td>V_\text{I} = 0.4V</td>
<td>-0.02</td>
<td>-0.25</td>
</tr>
<tr>
<td>I_{\text{IH}}</td>
<td>High-Level Input Current</td>
<td>V_{\text{CC}} = \text{Max}</td>
<td>V_\text{I} = 2.4V</td>
<td>25</td>
<td>\mu A</td>
</tr>
<tr>
<td>I_\text{I}</td>
<td>Maximum Input Current</td>
<td>V_{\text{CC}} = \text{Max}</td>
<td>V_\text{I} = 5.5V</td>
<td>100</td>
<td>\mu A</td>
</tr>
<tr>
<td>V_{\text{OL}}</td>
<td>Low-Level Output Voltage</td>
<td>V_{\text{CC}} = \text{Min}</td>
<td>I_{\text{OL}} = 8 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{\text{OH}}</td>
<td>High-Level Output Voltage</td>
<td>V_{\text{CC}} = \text{Min}</td>
<td>I_{\text{OH}}: \text{Mil-2 mA}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>\text{Com-3.2 mA}</td>
<td>2.4</td>
<td>2.8</td>
</tr>
<tr>
<td>I_{\text{OZ}}</td>
<td>Off-State Output Current</td>
<td>V_{\text{CC}} = \text{Max}</td>
<td>(Note 5) V_\text{O} = 0.4 \text{ or } 2.4V</td>
<td>-100</td>
<td>100</td>
</tr>
<tr>
<td>I_{\text{OS}}</td>
<td>Output Short-Circuit Current</td>
<td>V_{\text{CC}} = 5V</td>
<td>(Note 6) V_\text{O} = 0V</td>
<td>-30</td>
<td>-70</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-130</td>
<td>mA</td>
</tr>
<tr>
<td>I_{\text{CC}}</td>
<td>Supply Current</td>
<td>V_{\text{CC}} = \text{Max}</td>
<td></td>
<td>135</td>
<td>170</td>
</tr>
</tbody>
</table>

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and, although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 3: f_{\text{CLK}} with feedback is derived as (t_{\text{CLK}} + t_{\text{SU}})^{-1}.

Note 4: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: I/O leakage as the worst case of I_{\text{OXZ}} or I_{\text{OX}}, e.g. I_{\text{I}} and I_{\text{OZ}}.

Note 6: During I_{\text{OS}} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

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### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>tPD</td>
<td>Input or Feedback to Combinatorial Output Polarity Fuse Intact</td>
<td>$C_L = 50 , \text{pF}, , S1 , \text{Closed}$</td>
<td>20</td>
<td>35</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25</td>
<td>40</td>
<td>25</td>
</tr>
<tr>
<td>tCLK</td>
<td>Clocking Input to Registered Output or Feedback</td>
<td>$C_L = 50 , \text{pF}, , S1 , \text{Closed}$</td>
<td>10</td>
<td>17</td>
<td>35</td>
</tr>
<tr>
<td>tPZXG</td>
<td>$G$ Pin to Output Enabled</td>
<td>$C_L = 5 , \text{pF}$, Active High: S1 Open, Active Low: S1 Closed</td>
<td>10</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>tPZXG</td>
<td>$G$ Pin to Output Disabled</td>
<td>$C_L = 5 , \text{pF}$, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed</td>
<td>10</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>tPZI</td>
<td>Input to Output Enabled via Product Term</td>
<td>$C_L = 50 , \text{pF}$, Active High: S1 Open, Active Low: S1 Closed</td>
<td>18</td>
<td>35</td>
<td>18</td>
</tr>
<tr>
<td>tPZI</td>
<td>Input to Output Disabled via Product Term</td>
<td>$C_L = 5 , \text{pF}$, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed</td>
<td>15</td>
<td>35</td>
<td>15</td>
</tr>
<tr>
<td>tRESET</td>
<td>Power-Up to Registered Output-High</td>
<td></td>
<td>600</td>
<td>1000</td>
<td>600</td>
</tr>
<tr>
<td>tS</td>
<td>Asynchronous Set Input to Registered Output Low</td>
<td></td>
<td>22</td>
<td>40</td>
<td>22</td>
</tr>
<tr>
<td>tR</td>
<td>Asynchronous Reset Input to Registered Output High</td>
<td></td>
<td>27</td>
<td>45</td>
<td>27</td>
</tr>
</tbody>
</table>

### Schematic of Inputs and Outputs

![Schematic of Inputs and Outputs](image)

### Test Load

![Test Load](image)
Test Waveforms

Set-Up and Hold

Pulse Width

Propagation Delay

Enable and Disable

Notes:

\[ V_T = 1.5V \]

CL includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms

Power-Up Reset Waveform

*The clock input should not be switched from low to high until after time \( t_{\text{RESET}} \).
Functional Description

The PAL16RA8 logic array consists of 16 complementary input lines and 64 product-term lines with a programmable fuse link at each intersection (2048 fuses). The product terms are organized into eight groups of eight each. Four of the eight product terms in each group connect into an OR-gate to produce the sum-of-products logic function. The remaining four product terms in each group are used for control functions in the Output Logic Macro Cell (OLMC) as shown in Figure 1.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

Programmable Set and Reset

In each cell, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1, the output pin becomes a 0. If the reset product line is high, the register output becomes a logic 0, the output pin becomes a 1. The operation of the programmable set and reset overrides the clock.

Individually Programmable Register Bypass

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

Programmable Clock

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

Programmable and Hard-Wired Tri-State Outputs

The PAL16RA8 provides a product term dedicated to output control. There is also an output control pin (Pin 11). The output is enabled if both the output control pin is low and the output control product term is HIGH. If the output control pin is high all outputs will be disabled or if an output control product term is low, then that output will be disabled.

Programmable Output Polarity

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-or gates shown in the PAL16RA8 Logic Diagram. When the output polarity fuse is blown, the lower input to the exclusive-or gate is high, so the output is active-high, Similarly, when the output polarity fuse is intact, the output is active-low. The programmable output polarity features allows the user a higher degree of flexibility when writing equations.

Output Control Alternatives

<table>
<thead>
<tr>
<th>Output Always Enabled</th>
<th>Programmable</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="output_always_enabled.png" alt="Diagram" /></td>
<td><img src="programmable.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

Registered/Active Low

Combinatorial/Active Low

Registered/Active High

Combinatorial/Active High

Registered/Active Low

Combinatorial/Active Low

Registered/Active High

Combinatorial/Active High

Registered/Active Low

Combinatorial/Active Low

Registered/Active High

Combinatorial/Active High
**Functional Description** (Continued)

The PAL16RA8 devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, \( V_{CC} \) must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, \( V_{OL} \) or \( V_{OH} \), or resistively to \( V_{CC} \). However, switching any input not connected to a product term or logic function has no effect on its output logic state.

**CLOCK FREQUENCY SPECIFICATION**

The clock frequency (\( f_{CLK} \)) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (\( f_{CLK}^{-1} \) without feedback) is defined as the greater of the minimum clock period (\( t_{W \text{ high}} + t_{W \text{ low}} \)) and the minimum "data window" period (\( t_{SU} + t_{H} \)). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (\( f_{CLK}^{-1} \) with feedback) is defined as \( t_{CLK} + t_{SU} \). This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.
Functional Description (Continued)

FIGURE 1. "RA" Output Logic Macrocell Logic Diagram

20-Pin PAL16RA8 Block Diagram—DIP Connections
Output Register Preload

Register preload allows any arbitrary state to be loaded into the PAL output registers. This allows complete logic verification, including states that are impossible or impractical to reach. To use the preload feature, first disable the outputs by bringing OE high, and present the data at the output pins. A low-level on the preload pin (PL) will then load the data into the registers.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLANTM software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL16RA8 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.
Ordering Information

Programmable Array Logic Family
Number of Array Inputs
Output Type
RA = Register Asynchronous
Number of Outputs
Package Type
N = 20-Pin Plastic DIP
J = 20-Pin Ceramic DIP
V = 20 Lead Plastic Chip Carrier
Temperature Range
C = Commercial (0°C TO +75°C)
M = Military (-55°C TO +125°C)

PAL 16RA8NC

TL/L/9253-2
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number
General Description
The PAL20RA10 is a new member of National's broad PAL family. It provides several new features which will dramatically benefit PAL users. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the RA (Registered Asynchronous) devices.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL20RA10 is made up of ten Output Logic Macro Cells (OLMC). Four AND array outputs feed into the fixed OR-gate for each OLMC to generate the device's output functions. Four other AND array outputs are used for control functions in the OLMC. With a robust mixture of logic derived controlled functions and selectable output data paths, the PAL20RA10 provides an ideal solution for registered random logic applications.

This device is housed in a 24-pin 300 mil DIP. A 28-pin PCC package is also available. It can be programmed by most PAL programmers.

Features
- Programmable asynchronous set and reset
- Individually programmable clocks
- Programmable and hard-wired TRI-STATE® outputs
- Programmable output polarity
- Registers can be bypassed individually
- Register preload guarantees testability
- Outputs can be reconfigured as inputs
- Power-up reset for registered outputs
- Fully supported by National PLAN™ development software
- A variety of JEDEC-compatible programming equipment and design development software available
- Security fuse prevents direct copying of logic patterns

Block Diagram—PAL20RA10
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Operating</th>
<th>Programming</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage V_{CC}</td>
<td>Off-State Output Voltage</td>
</tr>
<tr>
<td>7.0V</td>
<td>5.5V</td>
</tr>
<tr>
<td>12.0V</td>
<td>12.0V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>Storage Temperature</td>
</tr>
<tr>
<td>5.5V</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>22.0V</td>
<td>ESD Tolerance (Note 2)</td>
</tr>
<tr>
<td>C_{ZAP} = 100 pF</td>
<td>1000V</td>
</tr>
<tr>
<td>R_{ZAP} = 1500Ω</td>
<td></td>
</tr>
<tr>
<td>Test Method: Human Body Model</td>
<td></td>
</tr>
<tr>
<td>Test Specification: NSC SOP-5-028</td>
<td></td>
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</tbody>
</table>

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>Supply Voltage</td>
<td>Min</td>
<td>Nom</td>
<td>Max</td>
</tr>
<tr>
<td>T_{A}</td>
<td>Operating Free-Air Temperature</td>
<td>-55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{C}</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{W}</td>
<td>Pulse Width of Clocking Input (High/Low)</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{WP}</td>
<td>Pulse Width of Preload (PL) Input (Low)</td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{SU}</td>
<td>Setup Time from Input or Feedback to Clocking Input</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{SUP}</td>
<td>Setup Time from Input to PL High</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{H}</td>
<td>Hold Time of Input after Clocking Input</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{HP}</td>
<td>Hold Time of Input after PL High</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f_{CLK}</td>
<td>Clock Frequency (Note 3)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IL}</td>
<td>Low-Level Input Voltage</td>
<td>(Note 4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IH}</td>
<td>High-Level Input Voltage</td>
<td>(Note 4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IC}</td>
<td>Input Clamp Voltage</td>
<td>V_{CC} = Min</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Low-Level Input Current</td>
<td>V_{CC} = Max</td>
<td>V_{I} = 0.4V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IH}</td>
<td>High-Level Input Current</td>
<td>V_{CC} = Max</td>
<td>V_{I} = 2.4V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{I}</td>
<td>Maximum Input Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Low-Level Output Voltage</td>
<td>V_{CC} = Min</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>High-Level Output Voltage</td>
<td>V_{CC} = Min</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OZ}</td>
<td>Off-State Output Current</td>
<td>V_{CC} = Max</td>
<td>(Note 5) V_{O} = 0.4V or 2.4V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OS}</td>
<td>Output Short-Circuit Current</td>
<td>V_{CC} = 5V</td>
<td>(Note 6) V_{O} = 0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Supply Current</td>
<td>V_{CC} = Max</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at those values.

Note 2: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 are connected directly to the security fuses, and, although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 3: f_{CLK} with feedback is derived as (f_{CLK} + t_{SU})^{-1}.

Note 4: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: I/O leakage as the worst case of I_{OZ} or I_{IH}, e.g. I_{IL} and I_{OZL}.

Note 6: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.
## Switching Characteristics

**Over Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>Military</th>
<th>Commercial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Parameter</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>tPD</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>Polarity Fuse Intact: $C_L = 50,\text{pF}, S1\ Closed$</td>
<td>20</td>
<td>35</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Polarity Fuse Blown: $C_L = 50,\text{pF}, S1\ Closed$</td>
<td>25</td>
<td>40</td>
<td>25</td>
</tr>
<tr>
<td>tCLK</td>
<td>Clock Input to Registered Output or Feedback</td>
<td>$C_L = 50,\text{pF}, S1\ Closed$</td>
<td>10</td>
<td>17</td>
<td>35</td>
</tr>
<tr>
<td>tS</td>
<td>Asynchronous Set Input to Registered Output Low</td>
<td></td>
<td>22</td>
<td>40</td>
<td>22</td>
</tr>
<tr>
<td>tR</td>
<td>Asynchronous Reset Input to Registered Output High</td>
<td></td>
<td>27</td>
<td>45</td>
<td>27</td>
</tr>
<tr>
<td>tPXZG</td>
<td>G Pin to Output Enabled</td>
<td>$C_L = 50,\text{pF}$, Active High: S1 Open, Active Low: S1 Closed</td>
<td>10</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>tPXZG</td>
<td>G Pin to Output Disabled</td>
<td>$C_L = 5,\text{pF}$, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed</td>
<td>10</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>tPXZI</td>
<td>Input to Output Enabled via Product Term</td>
<td>$C_L = 50,\text{pF}$, Active High: S1 Open, Active Low: S1 Closed</td>
<td>18</td>
<td>35</td>
<td>18</td>
</tr>
<tr>
<td>tPXZI</td>
<td>Input to Output Disabled via Product Term</td>
<td>$C_L = 5,\text{pF}$, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed</td>
<td>15</td>
<td>35</td>
<td>15</td>
</tr>
<tr>
<td>tRESET</td>
<td>Power-Up to Registered Output High</td>
<td></td>
<td>600</td>
<td>1000</td>
<td>600</td>
</tr>
</tbody>
</table>
Schematic of Inputs and Outputs

Test Waveforms

Set-Up and Hold

CLOCK

DATA

INPUT

IN-PHASE
OUTPUT
(S1 CLOSED)

OUT OF PHASE
OUTPUT
(S1 CLOSED)

Propagation Delay

Notes:

$V_T = 1.5V$

$C_L$ includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Enable and Disable

$V_{OH}$

$V_T$

$V_{OH}$

$V_T$

$V_{OH}$

$V_T$

$V_{CL}$

$V_T$

$V_{CL}$

Test Load

$V_{CC}$

$S_1$

$R_1$

$C_L$

$R_2$

$V_{OH}$

$V_{CL}$
Switching Waveforms

**Power-Up Reset Waveform**

*The clock input should not be switched from low to high until after time tRESET.*

**Functional Description**

The PAL20RA10 logic array consists of 20 complementary input lines and 80 product-term lines with a programmable fuse link at each intersection (3200 fuses). The product terms are organized into ten groups of eight each. Four of the eight product terms in each group connect into an OR-gate to produce the sum-of-products logic function. The remaining four product terms in each group are used for control functions in the Output Logic Macro Cell (OLMC) as shown in Figure 1.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

**Programmable Set and Reset**

In each cell, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1, the output pin becomes a 0. If the reset product line is high, the register output becomes a logic 0, the output pin becomes a 1. The operation of the programmable set and reset overrides the clock.

**Individually Programmable Register ByPass**

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

**Programmable Clock**

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.
Functional Description (Continued)

PROGRAMMABLE AND HARD-WIRED TRI-STATE OUTPUTS

The PAL20RA10 provides a product term dedicated to output control. There is also an output control pin (Pin 13). The output is enabled if both the output control pin is low and the output control product term is HIGH. If the output control pin is high all outputs will be disabled or if an output control product term is low, then that output will be disabled.

OUTPUT CONTROL ALTERNATIVES

<table>
<thead>
<tr>
<th>Output Control</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Always Enabled</td>
<td><img src="TL/L/8702-6" alt="Diagram" /></td>
</tr>
<tr>
<td>Programmable</td>
<td><img src="TL/L/8702-7" alt="Diagram" /></td>
</tr>
<tr>
<td>Hard-Wired</td>
<td><img src="TL/L/8702-8" alt="Diagram" /></td>
</tr>
<tr>
<td>Combination of Programmable and Hard-Wired</td>
<td><img src="TL/L/8702-9" alt="Diagram" /></td>
</tr>
</tbody>
</table>

PROGRAMMABLE OUTPUT POLARITY

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-or gates shown in the PAL20RA10 Logic Diagram. When the output polarity fuse is blown, the lower input to the exclusive-or gate is high, so the output is active-high. Similarly, when the output polarity fuse is intact, the output is active-low. The programmable output polarity features allows the user a higher degree of flexibility when writing equations.

POWER-UP RESET

The PAL20RA10 device resets all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interferring with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

CLOCK FREQUENCY SPECIFICATION

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_{W high} + t_{W low}) and the minimum “data window” period (t_{SU} + t_{d}). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.
Functional Description (Continued)

Typical Registered Logic Function Without Feedback

Typical Registered Logic Function With Feedback

FIGURE 1. "RA" Output Logic Macrocell Logic Diagram
Output Register Preload

Register preload allows any arbitrary state to be loaded into the PAL output registers. This allows complete logic verification, including states that are impossible or impractical to reach. To use the preload feature, first disable the outputs by bringing \(OE\) high, and present the data at the output pins. A low-level on the preload pin (PL) will then load the data into the registers.

Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format en-
Design Development Support (Continued)

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL20RA10 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

- **Programmable Array Logic Family**
- **Number of Array Inputs**
- **Output Type**
  - RA = Register Asynchronous
- **Number of Outputs**
- **Package Type**
  - N = 24-Pin Plastic DIP
  - J = 24-Pin Ceramic DIP
  - V = 28-Lead Plastic Chip Carrier JEDEC Standard Pinout
  - XV = 28-Lead PLCC Non-JEDEC Standard Pinout
- **Temperature Range**
  - C = Commercial (0°C to +75°C)
  - M = Military (-55°C to +125°C)
JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.
GAL16V8 Generic Array Logic

General Description
The NSC E2CMOSTM GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 20-pin GAL16V8 features 8 programmable Output Logic Macrocells (OLMCs) allowing each TRI-STATE® output to be configured by the user. Additionally, the GAL16V8 is capable of emulating, in a functional/fuse map/parametric compatible device, all common 20-pin PAL® device architectures.

Programming is accomplished using readily available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability and functionality of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features
- Electrically erasable cell technology
- Reconfigurable logic
- Reprogrammable cells
- Guaranteed 100% yields
- High performance E2CMOS technology
  - Low power: 45 mA/90 mA max active
  - High Speed: 20 ns–35 ns max access
- Eight output logic macrocells
  - Maximum flexibility for complex logic designs
  - Also emulates 20-pin PAL devices with full function/fuse map/parametric compatibility
- Preload and power-on reset of all registers
  - 100% functional testability
- Fully supported by National PLANTM development software
- High speed programming algorithm
- Security cell prevents copying logic

PAL Replacement by Device Type

<table>
<thead>
<tr>
<th>“Small-PAL” Mode</th>
<th>“Registered-PAL” Mode</th>
<th>“Medium-PAL” Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>10L8 12L6 14L4 16L2</td>
<td>16R8 16R6 16R4 16L8</td>
<td>16L8</td>
</tr>
<tr>
<td>10H8 12H6 14H4 16H2</td>
<td>16RP8 16RP6 16RP4 16H8</td>
<td>16H8</td>
</tr>
<tr>
<td>10PB 12PB 14PB 16P2</td>
<td>16P8</td>
<td></td>
</tr>
</tbody>
</table>

PAL Replacement by Speed/Power

<table>
<thead>
<tr>
<th>PAL</th>
<th>GAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev</td>
<td>Speed</td>
</tr>
<tr>
<td>B-2</td>
<td>25 ns</td>
</tr>
<tr>
<td>A</td>
<td>25 ns</td>
</tr>
<tr>
<td>B-4</td>
<td>35 ns</td>
</tr>
<tr>
<td>A-2</td>
<td>35 ns</td>
</tr>
<tr>
<td>STD</td>
<td>35 ns</td>
</tr>
</tbody>
</table>

*Shown for Medium PAL products

Block Diagram—GAL16V8
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V\text{CC})</td>
<td>-0.5V to +7.0V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>-2.5V to V\text{CC} + 1.0V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>-2.5V to V\text{CC} + 1.0V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>+100 mA</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td></td>
<td></td>
<td>-65°C to +125°C</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td></td>
<td></td>
<td>-65°C to +150°C</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature</td>
<td></td>
<td></td>
<td>(Soldering, 10 seconds)</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Tolerance</td>
<td></td>
<td></td>
<td>500V</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

### Recommended Operating Conditions

**SUPPLY VOLTAGE AND TEMPERATURE**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{CC}</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>T\text{A}</td>
<td>Operating Free-Air Temperature</td>
<td>0</td>
<td>25</td>
<td>75</td>
<td>°C</td>
</tr>
<tr>
<td>T\text{C}</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### AC Timing Requirements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GAL16V8-20L</th>
<th>GAL16V8-25Q</th>
<th>GAL16V8-35Q</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\text{SU}</td>
<td>Set-Up Time (Input or Feedback before Clock)</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{H}</td>
<td>Hold Time (Input after Clock)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{W}</td>
<td>Clock Pulse Width (High/Low)</td>
<td>12</td>
<td>15</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{CYCLE}</td>
<td>Clock Cycle Period (with Feedback) (Note 3)</td>
<td>30</td>
<td>35</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>f\text{CLK}</td>
<td>Clock Frequency (Note 4)</td>
<td>33.3</td>
<td>28.5</td>
<td>22.2</td>
<td>MHz</td>
</tr>
<tr>
<td>f\text{f}</td>
<td>Input Frequency (Note 5)</td>
<td>50.0</td>
<td>40.0</td>
<td>33.3</td>
<td>ns</td>
</tr>
<tr>
<td>f\text{PPR}</td>
<td>Clock Valid after Power-Up</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 3:** t\text{CYCLE} = t\text{SU} + f\text{CLK}

**Note 4:** f\text{CLK} (with feedback) = (t\text{CYCLE})\text{−}1

f\text{CLK} (without feedback) = (2 t\text{w})\text{−}1

**Note 5:** f\text{f} = (t f)\text{−}1
### Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Temperature Range</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>High Level Input Voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Min</td>
<td></td>
<td>2.0</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; + 1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Low Level Input Voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Min</td>
<td></td>
<td>-1.0</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>High Level Output Voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Min</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Low Level Output Voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Min</td>
<td></td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>High Level Off State Output Current</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Max, V&lt;sub&gt;O&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; (Max)</td>
<td></td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Low Level Off State Output Current</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Max, V&lt;sub&gt;O&lt;/sub&gt; = GND</td>
<td></td>
<td>-10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;I&lt;/sub&gt;</td>
<td>Maximum Input Current</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Max, V&lt;sub&gt;I&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; (Max)</td>
<td></td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;LH&lt;/sub&gt;</td>
<td>High Level Input Current</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Max, V&lt;sub&gt;I&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; (Max)</td>
<td></td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Low Level Input Current</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = Max, V&lt;sub&gt;I&lt;/sub&gt; = GND</td>
<td></td>
<td>-10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*One output at a time for a maximum duration of one second @ 25°C.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>GAL16V8-20L COM/IND</th>
<th>GAL16V8-25Q COM/IND</th>
<th>GAL16V8-30Q COM/IND</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>S1 Closed, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min: 20</td>
<td>Max: 25</td>
<td>Min: 30</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;CLK&lt;/sub&gt;</td>
<td>Clock to Registered Output or Feedback</td>
<td>S1 Closed, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>15</td>
<td>15</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PZXG&lt;/sub&gt;</td>
<td>G↓ to Registered Output Enabled</td>
<td>Active High: S1 Open, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>18</td>
<td>20</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PXG&lt;/sub&gt;</td>
<td>G↑ to Registered Output Disabled</td>
<td>From V&lt;sub&gt;OH&lt;/sub&gt;: S1 Open, C&lt;sub&gt;L&lt;/sub&gt; = 5 pF</td>
<td>18</td>
<td>20</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PZI&lt;/sub&gt;</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>Active High: S1 Open, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;PXI&lt;/sub&gt;</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>From V&lt;sub&gt;OH&lt;/sub&gt;: S1 Open, C&lt;sub&gt;L&lt;/sub&gt; = 5 pF</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;RESET&lt;/sub&gt;</td>
<td>Power-Up to Registered Output High</td>
<td>S1 Closed, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>45</td>
<td>45</td>
<td>45 µs</td>
<td></td>
</tr>
</tbody>
</table>

* -25Q available only in COM/IND operating ranges;
-35Q available only in MIL operating range (for COM/IND, use -25L).
AC Test Load

\[
\begin{align*}
\text{MIL} & \quad R1 = 390 \\
& \quad R2 = 750 \\
\text{COM/IND} & \quad R1 = 200 \\
& \quad R2 = 390
\end{align*}
\]

Test Waveforms

**Setup and Hold**

- Timing Input: 3V
- Data Input: 0V
- Propagation Delay: V_T
- Hold: V_T
- Pulse Width: V_T

**Pulse Width**

- High-Level Pulse Input: V_T
- Low-Level Pulse Input: V_T

**Propagation Delay**

- Input: V_T
- In-Phase Output (S1 Closed): V_T
- Out of Phase Output (S1 Closed): V_T

**Enable and Disable**

- Enable: V_T
- Normally High Output (S1 Open): V_T
- Normally Low Output (S1 Closed): V_T

Notes:

- C_L includes probe and jig capacitance.
- V_T = 1.5V.
- Test inputs have rise and fall times of 5 ns between 0.3V and 2.7V.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Switching Waveforms

Power-Up Reset Waveforms

Input/Output Schematics
**Ordering Information**

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

- **Generic Array Logic Family**
- **Number of Array Inputs**
- **Output Type:** V = Variable Architecture
- **Number of Outputs**
- **Speed:** t\textsubscript{PD} (ns)

<table>
<thead>
<tr>
<th>t\textsubscript{PD} (ns)</th>
<th>Power Versions</th>
<th>Temperature Ranges</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>L</td>
<td>C, I</td>
</tr>
<tr>
<td>25</td>
<td>L</td>
<td>C, I</td>
</tr>
<tr>
<td>25</td>
<td>Q</td>
<td>C, I</td>
</tr>
<tr>
<td>35</td>
<td>Q</td>
<td>C, I</td>
</tr>
</tbody>
</table>

- **Power Version:**
  - Q = Quarter Power (45 mA)
  - L = Half Power (90 mA)

- **Package Type:**
  - N = 20-Pin Plastic DIP
  - J = 20-Pin Ceramic DIP
  - V = 20-Lead Plastic Chip Carrier

- **Temperature Range:**
  - C = Commercial (0°C to +75°C)
  - I = Industrial (−40°C to +85°C)
  - M = Military (−55°C to +125°C)

---

**GAL16V8 Block Diagram—DIP Connections**

![Block Diagram](image)

**FIGURE 1**
**Functional Description**

The GAL logic array consists of a programmable AND array with fixed OR-gate connections, similar to the bipolar PAL architecture. The logic array is organized as 16 complementary input lines crossing 64 "product term" lines with a programmable E2PROM cell at each intersection (2048 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines "connected" to it are in the high logic state.

The 64 product terms are organized into eight output groups with eight terms each. Seven or eight of the product terms in each output group feed into an OR-gate to produce each output logic function; one of the product terms may instead be used to control the associated TRI-STATE device output. The fundamental transfer function of each GAL output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL programming patterns.

As shown in the GAL16V8 Block Diagram (Figure 1), a total of eight output logic functions are available. Each of the AND/OR logic functions feeds into an "output logic macrocell" (OLMC). The eight OLMCs control the flow of input and output signals between the logic array and the device's I/O pins.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-low or active-high (adjusted before the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

All of the possible I/O configurations of the GAL16V8 are classified into three basic modes: "Small-PAL" mode, "Registered-PAL" mode and "Medium-PAL" mode. These modes correspond to the architectures of the PAL families which the GAL16V8 can emulate. The modes determine the mixture of OLMC configurations which can be selected for the device. The OLMC Selection table (Table I) lists which functions can be selected on the device pin 1 and pins 11 through 19 for each of the three modes. The logic diagrams in Figure 3 illustrate these OLMC functions.

"OUTPUT" represents the always-active combinatorial output configuration available in the "Small-PAL" mode. "REGISTER" is the registered output with register feedback available in the "Registered-PAL" mode. "I/O" is the combinatorial bidirectional I/O available in "Registered-PAL" and "Medium-PAL" modes. "TRI-STATE" is the TRI-STATE combinational output function appearing on pins 12 and 19 in the "Medium-PAL" mode. "INPUT" in Table I denotes an OLMC used as a dedicated input only.

*Applies to both 20-pin DIP and 20-lead PLCC packages for GAL16V8.

---

**20-Lead PLCC Connection Diagram**

![Diagram of 20-Lead PLCC Connection](image)
### OLMC Selection Table

**TABLE I**

<table>
<thead>
<tr>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>CLOCK</td>
<td>INPUT</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>TRI-STATE**</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>OUTPUT ENABLE (G)</td>
<td>INPUT</td>
</tr>
</tbody>
</table>

*Active combinatorial output.

**TABLE II**

<table>
<thead>
<tr>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot;</th>
<th>&quot;Medium-PAL&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>OUTPUT ENABLE (G)</td>
<td>INPUT</td>
</tr>
<tr>
<td>10L8</td>
<td>12L6</td>
<td>16L2</td>
</tr>
<tr>
<td>10H8</td>
<td>12H6</td>
<td>16H2</td>
</tr>
<tr>
<td>10P8</td>
<td>12P6</td>
<td>16P2</td>
</tr>
<tr>
<td>16R8</td>
<td>16R6</td>
<td>16R4</td>
</tr>
<tr>
<td>16RP8</td>
<td>16RP6</td>
<td>16RP4</td>
</tr>
<tr>
<td>16H8</td>
<td>16P8</td>
<td></td>
</tr>
</tbody>
</table>

*Active combinatorial output.

**TRI-STATE combinatorial output.**
OLMC Configurations

OUTPUT (Active Combinatorial Output)

REGISTER (Registered Output)

I/O (Combinatorial Input/Output)

TRI-STATE (TRI-STATE Combinatorial Output)

FIGURE 3
Functional Description (Continued)

In the "Small-PAL" and "Medium-PAL" modes (Table I), pins 1 and 11 are always dedicated inputs. In the "Registered-PAL" mode, however, pin* 1 becomes the clock input controlling all OLMC registers, and pin* 11 becomes the output enable (G) input controlling the TRISTATE outputs of all registered PALs. Within the "Small-PAL" and "Registered-PAL" modes in Table I, the functions of pins 12 through 19 can be selected individually from either of the two functions listed. For example, in "Registered-PAL" mode, pins 12 through 19 can each be designated as either a register output or a combinatorial I/O. The "Medium-PAL" mode represents a single fixed configuration used to emulate combinatorial medium PAL devices (16L8, 16H8, 16P8).

Table II lists the bipolar PAL products which the GAL16V8 can emulate, and the specific input/output configurations used. This is just a subset, however, of all the configurations provided in Table I.

All registers in a GAL device are reset to the low state upon power-up. The active-low outputs, in turn, assume high logic levels (if enabled) regardless of the selected output polarity. This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, tpR) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or VCC (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

*Applies to both 20-pin DIP and 20-lead PCC packages for GAL16V8.

Clock/Input Frequency Specifications

The clock frequency (fCLK) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e. based only on external inputs), the minimum required cycle period (fCLK<sup>-1</sup> without feedback) is defined as the greater of the minimum clock period (t<sub>W</sub> high + t<sub>W</sub> low) and the minimum "data window" period (t<sub>SU</sub> + t<sub>SD</sub>). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f<sub>CYCLE</sub> = f<sub>CLK</sub><sup>-1</sup> with feedback) is defined as f<sub>CLK</sub> + t<sub>SU</sub>. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (f<sub>I</sub>) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The f<sub>I</sub> specification is derived as the inverse of the combinatorial propagation delay (t<sub>PD</sub>).

Design Development Support

A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible "cell-map" (analogous to a PAL "fuse-map"). The industry-standard JEDEC format ensures that the resulting cell-map file can be downloaded into a variety of programmable equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as PLAN software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMC are provided for direct map editing and diagnostic purposes (see "Programming Details"). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.
Security Cell
A security cell is provided on all GAL16V8 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature
Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information isread out of the device using the normal preprogram verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National’s PLAN development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase
The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection
GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latchting.

Manufacturer Testing
Because of E²CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through each device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload
The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all E²CMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the Register Preload Waveform in Figure 5, the preload sequence must not begin until the normal power-up reset operation has completed (after time tRESET). The device is placed into preload mode by raising the “PRLD” input (pin* 11) to voltage VIESS, as specified in the Register Preload Specifications (Table III).

To preload the OLMC registers, a series of data bits are shifted into the device on the “SIN” input (pin* 9), one bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the “CLK” input (pin* 1). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then “upward” through all remaining registered OLMCs in pin-number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in Figure 4.

As the data series is shifted into the SIN input, the contents of all registers (in registered OLMCs) are shifted “upward” and out onto the “SOUT” output (pin* 12). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the SOUT pin of each chip is connected to the SIN pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into SIN or out of SOUT, VIL/VOL = register reset (0), and VIL/VOL = register set (1). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

*Applies to both 20-pin DIP and 20-lead PCC Packages for GAL16V8.
Register Preload Specifications

**TABLE III**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input Voltage (High)</td>
<td></td>
<td>2.40</td>
<td></td>
<td></td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Voltage (Low)</td>
<td></td>
<td>0.00</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IES}$</td>
<td>Registered Preload Input Voltage</td>
<td></td>
<td>14.5</td>
<td>15</td>
<td>15.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output Voltage (High) (Note 1)</td>
<td>$I_{OL} \leq 12$ mA</td>
<td>0.00</td>
<td>±1</td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Voltage (Low) (Note 1)</td>
<td></td>
<td>0.00</td>
<td>0.50</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}, I_{IL}$</td>
<td>Input Current (Programming)</td>
<td></td>
<td>±1</td>
<td>±10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>High Level Output Current (Note 1)</td>
<td>$V_{OH} \leq V_{CC}$</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$t_{PW}$</td>
<td>Verify Pulse Width</td>
<td></td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{D}$</td>
<td>Pulse Sequence Delay</td>
<td></td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{RESET}$</td>
<td>Register Reset Time from Valid $V_{CC}$</td>
<td></td>
<td>45</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**Note 1:** The $S_{DOUT}$ output buffer is an open drain output during preload. This pin should be terminated to $V_{CC}$ with a 10 kΩ resistor.

Register Preload Waveforms

**FIGURE 4. Output Register Preload Pinout**

**FIGURE 5**
Programming Details

Understanding the information in this section is not essential when using approved programming equipment and software for developing GAL designs. This is a more thorough disclosure of the GAL architecture provided for direct JEDEC cell-map editing and diagnostic purposes. This section alone, however, does not contain sufficient information to implement the GAL programming algorithm. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

As mentioned in the Functional Description, the OLMC is responsible for selecting input and/or output paths, registered vs. combinatorial outputs, active-high or low polarity, and common vs. locally-controlled TRI-STATE control. Additionally, the OLMCs select between alternate logic array input paths to maintain JEDEC cell-map compatibility with either "small-PAL" or "medium-PAL" logic arrays.

The various configurations of the OLMCs are controlled by a set of programmable "architecture" cells, separate from the logic-defining array cells. Each GAL device contains two "global" architecture cells, "SYN" and "AC0", which affect all OLMCs. Each of the device's eight OLMCs also contains two "local" cells, "AC1" and "XOR". The OLMC Logic Diagram in Figure 6 shows how the architecture cells select the different paths through the OLMC.

The SYN bit controls whether a device will have any registered outputs (SYN = 0) or will be purely combinatorial (SYN = 1). The SYN bit determines whether device pins* 1 and 11 are used as the clock and global TRI-STATE control inputs (SYN = 0) or whether they are ordinary inputs (SYN = 1). The AC0 bit selects between the "Small-PAL" mode and the "Medium/Registered-PAL" modes. The function of the AC1 bits depend on the state of the AC0 bit. In "Small-PAL" mode (AC0 = 0), the AC1 bit in each OLMC determines whether associated device pin is an output (AC1 = 0) or an input (AC1 = 1). In "Registered-PAL" mode (AC0 = 1), the AC1 bit determines whether each OLMC is registered (AC1 = 0) or combinatorial (AC1 = 1). In "Medium-PAL" mode (AC0 = 1), the AC1 bits in all OLCMs must be set to 1 (combinatorial). All of the valid architecture bit configurations are shown in the OLMC Architecture table (Table IV), which has the same familiar format used in the OLMC Selection table (Table I).

Independent of SYN, AC0 and the AC1 bits, the XOR bit in each OLMC selects between active-low (XOR = 0) or active-high (XOR = 1) output polarity.

*Applies to both 20-pin DIP and 20-lead PCQ packages for GAL16V8.
OLMC Logic Diagram

FIGURE 6

OLMC Architecture Programming

TABLE IV

<table>
<thead>
<tr>
<th>Function</th>
<th>“Small-PAL” Mode</th>
<th>“Registered-PAL” Mode</th>
<th>“Medium-PAL” Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>INPUT INPUT</td>
<td>2,3</td>
<td>INPUT</td>
</tr>
<tr>
<td>***Pin 19</td>
<td>OUTPUT* INPUT</td>
<td>6,7</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>***Pin 18</td>
<td>OUTPUT* INPUT</td>
<td>10,11</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>***Pin 17</td>
<td>OUTPUT* INPUT</td>
<td>14,15</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>***Pin 16</td>
<td>OUTPUT* NC</td>
<td>18,19</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>***Pin 15</td>
<td>OUTPUT* NC</td>
<td>22,23</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>***Pin 14</td>
<td>OUTPUT* INPUT</td>
<td>26,27</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>***Pin 13</td>
<td>OUTPUT* INPUT</td>
<td>30,31</td>
<td>REGISTER I/O</td>
</tr>
<tr>
<td>Pin 11</td>
<td>INPUT INPUT</td>
<td>30,31</td>
<td>INPUT</td>
</tr>
</tbody>
</table>

AC<sub>1</sub> = 0    AC<sub>1</sub> = 1    AC<sub>1</sub> = 1
SYN = 1, AC0 = 0     SYN = 0, AC0 = 1     SYN = 1, AC0 = 1

All outputs are combinatorial and always active.  All I/O pins are combinatorial.

Note: Pin numbers above apply to both 20-pin DIP and 20-lead PCC packages for GAL16V8.

Note 1: All even and odd numbered JEDEC input line numbers correspond to true and complement array inputs, respectively.

*Active combinatorial output.
**Tri-STATE combinatorial output.
***AC<sub>1</sub> applies to these I/O pins only.
USER ELECTRONIC SIGNATURE WORD:

<table>
<thead>
<tr>
<th>2056</th>
<th>2064</th>
<th>2072</th>
<th>2080</th>
<th>2088</th>
<th>2096</th>
<th>2104</th>
<th>2112</th>
<th>2119</th>
</tr>
</thead>
<tbody>
<tr>
<td>BYTE 0</td>
<td>BYTE 1</td>
<td>BYTE 2</td>
<td>BYTE 3</td>
<td>BYTE 4</td>
<td>BYTE 5</td>
<td>BYTE 6</td>
<td>BYTE 7</td>
<td></td>
</tr>
<tr>
<td>MSB</td>
<td>LSB</td>
<td>MSB</td>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SYN=2192
ACO=2193

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

FIGURE 7
Typical Performance Characteristics

- Normalized $t_{PD}$ vs Supply Voltage
- Normalized $I_{CC}$ (Max) vs Supply Voltage
- Normalized $t_{SU}$ vs Supply Voltage
- Normalized $I_{OL}$ vs $V_{OL}$
- Normalized $I_{OH}$ vs $V_{OH}$

Supply Voltage (V) range: 4.0 to 6.0
Ambient Temperature (°C) range: -55 to 125

Graphs show the normalized performance characteristics for various conditions.
GAL20V8 Generic Array Logic

General Description
The NSC E2CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL20V8 features 8 programmable Output Logic Macrocells (OLMCs) allowing each TRI-STATE® output to be configured by the user. Additionally, the GAL20V8 is capable of emulating, in a functional/fuse map/parametric compatible device, the most popular 24-pin PAL® device architectures.

Programming is accomplished using readily available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability and functionality of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - Guaranteed 100% yields
- High performance E2CMOS technology
  - Low power: 45 mA/90 mA max active
  - High speed: 20 ns–35 ns max access
- Eight output logic macrocells
  - Maximum flexibility for complex logic designs
  - Also emulates 24-pin PAL devices with full function/fuse map/parametric compatibility
- Preload and power-on reset of all registers
  - 100% functional testability
- Fully supported by National PLAN™ development software
- High speed programming algorithm
- Security cell prevents copying logic

### PAL Replacement by Device Type

<table>
<thead>
<tr>
<th>“Small-PAL” Mode</th>
<th>“Registered-PAL” Mode</th>
<th>“Medium-PAL” Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>14L8</td>
<td>16L6, 18L4, 20L2</td>
<td>20L8</td>
</tr>
<tr>
<td>14L8</td>
<td>16L6, 18L4, 20H2</td>
<td>20RP6</td>
</tr>
<tr>
<td>14P8</td>
<td>16P6, 18P4, 20P2</td>
<td>20RP4</td>
</tr>
</tbody>
</table>

### PAL Replacement by Speed/Power

<table>
<thead>
<tr>
<th>PAL</th>
<th>Rev</th>
<th>Speed</th>
<th>Power*</th>
<th>GAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev</td>
<td>Speed</td>
<td>Power*</td>
<td>GAL</td>
<td></td>
</tr>
<tr>
<td>B-2</td>
<td>25 ns</td>
<td>105 mA</td>
<td>25L or 20L (90 mA) or 25Q (45 mA)</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>25 ns</td>
<td>210 mA</td>
<td>25L or 20L (90 mA)</td>
<td></td>
</tr>
<tr>
<td>B-4</td>
<td>35 ns</td>
<td>55 mA</td>
<td>30Q (45 mA)</td>
<td></td>
</tr>
<tr>
<td>A-2</td>
<td>35 ns</td>
<td>105 mA</td>
<td>30Q (45 mA)</td>
<td></td>
</tr>
<tr>
<td>STD</td>
<td>35 ns</td>
<td>210 mA</td>
<td>25L (90 mA)</td>
<td></td>
</tr>
</tbody>
</table>

*Shown for Medium PAL products.

Block Diagram—GAL20V8

![Block Diagram](image-url)
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) (Note 2)  
Input Voltage (Note 2)  
Off-State Output Voltage (Note 2)  
Output Current  
Storage Temperature  
Ambient Temperature with Power Applied  
Junction Temperature  
Lead Temperature (Soldering, 10 seconds)  
ESD Tolerance  

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Nom</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>4.5</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>0</td>
<td>25</td>
<td>75</td>
<td>-40</td>
</tr>
<tr>
<td>TC</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

AC TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GAL20V8-20L</th>
<th>GAL20V8-25Q</th>
<th>GAL20V8-35Q</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>COM/IND</td>
<td>MIL*</td>
<td>COM/IND</td>
<td>MIL*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>tsu</td>
<td>Setup Time (Input or Feedback before Clock)</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>th</td>
<td>Hold Time (Input after Clock)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>tw</td>
<td>Clock Pulse Width (High/Low)</td>
<td>12</td>
<td>15</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>tCYCLE</td>
<td>Clock Cycle Period (with Feedback) (Note 3)</td>
<td>30</td>
<td>35</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback</td>
<td>33.3</td>
<td>26.5</td>
<td>22.2</td>
</tr>
<tr>
<td></td>
<td>Without Feedback</td>
<td>41.6</td>
<td>33.3</td>
<td>33.3</td>
<td></td>
</tr>
<tr>
<td>fI</td>
<td>Input Frequency (Note 5)</td>
<td>50.0</td>
<td>40.0</td>
<td>33.3</td>
<td></td>
</tr>
<tr>
<td>tVR</td>
<td>Clock Valid after Power-Up</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

*25Q available only in COM/IND operating ranges;  
-30L available only in MIL operating range (for COM/IND, use -25L).

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preloading operations according to the applicable specification.

Note 3: tCYCLE = tsu + fCLK

Note 4: fCLK (with feedback) = (tCYCLE)^-1

fCLK (without feedback) = (2 tw)^-1

Note 5: t = (tpO)^-1

2-146
### Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Temperature Range</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OZH}$</td>
<td>High Level Off-State Output Current</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OZL}$</td>
<td>Low Level Off-State Output Current</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$V_{CC} + 1$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short Circuit Current</td>
<td>$V_{CC} = 5.0V, V_O = 0V$</td>
<td>$GND$</td>
<td>$-30$</td>
<td>$-130$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>Quarter Power (GAL20V8-25Q,-35Q)</td>
<td>$f = 15,\text{MHz}$</td>
<td>45</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Half Power (GAL20V8-20L,-25L)</td>
<td>$f = 15,\text{MHz}$</td>
<td>90</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$C_I$</td>
<td>Input Capacitance</td>
<td>$V_{CC} = 5.0V, V_I = 2.0V$</td>
<td>$GND$</td>
<td>8</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{I/O}$</td>
<td>I/O Capacitance</td>
<td>$V_{CC} = 5.0V, V_{I/O} = 2.0V$</td>
<td>$GND$</td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

*One output at a time for a maximum duration of one second @ 25°C.*

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>GAL20V8-20L</th>
<th>GAL20V8-25Q</th>
<th>GAL20V8-35Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>S1 Closed, $C_L = 50,\text{pF}$</td>
<td>20</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>$t_{CLK}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>S1 Closed, $C_L = 50,\text{pF}$</td>
<td>15</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>$t_{PZG}$</td>
<td>$g\downarrow$ to Registered Output Enabled</td>
<td>Active High: S1 Open, $C_L = 50,\text{pF}$</td>
<td>18</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Active Low: S1 Closed $C_L = 50,\text{pF}$</td>
<td>18</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>$t_{PXG}$</td>
<td>$g\uparrow$ to Registered Output Disabled</td>
<td>From $V_{OH}$: S1 Open, $C_L = 5,\text{pF}$</td>
<td>18</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>From $V_{OL}$: S1 Closed $C_L = 5,\text{pF}$</td>
<td>18</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>$t_{PXI}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>Active High: S1 Open, $C_L = 50,\text{pF}$</td>
<td>20</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Active Low: S1 Closed $C_L = 50,\text{pF}$</td>
<td>20</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>$t_{PXZI}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>From $V_{OH}$: S1 Open, $C_L = 5,\text{pF}$</td>
<td>20</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>From $V_{OL}$: S1 Closed $C_L = 5,\text{pF}$</td>
<td>20</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>$t_{RESET}$</td>
<td>Power-Up to Registered Output High</td>
<td>S1 Closed $C_L = 50,\text{pF}$</td>
<td>45</td>
<td>45</td>
<td>45</td>
</tr>
</tbody>
</table>

* -25Q available only in COM/IND operating ranges; -30L available only in MIL operating range (for COM/IND, use -2SL).
AC Test Load

![AC Test Load Diagram]

Test Waveforms

Setup and Hold

Timing Input

Input Rise Time

Data Input

High-Level Pulse Input

Pulse Width

Low-Level Pulse Input

Propagation Delay

Enable and Disable

Notes:

$C_l$ includes probe and jig capacitance.

$V_T = 1.5V$.

Test inputs have rise and fall times of 5 ns between 0.3V and 2.7V.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Switching Waveforms

Power-Up Reset Waveforms

Input/Output Schematics
Input/Output Schematics (Continued)

Phased Output Turn-On Circuit

Ordering Information
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

<table>
<thead>
<tr>
<th>Generic Array Logic Family</th>
<th>Number of Array Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Type:</th>
<th>Number of Outputs</th>
<th>Speed: ( t_{PD} ) (ns)</th>
<th>Power Versions</th>
<th>Temperature Ranges</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V ) = Variable Architecture</td>
<td></td>
<td>20</td>
<td>L</td>
<td>C, I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>L</td>
<td>C, I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>Q</td>
<td>C, I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>35</td>
<td>Q</td>
<td>C, I</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Version:</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Q ) = Quarter Power (45 mA)</td>
</tr>
<tr>
<td>( L ) = Half Power (90 mA)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package Type:</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N ) = 24-Pin Plastic DIP</td>
</tr>
<tr>
<td>( J ) = 24-Pin Ceramic DIP</td>
</tr>
<tr>
<td>( V ) = 24-Lead Plastic Chip Carrier</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Temperature Range:</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C ) = Commercial (0°C to +75°C)</td>
</tr>
<tr>
<td>( I ) = Industrial (-40°C to +85°C)</td>
</tr>
<tr>
<td>( M ) = Military (-55°C to +125°C)</td>
</tr>
</tbody>
</table>
The GAL logic array consists of a programmable AND array with fixed OR-gate connections, similar to the bipolar PAL architecture. The logic array is organized as 20 complementary input lines crossing 64 “product term” lines with a programmable E²PROM cell at each intersection (2560 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines “connected” to it are in the high logic state.

The 64 product terms are organized into eight output groups with eight terms each. Seven or eight of the product terms in each output group feed into an OR-gate to produce each output function logic; one of the product terms may instead be used to control the associated TRI-STATE device output. The fundamental transfer function of each GAL output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL programming patterns.

As shown in the GAL20V8 Block Diagram (Figure 1), a total of eight output logic functions are available. Each of the AND/OR logic functions feeds into an “output logic macro-cell” (OLMC). The eight OLMCs control the flow of input and output signals between the logic array and the device’s I/O pins.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function’s output polarity may be designated active-low or active-high (adjusted before the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

All of the possible I/O configurations of the GAL20V8 are classified into three basic modes: “Small-PAL” mode, “Registered-PAL” mode and “Medium-PAL” mode. These modes correspond to the architectures of the PAL families which the GAL20V8 can emulate. The modes determine the mixture of OLMC configurations which can be selected for the device. The OLMC Selection table (Table I) lists which functions can be selected on device pins* 1, 13 and 15 through 22 for each of the three modes. The logic diagrams in Figure 3 illustrate these OLMC functions.

“OUTPUT” represents the always-active combinatorial output configuration available in the “Small-PAL” mode. “REGISTER” is the registered output with register feedback available in the “Registered-PAL” mode. “I/O” is the combinatorial bidirectional I/O available in “Registered-PAL” and “Medium-PAL” modes. “TRI-STATE” is the TRI-STATE combinational output function appearing on pins* 15 and 22 in the “Medium-PAL” mode. “INPUT” in Table I denotes an OLMC used as a dedicated input only.

In the “Small-PAL” and “Medium-PAL” modes (Table I), pins* 1 and 13 are always dedicated inputs. In the “Registered-PAL” mode, however, pin* 1 becomes the clock input controlling all OLMC registers, and pin* 13 becomes the output enable (G) input controlling the TRI-STATE outputs of all registered OLMCs. Within the “Small-PAL” and “Registered-PAL” modes in Table I, the functions of pins* 15 through 22 can be selected individually from either of the two functions listed. For example, in “Registered-PAL” mode, pins* 15 through 22 can each be designated as either a registered output or a combinational I/O. The “Medium-PAL” mode represents a single fixed configuration used to emulate combinatorial medium PAL devices (20L8, 20H8, 20P8).

Table II lists the bipolar PAL products which the GAL20V8 can emulate, and the specific input/output configurations used. This is just a subset, however, of all the configurations provided in Table I.

All registers in a GAL device are reset to the low state upon power-up. The active-low outputs, in turn, assume high logic levels (if enabled) regardless of the selected output polarity. This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, tDR) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or VCC (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

* Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PCC Connection Diagram for conversion.
Clock/Input Frequency Specifications

The clock frequency \( f_{CLK} \) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period \( (f_{CLK}^{-1} \text{ without feedback}) \) is defined as the greater of the minimum clock period \( (t_{\text{high}} + t_{\text{low}}) \) and the minimum "data window" period \( (t_{\text{SU}} + t_{\text{H}}) \). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period \( (f_{\text{CYCLE}} = f_{CLK}^{-1} \text{ with feedback}) \) is defined as \( t_{\text{CLK}} + t_{\text{SU}} \). This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency \( f_l \) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The \( f_l \) specification is derived as the inverse of the combinatorial propagation delay \( (t_{PD}) \).

Design Development Support

A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible "cell-map" (analogous to a PAL "fuse-map"). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into a variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as PLAN software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMC are provided for direct map editing and diagnostic purposes (see "Programming Details"). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.
**OLMC Selection Table**

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>TRI-STATE**</td>
</tr>
<tr>
<td>INPUT</td>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT</td>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT</td>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT</td>
<td>OUTPUT ENABLE</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
</tbody>
</table>

* Active combinatorial output
**TRI-STATE combinatorial output

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-pin PCC Connection Diagram for conversion.

**PAL Replacement Configurations**

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>REGISTER</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>REGISTER</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>REGISTER</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>REGISTER</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>REGISTER</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>REGISTER ENABLE</td>
<td>INPUT</td>
</tr>
</tbody>
</table>

* Active combinatorial output.
**TRI-STATE combinatorial output

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-pin PCC Connection Diagram for conversion.
OLMC Configurations

OUTPUT (Active Combinatorial Output)

REGISTER (Registered Output)

I/O (Combinatorial Input/Output)

TRI-STATE (TRI-STATE Combinatorial Output)

FIGURE 3
Security Cell
A security cell is provided on all GAL20V8 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature
Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National’s PLAN development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase
The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection
GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Manufacturer Testing
Because of E2CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload
The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all E2CMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the Register Preload Waveform in Figure 5, the preload sequence must not begin until the normal power-up reset operation has completed (after time t\textsubscript{RESET}). The device is placed into preload mode by raising the "PRLD" input (pin* 13) to voltage $V_{IES}$, as specified in the Register Preload Specifications (Table III).

To preload the OLMC registers, a series of data bits are shifted into the device on the "SDIN" input (pin* 11), one bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the "DCLK" input (pin* 1). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then "upward" through all remaining registered OLMCs in pin-number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in Figure 4.

*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PCC Connection Diagram for conversion.
Register Preload (Continued)
As the data series is shifted into the \( S_{\text{DIN}} \) input, the contents of all registers (in registered OLMCs) are shifted "upward" and out onto the "\( S_{\text{DOUT}} \)" output (pin \( * \) 15). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the \( S_{\text{DOUT}} \) pin of each chip is connected to the \( S_{\text{DIN}} \) pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into \( S_{\text{DIN}} \) or out of \( S_{\text{DOUT}} \), \( V_{\text{IL}}/V_{\text{OL}} = \text{register reset (0)} \), and \( V_{\text{IH}}/V_{\text{OH}} = \text{register set (1)} \). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

* Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PCC Connection Diagram for conversion.

** The \( S_{\text{DOUT}} \) output buffer is an open drain output during preload. This pin should be terminated to \( V_{\text{CC}} \) with a 10 k\( \Omega \) resistor.

FIGURE 4. Output Register Preload Pinout

Register Preload Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IH}} )</td>
<td>Input Voltage (High)</td>
<td>2.40</td>
<td>( V_{\text{CC}} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IL}} )</td>
<td>Input Voltage (Low)</td>
<td>0.00</td>
<td>0.50</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IES}} )</td>
<td>Register Preload Input Voltage</td>
<td>14.5</td>
<td>15</td>
<td>15.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{OH}} )</td>
<td>Output Voltage (High) (Note 1)</td>
<td>( V_{\text{CC}} )</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{OL}} )</td>
<td>Output Voltage (Low) (Note 1)</td>
<td>( I_{\text{OL}} \leq 12 \text{ mA} )</td>
<td>0.00</td>
<td>0.50</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{IH}}, I_{\text{IL}} )</td>
<td>Input Current (Programming)</td>
<td>( \pm 1 )</td>
<td>( \pm 10 )</td>
<td>( \mu \text{A} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OH}} )</td>
<td>High Level Output Current (Note 1)</td>
<td>( V_{\text{OH}} \leq V_{\text{CC}} )</td>
<td>10</td>
<td>( \mu \text{A} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{PWW}} )</td>
<td>Verify Pulse Width</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{D}} )</td>
<td>Pulse Sequence Delay</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{RESET}} )</td>
<td>Register Reset Time from Valid ( V_{\text{CC}} )</td>
<td>45</td>
<td>45</td>
<td>( \mu \text{s} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The \( S_{\text{DOUT}} \) output buffer is an open drain output during preload. This pin should be terminated to \( V_{\text{CC}} \) with a 10 k\( \Omega \) resistor.

Register Preload Waveforms

**FIGURE 5**

**The \( S_{\text{DOUT}} \) output buffer is an open drain output during preload. This pin should be terminated to \( V_{\text{CC}} \) with a 10 k\( \Omega \) resistor.**
OLMC Logic Diagram

OLMC Architecture Programming

**TABLE IV**

<table>
<thead>
<tr>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>INPUT</td>
<td>Pin 23</td>
<td>INPUT</td>
<td>Pin 22</td>
<td>OUTPUT*</td>
</tr>
<tr>
<td></td>
<td>2,3</td>
<td></td>
<td>6, 7</td>
<td></td>
<td>10, 11</td>
</tr>
<tr>
<td><strong>Pin 22</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 21</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 20</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td><strong>Pin 20</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 19</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 18</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td><strong>Pin 19</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 18</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 17</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td><strong>Pin 18</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 17</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 16</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td><strong>Pin 17</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 16</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 15</strong></td>
<td><strong>OUTPUT</strong></td>
</tr>
<tr>
<td><strong>Pin 16</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 15</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 14</strong></td>
<td><strong>INPUT</strong></td>
</tr>
<tr>
<td><strong>Pin 15</strong></td>
<td><strong>OUTPUT</strong></td>
<td><strong>Pin 14</strong></td>
<td><strong>INPUT</strong></td>
<td><strong>Pin 13</strong></td>
<td><strong>INPUT</strong></td>
</tr>
<tr>
<td>AC1n = 0</td>
<td>AC1n = 1</td>
<td>AC1n = 0</td>
<td>AC1n = 1</td>
<td>AC1n = 1</td>
<td>AC1n = 1</td>
</tr>
<tr>
<td>SYN = 1, AC0 = 0</td>
<td></td>
<td>SYN = 0, AC0 = 1</td>
<td></td>
<td>SYN = 1, AC0 = 1</td>
<td></td>
</tr>
</tbody>
</table>

All outputs are combinatorial and always active.

At least one output is registered.

All I/O pins are combinatorial.

Note 1: All even and odd numbered JEDEC input line numbers correspond to true and complement array inputs, respectively.

*Active combinatorial output.

**TRI-STATE combinatorial output.

***AC1n applies to these I/O pins only.

*Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PCC Connection Diagram for conversion.

FIGURE 6
GAL20V8 Logic Diagram

DIP PIN NUMBERS - PRODUCT LINE FIRST CELL NUMBERS - INPUT LINE NUMBERS

FIGURE 7
Programming Details

Understanding the information in this section is not essential when using approved programming equipment and software for developing GAL designs. This is a more thorough disclosure of the GAL architecture provided for direct JEDEC cell-map editing and diagnostic purposes. This section alone, however, does not contain sufficient information to implement the GAL programming algorithm. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

As mentioned in the Functional Description, the OLMC is responsible for selecting input and/or output paths, registered vs. combinatorial outputs, active-high or low polarity, and common vs. locally-controlled TRI-STATE control. Additionally, the OLMCs select between alternate logic array input paths to maintain JEDEC cell-map compatibility with either "small-PAL" or "medium-PAL" logic arrays.

The various configurations of the OLMCs are controlled by a set of programmable "architecture" cells, separate from the logic-defining array cells. Each GAL device contains two "global" architecture cells, "SYN" and "AC0", which affect all OLMCs. Each of the device's eight OLMCs also contains two "local" cells, "AC1" and "XOR". The OLMC Logic Diagram in Figure 6 shows how the architecture cells select the different paths through the OLMC.

The SYN bit controls whether a device will have any registered outputs (SYN = 0) or will be purely combinatorial (SYN = 1). The SYN bit determines whether device pins* 1 and 13 are used as the clock and global TRI-STATE control inputs (SYN = 0) or whether they are ordinary inputs (SYN = 1). The AC0 bit selects between the "Small-PAL" mode and the "Medium/Registered-PAL" modes. The function of the AC1 bits depend on the state of the AC0 bit. In "Small-PAL" mode (AC0 = 0), the AC1 bit in each OLMC determines whether the associated device pin is an output (AC1 = 0) or an input (AC1 = 1). In "Registered-PAL" mode (AC0 = 1), the AC1 bit determines whether each OLMC is registered (AC1 = 0) or combinatorial (AC1 = 1). In "Medium-PAL" mode (AC0 = 1), the AC1 bits in all OLMCs must be set to 1 (combinatorial). All of the valid architecture bit configurations are shown in the OLMC Architecture table (Table IV), which has the same familiar format used in the OLMC Selection table (Table I).

Independent of SYN, AC0 and the AC1 bits, the XOR bit in each OLMC selects between active-low (XOR = 0) or active-high (XOR = 1) output polarity.

* Applies to 24-pin DIP packages for GAL20V8; refer to the 28-lead PCC Connection Diagram for conversion.
Typical Performance Characteristics

- Normalized $t_{PD}$ vs Supply Voltage
- Normalized $t_{PD}$ vs Temperature
- Normalized $I_{CC \text{ Max}}$ vs Supply Voltage
- Normalized $t_{CLK}$ vs Supply Voltage
- Normalized $t_{CLK}$ vs Temperature
- Normalized $t_{SU}$ vs Supply Voltage
- Normalized $t_{SU}$ vs Temperature
- $I_{O\text{L}}$ vs $V_{OL}$
- $I_{OH}$ vs $V_{OH}$

Supply Voltage (V):
- 1.3
- 1.2
- 1.1
- 1.0
- 0.9
- 0.8

Ambient Temperature (°C):
- -55
- 25
- 85
- 125

Normalized $t_{PD}$:
- 1.3
- 1.2
- 1.1
- 1.0

Normalized $I_{CC \text{ Max}}$:
- 1.3
- 1.2
- 1.1
- 1.0
- 0.9
- 0.8

Normalized $t_{SU}$:
- 1.3
- 1.2
- 1.1
- 1.0

Normalized $t_{CLK}$:
- 1.3
- 1.2
- 1.1
- 1.0

$I_{O\text{L}}$ (mA):
- 210
- 180
- 150
- 120
- 90
- 60
- 30

$I_{OH}$ (mA):
- 100
- 80
- 60
- 40
- 20
- 0

$V_{OL}$ (V):
- 2.0
- 3.0
- 4.0

$V_{OH}$ (V):
- 0
- 1.0
- 2.0
- 3.0
- 4.0
**GAL16V8A-10, -12, -15, -20**

**Generic Array Logic**

**General Description**

The NSC E²CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 20-pin GAL16V8A features 8 programmable Output Logic Macrocells (OLMCs) allowing each TRI-STATE® output to be configured by the user. Additionally, the GAL16V8A is capable of emulating, in a functional/fuse map/parametric compatible device, all common 20-pin PAL® device architectures.

Programming is accomplished using readily available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability and functionality of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

### Features

- High performance E²CMOS technology
  - 10 ns maximum propagation delay
  - \( f_{CLK} = 62.5 \text{ MHz} \)
  - 8 ns maximum from clock input to data output
  - TTL compatible 24 mA outputs
  - UltraMOS® III advanced CMOS technology
- 36% reduction in power
  - 115 mA max \( I_{CC} \)
- Electrally erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (≤50 ms)
  - 20 year data retention
- Eight output logic macrocells
  - Maximum flexibility for complex logic designs
  - Programmable output polarity
  - Also emulates 20-pin PAL devices with full function/fuse map/parametric compatibility
- Preload and power-up reset of all registers
  - 100% functional testability
- Fully supported by National PLANT™ development software
- Security cell prevents copying logic
- Electronic signature for identification
- Same JEDEC map as GAL16V8

### PAL Replacement by Device Type

<table>
<thead>
<tr>
<th>&quot;Small PAL&quot; Mode</th>
<th>&quot;Registered PAL&quot; Mode</th>
<th>&quot;Medium PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>10L6</td>
<td>12L6</td>
<td>14L4</td>
</tr>
<tr>
<td>10H6</td>
<td>12H6</td>
<td>14H4</td>
</tr>
<tr>
<td>10P6</td>
<td>12P6</td>
<td>14P4</td>
</tr>
</tbody>
</table>

### PAL Replacement by Speed/Power

<table>
<thead>
<tr>
<th>Speed Series</th>
<th>D</th>
<th>D (MIL)</th>
<th>D2</th>
<th>B</th>
<th>D2 (MIL)</th>
<th>B (MIL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>10 ns</td>
<td>15 ns</td>
<td>15 ns</td>
<td>15 ns</td>
<td>20 ns</td>
<td>20 ns</td>
</tr>
<tr>
<td>Power</td>
<td>180 mA</td>
<td>180 mA</td>
<td>90 mA</td>
<td>180 mA</td>
<td>90 mA</td>
<td>180 mA</td>
</tr>
<tr>
<td>GAL</td>
<td>10L</td>
<td>15L</td>
<td>15L</td>
<td>15L</td>
<td>20L</td>
<td>20L</td>
</tr>
<tr>
<td>Speed Version</td>
<td>115 mA</td>
<td>140 mA</td>
<td>115 mA</td>
<td>115 mA</td>
<td>140 mA</td>
<td>140 mA</td>
</tr>
</tbody>
</table>

### Block Diagram—GAL16V8A
Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage $V_{CC}$: $-0.5V$ to $+7.0V$
Input Voltage (Note 2): $-2.5V$ to $V_{CC} + 1.0V$
Off-State Output Voltage (Note 2): $-2.5V$ to $V_{CC} + 1.0V$
Output Current: $\pm 100\ mA$
Storage Temperature: $-65\degree C$ to $+150\degree C$
Ambient Temperature with Power Applied: $-65\degree C$ to $+125\degree C$
Junction Temperature: $-65\degree C$ to $+150\degree C$
Lead Temperature (Soldering, 10 seconds): $260\degree C$
ESD Tolerance: $500V$
$C_{ZAP} = 100\ pF$
$R_{ZAP} = 1500\Omega$
Test Method: Human Body Model
Test Specification: NSC SOP-5-026 Rev. C

Recommended Operating Conditions
SUPPLY VOLTAGE AND TEMPERATURE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td>0</td>
<td>25</td>
<td>75</td>
</tr>
<tr>
<td>$T_C$</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AC TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GAL16V8A-10L*</th>
<th>GAL16V8A-12L</th>
<th>GAL16V8A-15L</th>
<th>GAL16V8A-20L*</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{SU}$</td>
<td>Set-Up Time (Input or Feedback before Clock)</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>$t_H$</td>
<td>Hold Time (Input after Clock)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock Pulse Width (High/Low)</td>
<td>8</td>
<td>8</td>
<td>10</td>
<td>12</td>
</tr>
<tr>
<td>$t_{CYCLE}$</td>
<td>Clock Cycle Period (with Feedback) (Note 3)</td>
<td>18</td>
<td>22</td>
<td>24</td>
<td>30</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 4) With Feedback</td>
<td>55.5</td>
<td>48.0</td>
<td>41.6</td>
<td>33.3</td>
</tr>
<tr>
<td></td>
<td>Without Feedback</td>
<td>62.5</td>
<td>62.5</td>
<td>50.0</td>
<td>41.6</td>
</tr>
<tr>
<td>$f_I$</td>
<td>Input Frequency (Note 5)</td>
<td>100</td>
<td>83.3</td>
<td>66.6</td>
<td>50.0</td>
</tr>
<tr>
<td>$t_{PR}$</td>
<td>Clock Valid after Power-Up</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

*Preliminary

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + t_{CLK}$

Note 4: $f_{CLK}$ (with feedback) $= \frac{t_{CYCLE}}{1}$

Note 5: $f_I = \frac{t_{PO}}{1}$

Note 6: $f = \frac{t_{PO}}{1}$
### Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Temperature Range</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td>$V_{CC} = \text{Min} \quad I_{OH} = -3.2 \text{ mA}$</td>
<td>COM/IND</td>
<td>2.4</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>$V_{CC} = \text{Min} \quad I_{OL} = 12 \text{ mA}$</td>
<td>MIL</td>
<td>0.5</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>COM/IND</td>
<td>2.4</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>COM/IND</td>
<td>0.5</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>High Level Off State Output Current</td>
<td>$V_{CC} = \text{Max}, \quad V_O = V_{CC} \text{(Max)}$</td>
<td>COM/IND</td>
<td>10</td>
<td>$\mu$A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Low Level Off State Output Current</td>
<td>$V_{CC} = \text{Max}, \quad V_O = V_{CC} \text{(Max)}$</td>
<td>COM/IND</td>
<td>10</td>
<td>$\mu$A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_I$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max}, \quad V_I = V_{CC} \text{(Max)}$</td>
<td>COM/IND</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{CC} = \text{Max}, \quad V_I = V_{CC} \text{(Max)}$</td>
<td>MIL</td>
<td>0.5</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{CC} = \text{Max}, \quad V_I = \text{GND}$</td>
<td>MIL</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$*</td>
<td>Output Short Circuit Current</td>
<td>$V_{CC} = 5.0V, \quad V_O = \text{GND}$</td>
<td>COM/IND</td>
<td>$-30$</td>
<td>$-150$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$f = 25 \text{ MHz}, \quad V_{CC} = \text{Max}$</td>
<td>COM/IND</td>
<td>$115$</td>
<td>mA</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>Input Capacitance</td>
<td>$V_{CC} = 5.0V, \quad V_I = 2.0V$</td>
<td>COM/IND</td>
<td>8</td>
<td>pF</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$C_{I/O}$</td>
<td>I/O Capacitance</td>
<td>$V_{CC} = 5.0V, \quad V_{I/O} = 2.0V$</td>
<td>COM/IND</td>
<td>10</td>
<td>pF</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

*One output at a time for a maximum duration of one second.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>COM</th>
<th>COM</th>
<th>COM IND/MIL</th>
<th>IND/MIL</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>S1 Closed, $C_L = 50 \text{ pF}$</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLK}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>S1 Closed, $C_L = 50 \text{ pF}$</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZG}$</td>
<td>$\overline{G}$ to Registered Output Enabled</td>
<td>Active High: S1 Open, $C_L = 50 \text{ pF}$</td>
<td>10</td>
<td>10</td>
<td>15</td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZG}$</td>
<td>$\overline{G}$ to Registered Output Disabled</td>
<td>Active Low: S1 Closed, $C_L = 50 \text{ pF}$</td>
<td>10</td>
<td>10</td>
<td>15</td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ZXI}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>Active High: S1 Open, $C_L = 50 \text{ pF}$</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{XZI}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>Active Low: S1 Closed, $C_L = 50 \text{ pF}$</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RESET}$</td>
<td>Power-Up to Registered Output High</td>
<td>S1 Closed, $C_L = 50 \text{ pF}$</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>$\mu$s</td>
</tr>
</tbody>
</table>

*Preliminary
AC Test Load

Test Waveforms

Setup and Hold

Pulse Width

Propagation Delay

Enable and Disable

Notes:

C<sub>s</sub> includes probe and jig capacitance.

V<sub>T</sub> = 1.5V.

Test inputs have rise and fall times of 5 ns between 0.3V and 2.7V.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Switching Waveforms

Power-Up Reset Waveforms

Input/Output Schematics

Input Translator/Buffer

Phased Output Turn-On Circuit

TL/L/9999-15

TL/L/9999-16

TL/L/9999-17

TL/L/9999-18
Ordering Information

Generic Array Logic Family
Number of Array Inputs
Output Type: V = Variable Architecture
Number of Outputs
Second Generation GAL Technology
Speed: 10: tpd = 10ns
12: tpd = 12ns
15: tpd = 15ns
20: tpd = 20ns

L = Low Power (115 mA for GAL16V8A devices)
Package Type: N = 20-Pin Plastic DIP
J = 20-Pin Ceramic DIP
V = 20-Lead Plastic Chip Carrier
Temperature Range: C = Commercial (0°C to +75°C)
I = Industrial (-40°C to +85°C)
M = Military (-55°C to +125°C)

* -10 and -20 devices are Preliminary.
** -20 devices are Military only.

GAL16V8A Block Diagram—DIP Connections

FIGURE 1
Functional Description

The GAL logic array consists of a programmable AND array with fixed OR-gate connections, similar to the bipolar PAL architecture. The logic array is organized as 16 complementary input lines crossing 64 "product term" lines with a programmable E2PROM cell at each intersection (2048 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines "connected" to it are in the high logic state.

The 64 product terms are organized into eight output groups with eight terms each. Seven or eight of the product terms in each output group feed into an OR-gate to produce each output logic function; one of the product terms may instead be used to control the associated TRI-STATE device output. The 20-Lead PLCC Connection Diagram (Figure 1) shows how the output logic functions are organized into output logic macrocells (OLMCs). The eight OLMCs control the flow of input and output signals between the logic array and the device's I/O pins.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-low or active-high (adjusted before the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

All of the possible I/O configurations of the GAL16V8A are classified into three basic modes: "Small-PAL" mode, "Registered-PAL" mode and "Medium-PAL" mode. These modes correspond to the architectures of the PAL families which the GAL16V8A can emulate. The modes determine the mixture of OLMC configurations which can be selected for the device. The OLMC Selection table (Table I) lists which functions can be selected on the device pin* 1 and pins* 11 through 19 for each of the three modes. The logic diagrams in Figure 3 illustrate these OLMC functions.

"OUTPUT" represents the always-active combinatorial output configuration available in the "Small-PAL" mode. "REGISTER" is the registered output with register feedback available in the "Registered-PAL" mode. "I/O" is the combinatorial bidirectional I/O available in "Registered-PAL" and "Medium-PAL" modes. "TRI-STATE" is the TRI-STATE combinational output function appearing on pins* 12 and 19 in the "Medium-PAL" mode. "INPUT" in Table I denotes an OLMC used as a dedicated input only.

*Applies to both 20-pin DIP and 20-lead PLCC packages for GAL16V8A.

20-Lead PLCC Connection Diagram

FIGURE 2
TABLE I

<table>
<thead>
<tr>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>CLOCK</td>
<td>INPUT</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>TRI-STATE**</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT</td>
<td>OUTPUT ENABLE (G)</td>
<td>INPUT</td>
</tr>
</tbody>
</table>

*Active combinatorial output  
**TRI-STATE combinatorial output

TABLE II

<table>
<thead>
<tr>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
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<td>OUTPUT*</td>
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<td>INPUT</td>
</tr>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>10L8</td>
<td>12L6</td>
<td>14L4</td>
</tr>
<tr>
<td>10H8</td>
<td>12H6</td>
<td>14H4</td>
</tr>
<tr>
<td>10P8</td>
<td>12P6</td>
<td>14P4</td>
</tr>
</tbody>
</table>

*Active combinatorial output  
**TRI-STATE combinatorial output.
OLMC Configurations

OUTPUT (Active Combinatorial Output)

REGISTER (Registered Output)

I/O (Combinatorial Input/Output)

TRI-STATE (TRI-STATE Combinatorial Output)

FIGURE 3
Functional Description (Continued)

In the “Small-PAL” and “Medium-PAL” modes (Table I), pins *1 and 11 are always dedicated inputs. In the “Registered-PAL” mode, however, pin * 1 becomes the clock input controlling all OLMC registers, and pin * 11 becomes the output enable (G) input controlling the TRI-STATE outputs of all registered OLMCs. Within the “Small-PAL” and “Registered-PAL” modes in Table I, the functions of pins * 12 through 19 can be selected individually from either of the two functions listed. For example, in “Registered-PAL” mode, pins * 12 through 19 can each be designated as either a registered output or a combinatorial I/O. The “Medium-PAL” mode represents a single fixed configuration used to emulate combinatorial medium PAL devices (16L8, 16H8, 16P8).

Table II lists the bipolar PAL products which the GAL16V8A can emulate, and the specific input/output configurations used. This is just a subset, however, of all the configurations provided in Table I.

All registers in a GAL device are reset to the low state upon power-up. The active-low outputs, in turn, assume high logic levels (if enabled) regardless of the selected output polarity. This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, tREF) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or VCC (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

* Applies to both 20-pin DIP and 20-lead FCC packages for GAL16V8A.

Clock/Input Frequency Specifications

The clock frequency (fCLK) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e. based only on external inputs), the minimum required cycle period (fCLK−1 without feedback) is defined as the greater of the minimum clock period (tH, high + tL, low) and the minimum “data window” period (fSU + tH). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (fCYCLE = fCLK−1 with feedback) is defined as fCLK + fSU. This provides sufficient time for outputs from the registers to feedback through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (fI) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinational output. The fI specification is derived as the inverse of the combinatorial propagation delay (tP).

Design Development Support

A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible “cell-map” (analogous to a PAL “fuse-map”). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into a variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device. The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as PLAN software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMCs are provided for direct map editing and diagnostic purposes (see “Programming Details”). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.
Security Cell
A security cell is provided on all GAL16V8A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature
Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National's PLAN development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase
The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection
GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

To insure that no undesired bias conditions occur with P+ diffusions, a Latch-Lock™ power-up circuitry has been developed. The drain of all P channel devices normally connected to the device supply are now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.

Manufacturer Testing
Because of E2CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every reprogrammable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all reprogrammable cells in the device include margin testing, internal verify, and program retention during hot- and cold-temperature testing. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload
The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all E2CMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the Register Preload Waveform in Figure 5, the preload sequence must not begin until the normal power-up reset operation has completed (after time \( t_{\text{RESET}} \)). The device is placed into preload mode by raising the "PRLD" input (pin* 11) to voltage \( V_{\text{IL}} \), as specified in the Register Preload Specifications (Table III).

To preload the OLMC registers, a series of data bits are shifted into the device on the "SDIN" input (pin* 9), one bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the "DCLK" input (pin* 1). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then "upward" through all remaining registered OLMCs in pin number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in Figure 4.

As the data series is shifted into the SDIN input, the contents of all registers (in registered OLMCs) are shifted "upward" and out onto the "SOUT" output (pin* 12). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the SOUT pin of each chip is connected to the SDIN pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into SDIN or out of SOUT, \( V_{\text{IL}} / V_{\text{OH}} = \) register reset (0), and \( V_{\text{IL}} / V_{\text{OH}} = \) register set (1). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

*Applies to both 20-pin DIP and 20-lead PCQ Packages for GAL16V8A.
Register Preload (Continued)

**The S\textsubscript{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V\textsubscript{CC} with a 10 k\Omega resistor.**

FIGURE 4. Output Register Preload Pinout

Register Preload Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{IH}</td>
<td>Input Voltage (High)</td>
<td>2.40</td>
<td>V\textsubscript{CC}</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{IL}</td>
<td>Input Voltage (Low)</td>
<td>0.00</td>
<td>0.50</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{IES}</td>
<td>Registered Preload Input Voltage</td>
<td>14.5</td>
<td>15</td>
<td>15.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{OH}</td>
<td>Output Voltage (High) (Note 1)</td>
<td>V\textsubscript{OH} \leq V\textsubscript{CC}</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{OL}</td>
<td>Output Voltage (Low) (Note 1)</td>
<td>0.00</td>
<td>0.50</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{IH}, I\textsubscript{IL}</td>
<td>Input Current (Programming)</td>
<td>±1</td>
<td>±10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{OH}</td>
<td>High Level Output Current (Note 1)</td>
<td>V\textsubscript{OH} \leq V\textsubscript{CC}</td>
<td>10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{PWV}</td>
<td>Verify Pulse Width</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{D}</td>
<td>Pulse Sequence Delay</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{RESET}</td>
<td>Register Reset Time from Valid V\textsubscript{CC}</td>
<td>45</td>
<td>μs</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The S\textsubscript{DOUT} output buffer is an open drain output. This pin should be terminated to V\textsubscript{CC} with a 10k resistor.

Register Preload Waveforms

**The S\textsubscript{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V\textsubscript{CC} with a 10 k\Omega resistor.**

FIGURE 5

FIGURE 2-173
Programming Details

Understanding the information in this section is not essential when using approved programming equipment and software for developing GAL designs. This is a more thorough disclosure of the GAL architecture provided for direct JEDEC cell-map editing and diagnostic purposes. This section alone, however, does not contain sufficient information to implement the GAL programming algorithm. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

As mentioned in the Functional Description, the OLMC is responsible for selecting input and/or output paths, registered vs. combinatorial outputs, active-high or low polarity, and common vs. locally-controlled TRI-STATE control. Additionally, the OLMCs select between alternate logic array input paths to maintain JEDEC cell-map compatibility with either "small-PAL" or "medium-PAL" logic arrays.

The various configurations of the OLMCs are controlled by a set of programmable "architecture" cells, separate from the logic-defining array cells. Each GAL device contains two "global" architecture cells, "SYN" and "AC0", which affect all OLMCs. Each of the device's eight OLMCs also contains two "local" cells, "AC1" and "XOR". The OLMC Logic Diagram in Figure 6 shows how the architecture cells select the different paths through the OLMC.

The SYN bit controls whether a device will have any registered outputs (SYN = 0) or will be purely combinatorial (SYN = 1). The SYN bit determines whether device pins* 1 and 11 are used as the clock and global TRI-STATE control inputs (SYN = 0) or whether they are ordinary inputs (SYN = 1). The AC0 bit selects between the "Small-PAL" mode and the "Medium/Registered-PAL" modes. The function of the AC1 bits depend on the state of the AC0 bit. In "Small-PAL" mode (AC0 = 0), the AC1 bit in each OLMC determines whether the associated device pin is an output (AC1 = 0) or an input (AC1 = 1). In "Registered-PAL" mode (AC0 = 1), the AC1 bit determines whether each OLMC is registered (AC1 = 0) or combinatorial (AC1 = 1). In "Medium-PAL" mode (AC0 = 1), the AC1 bits in all OLMCs must be set to 1 (combinatorial). All of the valid architecture bit configurations are shown in the OLMC Architecture table (Table IV), which has the same familiar format used in the OLMC Selection table (Table I).

Independent of SYN, AC0 and the AC1 bits, the XOR bit in each OLMC selects between active-low (XOR = 0) or active-high (XOR = 1) output polarity.

*Applies to both 20-pin DIP and 20-lead PCC packages for GAL16V8A.
## OLMC Logic Diagram

![OLMC Logic Diagram](image)

*Applies to both 20-pin DIP and 20-lead PCC packages for GAL16V8A.

## OLMC Architecture Programming

### FIGURE 6

#### TABLE IV

<table>
<thead>
<tr>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
<th>JEDEC Input Line #s (Note 1)</th>
<th>JEDEC Input Line #s (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>INPUT</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 19</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 18</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 17</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 16</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 15</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 14</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 13</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td><strong>Pin 12</strong></td>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
<tr>
<td>Pin 11</td>
<td>INPUT</td>
<td>INPUT</td>
<td>2,3</td>
</tr>
</tbody>
</table>

### Notes:
- Pin numbers above apply to both 20-pin DIP and 20-lead PCC packages for GAL16V8A.
- **Note 1:** All even and odd numbered JEDEC input line numbers correspond to true and complement array inputs, respectively.
- **AC1** is a combinatorial output.
- **AC1** is a combinatorial output.
- **AC1** is a combinatorial output.
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- **AC1** is a combinatorial output.
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- **AC1** is a combinatorial output.
- **AC1** is a combinatorial output.
GAL16V8A Logic Diagram

DIP PIN NUMBERS
PRODUCT LINE FIRST CELL NUMBERS

INPUT LINE
DIP PIN
NUMBERS

VCC

USER ELECTRONIC SIGNATURE WORD:

SYN=2192
ACO=2193

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

FIGURE 7
National Semiconductor

GAL20V8A-10, -12, -15, -20
Generic Array Logic

General Description
The NSC E2CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL20V8A features 8 programmable Output Logic Macrocells (OLMCs) allowing each TRI-STATE® output to be configured by the user. Additionally, the GAL20V8A is capable of emulating, in a functional/fuse map/parametric compatible device, the most popular 24-pin PAL® device architectures.

Programming is accomplished using readily available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features
- High performance E2CMOS technology
  - 10 ns maximum propagation delay
  - \( f_{\text{CLK}} = 62.5 \text{ MHz} \)
  - 8 ns maximum from clock input to data output
  - TTL compatible 24 mA outputs
  - UltraMOS® III advanced CMOS technology
- 36% reduction in power
  - 115 mA max \( I_{\text{CC}} \)
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (<50 ms)
  - 20 year data retention
- Eight output logic macrocells
  - Maximum flexibility for complex logic designs
  - Programmable output polarity
  - Also emulates 24-pin PAL devices with full function/fuse map/parametric compatibility
- Preload and power-up reset of all registers
  - 100% functional testability
- Fully supported by National PLAN™ development software
- Security cell prevents copying logic
- Electronic signature for identification
- Same JEDEC map as GAL20V8

PAL Replacement by Device Type

<table>
<thead>
<tr>
<th>&quot;Small PAL&quot; Mode</th>
<th>&quot;Registered PAL&quot; Mode</th>
<th>&quot;Medium PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>14L8</td>
<td>16L6</td>
<td>18L4</td>
</tr>
<tr>
<td>14L8</td>
<td>16L6</td>
<td>18L4</td>
</tr>
<tr>
<td>14L8</td>
<td>16H6</td>
<td>18H4</td>
</tr>
<tr>
<td>14L8</td>
<td>16P6</td>
<td>18P4</td>
</tr>
</tbody>
</table>

PAL Replacement by Speed/Power

<table>
<thead>
<tr>
<th>Speed Series</th>
<th>Speed</th>
<th>Power</th>
<th>Speed Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>10 ns</td>
<td>180 mA</td>
<td>10L (115 mA)</td>
</tr>
<tr>
<td>D (MIL)</td>
<td>15 ns</td>
<td>160 mA</td>
<td>15L (140 mA)</td>
</tr>
<tr>
<td>D2</td>
<td>15 ns</td>
<td>105 mA</td>
<td>15L (115 mA)</td>
</tr>
<tr>
<td>B</td>
<td>15 ns</td>
<td>180 mA</td>
<td>15L (115 mA)</td>
</tr>
<tr>
<td>D2 (MIL)</td>
<td>20 ns</td>
<td>105 mA</td>
<td>20L (140 mA)</td>
</tr>
<tr>
<td>B (MIL)</td>
<td>20 ns</td>
<td>180 mA</td>
<td>20L (140 mA)</td>
</tr>
</tbody>
</table>

Block Diagram—GAL20V8A
**Absolute Maximum Ratings (Note 1)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{CC}$) & $-0.5V$ to $+7.0V$

Input Voltage (Note 2) & $-2.5V$ to $V_{CC} + 1.0V$

Off-State Output Voltage (Note 2) & $-2.5V$ to $V_{CC} + 1.0V$

Output Current & $\pm 100$ mA

Storage Temperature & $-65^\circ$C to $+150^\circ$C

Ambient Temperature with Power Applied & $-65^\circ$C to $+125^\circ$C

Junction Temperature & $-65^\circ$C to $+150^\circ$C

Lead Temperature (Soldering, 10 seconds) & $260^\circ$C

ESD Tolerance & 500V

$C_{ZAP} = 100$ pF

$R_{ZAP} = 1500\Omega$

Test Method: Human Body Model

Test Specification: NSC SOP-5-028 Rev. C

---

**Recommended Operating Conditions**

**SUPPLY VOLTAGE AND TEMPERATURE**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>4.75 5 5.25</td>
<td>4.5 5 5.5</td>
<td>4.5 5 5.5</td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Free-Air Temperature</td>
<td>0 25 75</td>
<td>$-40 25 85$</td>
<td>$-55 25$</td>
<td>°C</td>
</tr>
<tr>
<td>$T_C$</td>
<td>Operating Case Temperature</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

---

**AC TIMING REQUIREMENTS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GAL20V8A-10L*&lt;sup&gt;4&lt;/sup&gt;</th>
<th>GAL20V8A-12L</th>
<th>GAL20V8A-15L</th>
<th>GAL20V8A-20L*&lt;sup&gt;4&lt;/sup&gt;</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{SU}$</td>
<td>Set-Up Time (Input or Feedback before Clock)</td>
<td>10 12</td>
<td>12</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_H$</td>
<td>Hold Time (Input after Clock)</td>
<td>0 0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock Pulse Width (High/Low)</td>
<td>8 8</td>
<td>10</td>
<td>12</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{CYCLE}$</td>
<td>Clock Cycle Period (with Feedback) (Note 3)</td>
<td>18 22</td>
<td>24</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Clock Frequency (Note 4)</td>
<td>With Feedback</td>
<td>55.5</td>
<td>48.0</td>
<td>41.6</td>
<td>33.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Without Feedback</td>
<td>62.5</td>
<td>62.5</td>
<td>50.0</td>
<td>41.6</td>
</tr>
<tr>
<td>$f_I$</td>
<td>Input Frequency (Note 5)</td>
<td>100.0</td>
<td>83.3</td>
<td>66.6</td>
<td>50.0</td>
<td></td>
</tr>
<tr>
<td>$t_{SR}$</td>
<td>Clock Valid after Power-Up</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

*Preliminary

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + f_{CLK}$

Note 4: $f_{CLK}$ (with feedback) = $(t_{CYCLE})^{-1}$

$C_{ZAP} = 100$ pF

$R_{ZAP} = 1500\Omega$

Test Method: Human Body Model

Test Specification: NSC SOP-5-028 Rev. C

---

*Note: 2·178
**Electrical Characteristics** Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Temperature Range</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td></td>
<td></td>
<td>2.0</td>
<td>VCC</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td></td>
<td></td>
<td>-0.5</td>
<td>0.8</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min</td>
<td></td>
<td></td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min</td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IOZH</td>
<td>High Level Off State</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Off State</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Ii</td>
<td>Maximum Input Current</td>
<td>VCC = Max, VI = VCC (Max)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>IIH</td>
<td>High Level Input Current</td>
<td>VCC = Max, VI = VCC (Max)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>III</td>
<td>Low Level Input Current</td>
<td>VCC = Max, VI = GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>IOS*</td>
<td>Output Short Circuit Current</td>
<td>VCC = 5.0V, VO = GND</td>
<td></td>
<td></td>
<td></td>
<td>-30</td>
<td>-150</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>f = 25 MHz, VCC = Max</td>
<td></td>
<td></td>
<td></td>
<td>115</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Input Capacitance</td>
<td>VCC = 5.0V, VI = 2.0V</td>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>CI/O</td>
<td>I/O Capacitance</td>
<td>VCC = 5.0V, VI/VO = 2.0V</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

*One output at a time for a maximum duration of one second.

**Switching Characteristics** Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>GAL20V8A-10L*</th>
<th>GAL20V8A-12L</th>
<th>GAL20V8A-15L</th>
<th>GAL20V8A-20L*</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Input or Feedback to</td>
<td>S1 Closed, CL = 50 pF</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>tCLK</td>
<td>Clock to Registered Output</td>
<td>S1 Closed, CL = 50 pF</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tPZG</td>
<td>Active High; S1 Open, CL = 50</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>15</td>
<td>18</td>
</tr>
<tr>
<td>tPZI</td>
<td>Input to Combinatorial Output</td>
<td>From VOH; S1 Open, CL = 5 pF</td>
<td>10</td>
<td>10</td>
<td>15</td>
<td>18</td>
</tr>
<tr>
<td>tRXI</td>
<td>Input to Combinatorial Output</td>
<td>From VOH; S1 Open, CL = 5 pF</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>fRESET</td>
<td>Power-Up to Registered</td>
<td>S1 Closed, CL = 50 pF</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
</tr>
</tbody>
</table>

*Preliminary
AC Test Load

![AC Test Load Diagram]

Test Waveforms

Setup and Hold

![Setup and Hold Diagram]

Pulse Width

![Pulse Width Diagram]

Propagation Delay

![Propagation Delay Diagram]

Enable and Disable

![Enable and Disable Diagram]

Notes:

- $C_0$ includes probe and jig capacitance.
- $V_T = 1.5V$.
- Test inputs have rise and fall times of 5 ns between 0.3V and 2.7V.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Switching Waveforms

Power-Up Reset Waveforms

Input/Output Schematics

Input Translator/Buffer

TL/L/10000-15

TL/L/10000-16

TL/L/10000-17
Input/Output Schematics (Continued)

Phased Output Turn-On Circuit

Ordering Information

Generic Array Logic Family
Number of Array Inputs
Output Type: V = Variable Architecture
Number of Outputs
Second Generation GAL Technology
Speed: 10: \( t_{PD} = 10 \text{ns} \)
12: \( t_{PD} = 12 \text{ns} \)
15: \( t_{PD} = 15 \text{ns} \)
20: \( t_{PD} = 20 \text{ns} \)

L = Low Power (115 mA for GAL20V8A devices)
Package Type: N = 24-Pin Plastic DIP
J = 24-Pin Ceramic DIP
V = 28-Lead Plastic Chip Carrier

Temperature Range: C = Commercial (0°C to +75°C)
I = Industrial (-40°C to +85°C)
M = Military (-55°C to +125°C)

GAL20V8A - 15 LNC

*10 and -20 devices are Preliminary.
**20 devices are Military only.
Functional Description

The GAL logic array consists of a programmable AND array with fixed OR-gate connections, similar to the bipolar PAL architecture. The logic array is organized as 20 complementary input lines crossing 64 “product term” lines with a programmable E2PROM cell at each intersection (2560 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines “connected” to it are in the high logic state.

The 64 product terms are organized into eight output groups with eight terms each. Seven or eight of the product terms in each output group feed into an OR-gate to produce each output logic function; one of the product terms may instead be used to control the associated TRI-STATE device output. The fundamental transfer function of each GAL output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL programming patterns.

As shown in the GAL20V8A Block Diagram (Figure 1), a total of eight output logic functions are available. Each of the AND/OR logic functions feeds into an “output logic macrocell” (OLMC). The eight OLMCs control the flow of input and output signals between the logic array and the device’s I/O pins.

Under control of an OLMC, each output may be designated either registered or combinational (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function’s output polarity may be designated active-low or active-high (adjusted before the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

All of the possible I/O configurations of the GAL20V8A are classified into three basic modes: “Small-PAL” mode, “Registered-PAL” mode and “Medium-PAL” mode. These modes correspond to the architectures of the PAL families which the GAL20V8A can emulate. The modes determine the mixture of OLMC configurations which can be selected for the device. The OLMC Selection table (Table I) lists which functions can be selected on device pins* 1, 13 and 15 through 22 for each of the three modes. The logic diagrams in Figure 3 illustrate these OLMC functions.

“OUTPUT” represents the always-active combinatorial output configuration available in the “Small-PAL” mode. “REGISTER” is the registered output with register feedback available in the “Registered-PAL” mode. “I/O” is the combinatorial bidirectional I/O available in “Registered-PAL” and “Medium-PAL” modes. “TRI-STATE” is the TRI-STATE combinatorial output function appearing on pins* 15 and 22 in the “Medium-PAL” mode. “INPUT” in Table I denotes an OLMC used as a dedicated input only.

In the “Small-PAL” and “Medium-PAL” modes (Table I), pins* 1 and 13 are always dedicated inputs. In the “Registered-PAL” mode, however, pin* 1 becomes the clock input controlling all OLMC registers, and pin* 13 becomes the output enable (G) input controlling the TRI-STATE outputs of all registered OLMCs. Within the “Small-PAL” and “Registered-PAL” modes in Table I, the functions of pins* 15 through 22 can be selected individually from either of the two functions listed. For example, in “Registered-PAL” mode, pins* 15 through 22 can each be designated as either a registered output or a combinational I/O. The “Medium-PAL” mode represents a single fixed configuration used to emulate combinational medium PAL devices (20L8, 20H8, 20P8).

Table II lists the bipolar PAL products which the GAL20V8A can emulate, and the specific input/output configurations used. This is just a subset, however, of all the configurations provided in Table I.

All registers in a GAL device are reset to the low state upon power-up. The active-low outputs, in turn, assume high logic levels (if enabled) regardless of the selected output polarity. This may simplify sequential circuit design and test. To ensure successful power-up reset, VCC must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, tpP) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or VCC (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

* Applies to 24-pin DIP packages for GAL20V8A; refer to the 28-lead PCC Connection Diagram for conversion.
FIGURE 1
Clock/Input Frequency Specifications

The clock frequency (fCLK) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (fCLK<sup>-1</sup> without feedback) is defined as the greater of the minimum clock period (t<sub>W</sub> high + t<sub>W</sub> low) and the minimum “data window” period (t<sub>SU</sub> + t<sub>H</sub>). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f<sub>CYCLE</sub>) is defined as f<sub>CLK</sub> -<sub>1</sub> with feedback) is defined as f<sub>CLK</sub> + t<sub>SU</sub>. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (f<sub>I</sub>) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The f<sub>I</sub> specification is derived as the inverse of the combinatorial propagation delay (t<sub>PD</sub>).

Design Development Support

A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible “cell-map” (analogous to a PAL “fuse-map”). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into a variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as PLAN software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMC are provided for direct map editing and diagnostic purposes (see “Programming Details”). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.
### OLMC Selection Table

#### TABLE I

<table>
<thead>
<tr>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>CLOCK</td>
<td>INPUT</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>TRISTATE**</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>INPUT or OUTPUT*</td>
<td>REGISTER or I/O</td>
<td>TRISTATE**</td>
</tr>
<tr>
<td>INPUT</td>
<td>OUTPUT ENABLE (G)</td>
<td>INPUT</td>
</tr>
</tbody>
</table>

* Active combinatorial output
**TRI-STATE combinatorial output

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-lead PCC Connection Diagram for conversion.

### PAL Replacement Configurations

#### TABLE II

<table>
<thead>
<tr>
<th>&quot;Small-PAL&quot; Mode</th>
<th>&quot;Registered-PAL&quot; Mode</th>
<th>&quot;Medium-PAL&quot; Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
</tr>
<tr>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
<td>OUTPUT*</td>
</tr>
<tr>
<td>INPUT</td>
<td>INPUT</td>
<td>INPUT</td>
</tr>
<tr>
<td>14L8</td>
<td>16L6</td>
<td>18L4</td>
</tr>
<tr>
<td>14H8</td>
<td>16H6</td>
<td>18H4</td>
</tr>
<tr>
<td>14P8</td>
<td>16P6</td>
<td>18P4</td>
</tr>
<tr>
<td>20L2</td>
<td>20R8</td>
<td>20RP8</td>
</tr>
<tr>
<td>20H2</td>
<td>20RP6</td>
<td>20RP4</td>
</tr>
<tr>
<td>20P2</td>
<td>20P4</td>
<td>20P4</td>
</tr>
</tbody>
</table>

* Active combinatorial output.
**TRI-STATE combinatorial output.

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-pin PCC Connection Diagram for conversion.
OLMC Configurations

OUTPUT (Active Combinatorial Output)

REGISTER (Registered Output)

I/O (Combinatorial Input/Output)

TRI-STATE (TRI-STATE Combinatorial Output)

FIGURE 3
Security Cell
A security cell is provided on all GAL20V8A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature
Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National’s PLAN development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase
The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection
GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching. To ensure that no undesired bias conditions occur with P+ diffusions, a Latch-Lock™ power-up circuitry has been developed. The drain of all P channel devices normally connected to the device supply are now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.

Manufacturer Testing
Because of E²CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload
The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all E²CMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the Register Preload Waveform in Figure 5, the preload sequence must not begin until the normal power-up reset operation has completed (after time tRESET). The device is placed into preload mode by raising the "PRLO" input (pin* 13) to voltage VRESET, as specified in the Register Preload Specifications (Table III).

To preload the OLMC registers, a series of data bits are shifted into the device on the "SDIN" input (pin* 11). One bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the "DCLK" input (pin* 1). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then "upward" through all remaining registered OLMCs in pin-number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in Figure 4.

*Applies to 24-pin DIP packages for GAL20V8A; refer to the 28-lead POC Connection Diagram for conversion.
Register Preload (Continued)

As the data series is shifted into the SDIN input, the contents of all registers (in registered OLMCs) are shifted "upward" and out onto the "SOOUT" output (pin 15). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the SOOUT pin of each chip is connected to the SDIN pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into SDIN or out of SDOUT, VIL/VOL = register reset (0), and VIH/VOH = register set (1). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

*Applies to 24-pin DIP packages for GAL20VBA; refer to the 28-lead PCC Connection Diagram for conversion.

Register Preload Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Voltage (Low)</td>
<td>0.00</td>
<td>0.50</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input Voltage (High)</td>
<td>2.40</td>
<td>VCC</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VS</td>
<td>Register Preload Input Voltage</td>
<td>14.5</td>
<td>15</td>
<td>15.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output Voltage (High) (Note 1)</td>
<td>VCC</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOLS</td>
<td>Output Voltage (Low) (Note 1)</td>
<td>0.00</td>
<td>0.50</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Output Current (Note 1)</td>
<td>±1</td>
<td>±10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOL</td>
<td>Low Level Output Current (Note 1)</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPWV</td>
<td>Verify Pulse Width</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>tD</td>
<td>Pulse Sequence Delay</td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>tRESET</td>
<td>Register Reset Time from Valid VCC</td>
<td>45</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The SOOUT output buffer is an open drain output. This pin should be terminated to VCC with a 10 kΩ resistor.

Register Preload Waveforms

---

**The SOOUT output buffer is an open drain output during preload. This pin should be terminated to VCC with a 10 kΩ resistor.**
OLMC Logic Diagram

OLMC Architecture Programming

TABLE IV

<table>
<thead>
<tr>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
<th>Function</th>
<th>JEDEC Input Line #s (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>INPUT INPUT</td>
<td>CLOCK</td>
<td>INPUT INPUT</td>
<td>INPUT</td>
<td>2, 3</td>
</tr>
<tr>
<td>Pin 23</td>
<td>INPUT INPUT</td>
<td>C LOCK</td>
<td>INPUT INPUT</td>
<td>INPUT</td>
<td>2, 3</td>
</tr>
<tr>
<td>Pin 22</td>
<td>OUTPUT* INPUT</td>
<td>10, 11</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>10, 11</td>
</tr>
<tr>
<td>Pin 21</td>
<td>OUTPUT* INPUT</td>
<td>14, 15</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>14, 15</td>
</tr>
<tr>
<td>Pin 20</td>
<td>OUTPUT* INPUT</td>
<td>18, 19</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>18, 19</td>
</tr>
<tr>
<td>Pin 19</td>
<td>OUTPUT* NC</td>
<td>NC</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>22, 23</td>
</tr>
<tr>
<td>Pin 18</td>
<td>OUTPUT* NC</td>
<td>NC</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>26, 27</td>
</tr>
<tr>
<td>Pin 17</td>
<td>OUTPUT* INPUT</td>
<td>22, 23</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>30, 31</td>
</tr>
<tr>
<td>Pin 16</td>
<td>OUTPUT* INPUT</td>
<td>26, 27</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>TRI-STATE**</td>
</tr>
<tr>
<td>Pin 15</td>
<td>OUTPUT* INPUT</td>
<td>30, 31</td>
<td>REGISTER I/O</td>
<td>1/0</td>
<td>TRI-STATE**</td>
</tr>
<tr>
<td>Pin 14</td>
<td>INPUT INPUT</td>
<td>34, 35</td>
<td>INPUT INPUT</td>
<td>1/0</td>
<td>34, 35</td>
</tr>
<tr>
<td>Pin 13</td>
<td>INPUT INPUT</td>
<td>38, 39</td>
<td>0 0</td>
<td>1/0</td>
<td>38, 39</td>
</tr>
</tbody>
</table>

AC1n = 0 AC1n = 1 AC1n = 0 AC1n = 1 AC1n = 1
SYN = 1, AC0 = 0 SYN = 0, AC0 = 1 SYN = 1, AC0 = 1

All outputs are combinatorial and always active.
At least one output is registered.
All I/O pins are combinatorial.

Note: Pin numbers above apply to 24-pin DIP packages; refer to the 28-lead PCC Connection Diagram for conversion.

Note 1: All even and odd numbered JEDEC input line numbers correspond to true and complement array inputs, respectively.

*Active combinatorial output.
**TRI-STATE combinatorial output.
***AC1n applies to these I/O pins only.
GAL20V8A Logic Diagram

DIP PIN NUMBERS
PRODUCT LINE FIRST CELL NUMBERS
INPUT LINE NUMBERS

DIP PIN: 

VCC

24

OLMC XOR=2560
AC1=2632
PTD=2640
-2647

OLMC XOR=2561
AC1=2633
PTD=2648
-2655

OLMC XOR=2562
AC1=2634
PTD=2656
-2663

OLMC XOR=2563
AC1=2635
PTD=2664
-2671

OLMC XOR=2564
AC1=2636
PTD=2668
-2679

OLMC XOR=2565
AC1=2637
PTD=2669
-2679

OLMC XOR=2566
AC1=2638
PTD=2680
-2687

OLMC XOR=2567
AC1=2639
PTD=2666
-2687

2703

USER ELECTRONIC SIGNATURE WORD:
2568 2576 2584 2592 2600 2608 2616 2624 2631

BYTE 0 BYTE 1 BYTE 2 BYTE 3 BYTE 4 BYTE 5 BYTE 6 BYTE 7

MSB LSB MSB LSB

SYN=2704
ACO=2705

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

FIGURE 7
Programming Details

Understanding the information in this section is not essential when using approved programming equipment and software for developing GAL designs. This is a more thorough disclosure of the GAL architecture provided for direct JEDEC cell-map editing and diagnostic purposes. This section alone, however, does not contain sufficient information to implement the GAL programming algorithm. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

As mentioned in the Functional Description, the OLMC is responsible for selecting input and/or output paths, registered vs. combinatorial outputs, active-high or low polarity, and common vs. locally-controlled TRI-STATE control. Additionally, the OLMCs select between alternate logic array input paths to maintain JEDEC cell-map compatibility with either “small-PAL” or “medium-PAL” logic arrays.

The various configurations of the OLMCs are controlled by a set of programmable “architecture” cells, separate from the logic-defining array cells. Each GAL device contains two “global” architecture cells, “SYN” and “AC0”, which affect all OLMCs. Each of the device’s eight OLMCs also contains two “local” cells, “AC1” and “XOR”. The OLMC Logic Diagram in Figure 6 shows how the architecture cells select the different paths through the OLMC.

The SYN bit controls whether a device will have any registered outputs (SYN = 0) or will be purely combinatorial (SYN = 1). The SYN bit determines whether device pins* 1 and 13 are used as the clock and global TRI-STATE control inputs (SYN = 0) or whether they are ordinary inputs (SYN = 1). The AC0 bit selects between the “Small-PAL” mode and the “Medium/Registered-PAL” modes. The function of the AC1 bits depend on the state of the AC0 bit. In “Small-PAL” mode (AC0 = 0), the AC1 bit in each OLMC determines whether the associated device pin is an output (AC1 = 0) or an input (AC1 = 1). In “Registered-PAL” mode (AC0 = 1), the AC1 bit determines whether each OLMC is registered (AC1 = 0) or combinatorial (AC1 = 1). In “Medium-PAL” mode (AC0 = 1), the AC1 bits in all OLMCs must be set to 1 (combinatorial). All of the valid architecture bit configurations are shown in the OLMC Architecture table (Table IV), which has the same familiar format used in the OLMC Selection table (Table I).

Independent of SYN, AC0 and the AC1 bits, the XOR bit in each OLMC selects between active-low (XOR = 0) or active-high (XOR = 1) output polarity.

*Applies to 24-pin DIP packages for GAL20V8A; refer to the 28-lead PCC Connection Diagram for conversion.
GAL22V10, -15, -20, -25, -30
Generic Array Logic

General Description
The NSC E2CMOSTM GAL® devices combine a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL22V10 features 22 inputs, and 10 programmable Output Logic Macro Cells (OLMCs) allowing each TRI-STATE® output to be configured by the user. The architecture of each output is user-programmable for registered or combinatorial operation, active high or low polarity, and as an input, output or bidirectional I/O. This architecture features variable product term distribution, from 8 to 16 logical product terms to each output, as shown in the logic diagram. CMOS circuitry allows the GAL22V10 to consume just 90 mA typical Icc which represents a 50% saving in power when compared to its bipolar counterparts. Synchronous preset and asynchronous reset product terms have been added which are common to all output registers to enhance system operation. The GAL22V10 is directly compatible with the bipolar PAL22V10 in terms of functionality, fuse map, pinout, and electrical characteristics.

Programming is accomplished using industry standard available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles. Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability of all GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features:
- High performance E2CMOS technology
  - 15 ns maximum propagation delay
  - fmax = 50 MHz with feedback
  - 8 ns maximum from clock input to data output
  - TTL compatible 16 mA outputs
  - UltraMOS® III advanced CMOS technology
  - Internal pull-up resistor on all pins
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (<50 ms)
  - 20 year data retention
- Ten output logic macrocells
  - Maximum Flexibility
  - Programmable output polarity
  - Maximum flexibility for complex logic designs
  - Full function/fuse map/parametric compatibility with PAL22V10 devices
- Variable product term distribution
  - From 8 to 16 product terms per output data function
- Synchronous preset and asynchronous reset to all registers
- Preload and power-up reset of all registers
  - 100% functional testability
- Fully supported by National PLANTM and other industry standard development software
- Security cell prevents copying logic

Ordering Information

<table>
<thead>
<tr>
<th></th>
<th>Generic Array Logic Family</th>
<th>Number of Array Inputs</th>
<th>Output Type:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V = Variable Architecture</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Number of Outputs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>15: tpd = 15 ns (Comm)</td>
<td>20: tpd = 20 ns (Ind/Mil)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25: tpd = 25 ns (Comm)</td>
<td>30: tpd = 30 ns (Ind/Mil)</td>
<td></td>
</tr>
<tr>
<td>L = Low Power</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Type:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N = 24-Pin Plastic DIP</td>
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<td></td>
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</tr>
<tr>
<td>J = 24-Pin Ceramic DIP</td>
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<td></td>
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</tr>
<tr>
<td>V = 26-Lead Plastic Chip Carrier</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C = Commercial (-40°C to +85°C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I = Industrial (-40°C to +85°C)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>M = Military (-55°C to +125°C)</td>
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Block Diagram—GAL22V10
### Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC) (Note 2)</td>
<td>-0.5V to +7.0V</td>
</tr>
<tr>
<td>Input Voltage (Note 2)</td>
<td>-2.5V to VCC + 1.0V</td>
</tr>
<tr>
<td>Off-State Output Voltage (Note 2)</td>
<td>-2.5V to VCC + 1.0V</td>
</tr>
<tr>
<td>Output Current</td>
<td>±100 mA</td>
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<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature with Power Applied</td>
<td>-65°C to +125°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>-65°C to +150°C</td>
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<td>Lead Temperature (Soldering, 10 seconds)</td>
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<tr>
<td>ESD Tolerance</td>
<td>TBD</td>
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<td>Test Method: Human Body Model</td>
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<td>Test Specification: NSC SOP-5-028</td>
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### Recommended Operating Conditions
#### SUPPLY VOLTAGE AND TEMPERATURE

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<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
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<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
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<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>4.5</td>
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<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>0</td>
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<td>75</td>
<td>-40</td>
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<td>TC</td>
<td>Operating Case Temperature</td>
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### AC TIMING REQUIREMENTS

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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GAL22V10-15L</th>
<th>GAL22V10-20L</th>
<th>GAL22V10-25L</th>
<th>GAL22V10-30L</th>
<th>Units</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>COM</td>
<td>IND/MIL</td>
<td>COM</td>
<td>IND/MIL</td>
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<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>tsu</td>
<td>Set-Up Time (Input or Feedback before Clock)</td>
<td>12</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>15</td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time (Input after Clock)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width (High/Low)</td>
<td>10</td>
<td>12</td>
<td>15</td>
<td>20</td>
<td>12</td>
</tr>
<tr>
<td>tAW</td>
<td>Asynchronous Reset Input Pulse Width</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td>tAR</td>
<td>Asynchronous Reset Recovery Time</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td>tCYCLE</td>
<td>Clock Cycle Period (with Feedback) (Note 3)</td>
<td>22</td>
<td>30</td>
<td>25</td>
<td>30</td>
<td>25</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4) With Feedback</td>
<td>45.4</td>
<td>33.3</td>
<td>28.5</td>
<td>22.2</td>
<td>33.3</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4) Without Feedback</td>
<td>50.0</td>
<td>41.6</td>
<td>33.3</td>
<td>33.3</td>
<td>41.6</td>
</tr>
<tr>
<td>fI</td>
<td>Input Frequency (Note 5)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>fVR</td>
<td>Clock Valid after Power-Up</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

**Notes:**
- Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.
- Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.
- Note 3: tCYCLE = tsu + tCLK
- Note 4: fCLK (with feedback) = (tCYCLE)⁻¹
- fCLK (without feedback) = (2 tW)⁻¹
- Note 5: fI = (tPO)⁻¹
### Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Symbols</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_OH = -2.2 \text{mA}$</td>
<td>COM/IND</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>$V_{SS} = 0.5$</td>
<td>$I_OH = -2.0 \text{mA}$</td>
<td>MIL</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_OH = -16 \text{mA}$</td>
<td>COM/IND</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = \text{Min}$</td>
<td>$I_OH = -12 \text{mA}$</td>
<td>MIL</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>High Level Off State Output Current</td>
<td>$V_{CC} = \text{Max}, V_O = V_{CC} (\text{Max})$</td>
<td>10</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Low Level Off State Output Current</td>
<td>$V_{CC} = \text{Max}, V_O = \text{GND}$</td>
<td>$V_{CC} = \text{Max}, V_I = \text{GND}$</td>
<td>10</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_I$</td>
<td>Maximum Input Current</td>
<td>$V_{CC} = \text{Max}, V_I = V_{CC} (\text{Max})$</td>
<td>$I_I = -150$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{CC} = \text{Max}, V_I = V_{CC} (\text{Max})$</td>
<td>10</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{CC} = \text{Max}, V_I = \text{GND}$</td>
<td>$I_{IL} = -150$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>Output Short Circuit Current</td>
<td>$V_{CC} = 5.0V, V_O = \text{GND}$</td>
<td>$I_{OH} = -50$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Output Supply Current</td>
<td>$f = 15 \text{MHz}, V_{CC} = \text{Max}$</td>
<td>$I_{OL} = -35$</td>
<td>$\mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>Input Capacitance</td>
<td>$V_{CC} = 5.0V, V_I = 2.0V$</td>
<td>8</td>
<td>$\text{pF}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{I/O}$</td>
<td>I/O Capacitance</td>
<td>$V_{CC} = 5.0V, V_{I/O} = 2.0V$</td>
<td>10</td>
<td>$\text{pF}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*One output at a time for a maximum duration of one second.

### Switching Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>GAL22V10-15L</th>
<th>GAL22V10-20L</th>
<th>GAL22V10-25L</th>
<th>GAL22V10-30L</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{PD}$</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>$S1 \text{ Closed, } C_L = 50 \text{ pF}$</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>$I_{CLK}$</td>
<td>Clock to Registered Output or Feedback</td>
<td>$S1 \text{ Closed, } C_L = 50 \text{ pF}$</td>
<td>8</td>
<td>10</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>$I_{PZI}$</td>
<td>Input to Combinatorial Output Enabled via Product Term</td>
<td>$\text{Active High;} S1 \text{ Open, } C_L = 50 \text{ pF}$</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>$I_{PZI}$</td>
<td>Input to Combinatorial Output Disabled via Product Term</td>
<td>$\text{Active Low;} S1 \text{ Closed, } C_L = 50 \text{ pF}$</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>$I_{AP}$</td>
<td>Asynchronous Reset to Register Output</td>
<td>From $V_{OH}; S1 \text{ Open, } C_L = 5 \text{ pF}$</td>
<td>20</td>
<td>25</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>$I_{RESET}$</td>
<td>Power-Up to Registered Output High</td>
<td>$S1 \text{ Closed, } C_L = 50 \text{ pF}$</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
</tr>
</tbody>
</table>
AC Test Load

Test Waveforms

Setup and Hold

Setup and Hold

Pulse Width

Propagation Delay

Enable and Disable

Notes:

- $C_L$ includes probe and jig capacitance.
- $V_T = 1.5V$.
- Test inputs have rise and fall times of 5 ns between 0.3V and 2.7V.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Switching Waveforms

Power-Up Reset Waveforms

Input/Output Schematics
Functional Description

The GAL22V10 logic array consists of a programmable AND array with fixed OR-gate connections, similar to the traditional bipolar PAL architecture. The logic array is organized as 22 complementary input lines crossing 132 "product term" lines with a programmable E2PROM cell at each intersection (S808 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines "connected" to it are in the high logic state.

Of the 132 product terms, 130 are distributed among ten "output logic macrocells" (OLMCs) with a varying number of terms allocated to each OLMC (as shown in Figure 1). The ten OLMCs control the flow of input and output signals between the logic array and the device's I/O pins. For a given OLMC, 8, 10, 12, 14 or 16 product terms feed into an OR-gate to produce each output value. This varied distribution of product terms among outputs allows more optimum use of device resources. One additional product term in each of the ten OLMCs is used to control the associated TRI-STATE device output. One global product term is used to control an asynchronous preset, and another global product term is used for a synchronous reset, and both are connected to all ten of the output registers.

The fundamental transfer function of each GAL22V10 output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL22V10 programming patterns.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-low or active-high (adjusted after the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

The four possible I/O configurations of each GAL22V10 OLMC are: registered-active low, registered-active high, combinatorial-active low, and combinatorial-active high. These combinations are shown in Figure 3. The feedback paths are redirected with the register selection. The registered configurations include an internal feedback path taken directly from the register output. The combinatorial configurations include feedback from the I/O pin, thus allowing for bidirectional I/O or additional input channels.

All registers in a GAL22V10 device are reset to the low state upon power-up. Outputs, in turn, assume either low or high logic levels (if enabled) depending on the selected output polarity. Power-up reset may simplify sequential circuit design and test. To ensure successful power-up reset, \( V_{CC} \) must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, \( t_{PR} \)) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or \( V_{CC} \) (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The \( Q \) outputs of the register will go to the logic high state following a low-to-high transition of the clock input when the synchronous preset (SP) product term is asserted. The register will be forced to the logic low state independent of the clock when the asynchronous reset (AR) product term is asserted. Product term control allows preset and reset to be functions of any combination of device inputs and output feedback. The outputs will be high or low depending upon the polarity option chosen.

Note that preset and reset control the flip-flop, not the output. Thus, if active low polarity is selected, a synchronous preset would produce low-level outputs, and an asynchronous reset would produce high-level outputs (if enabled).
Clock/Input Frequency Specifications

The clock frequency ($f_{CLK}$) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL22V10 registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e. based only on external inputs), the minimum required cycle period ($t_{cycle}$ without feedback) is defined as the greater of the minimum clock period ($t_{H}$ high + $t_{L}$ low) and the minimum "data window" period ($t_{SLH}$ + $t_{H}$). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period ($t_{cycle}$ = $f_{CLK}^{-1}$ with feedback) is defined as $t_{CLK} + t_{SLH}$. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency ($f_I$) parameter specifies the maximum rate at which each GAL22V10 input can be toggled and still produce valid logic transitions on each combinational output. The $f_I$ specification is derived as the inverse of the combinational propagation delay ($t_{PD}$).

Design Development Support

A variety of software tools and programming equipment are available to support the development of designs using GAL22V10 products. Typical software packages, including National’s PLAN software, accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible “cell-map” (analogous to a PAL “fuse-map”). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into industry standard programming equipment. Many software packages and programming units support a multitude of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

The GAL22V10 can accept fuse-maps prepared for other PAL22V10 devices. PAL22V10 fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL22V10 device into the programming unit (provided the PAL device has not been secured).

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL22V10 logic array and OLMC are provided for direct map editing and diagnostic purposes. Figure 6 and Table II show details of the OLMC and the programmable architecture cell combinations. Figure 7 shows the JEDEC logic diagram and details of all programmable cell locations. For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL22V10 programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.
OLMC Selection Table

FIGURE 3-1. Registered/Active Low

FIGURE 3-2. Registered/Active High

FIGURE 3-3. Combinatorial/Active Low

FIGURE 3-4. Combinatorial/Active High
Security Cell
A security cell is provided on all GAL22V10 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature
Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National's PLAN development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase
The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection
GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Manufacturer Testing
Because of E2CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload
The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers into an arbitrary "present state" value, and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all E2CMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the register preload waveform in Figure 5, the preload sequence must not begin until the normal power-up reset operation has completed (after time tRESET). The device is placed into preload mode by raising the "PRLD" input (pin 13*) to voltage VRES, as specified in the register preload specifications (Table I).

To preload the OLMC registers, a series of data bits are shifted into the device on the "SDIN" input (pin 11*), one bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the "DCLK" input (pin 1*). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then "upward" through all remaining registered OLMCs in pin-number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in Figure 4.

*Applies to 24-pin DIP packages for GAL22V10; refer to the 28-lead PCC Connection Diagram for conversion.
Register Preload (Continued)
As the data series is shifted into the SDIN input, the contents of all registers (in registered OLMCs) are shifted "upward" and out onto the "SOOUT" output (pin 15*). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the SOOUT pin of each chip is connected to the SDIN pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into SDIN or out of SDOUT, VIL/VOL = register reset (0), and VIH/VOH = register set (1). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

*Applies to 24-pin DIP packages for GAL22V10; refer to the 28-lead PCC Connection Diagram for conversion.

**The SOOUT output buffer is an open drain output during preload. This pin should be terminated to VCC with a 10 kΩ resistor.

FIGURE 4. Output Register Preload Pinout

Register Preload Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Input Voltage (High)</td>
<td></td>
<td>2.40</td>
<td></td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Voltage (Low)</td>
<td></td>
<td>0.00</td>
<td></td>
<td>0.50</td>
<td>V</td>
</tr>
<tr>
<td>VIES</td>
<td>Register Preload Input Voltage</td>
<td></td>
<td>14.5</td>
<td>15</td>
<td>15.5</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output Voltage (High) (Note 1)</td>
<td></td>
<td></td>
<td></td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Voltage (High) (Note 1)</td>
<td>iOL ≤ 12 mA</td>
<td>0.00</td>
<td></td>
<td>0.50</td>
<td>V</td>
</tr>
<tr>
<td>IIL, IIL</td>
<td>Input Current (Programming)</td>
<td>±1</td>
<td></td>
<td>±10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>IOH</td>
<td>High Level Output Current (Note 1)</td>
<td>VOH ≤ VCC</td>
<td></td>
<td></td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>tPWV</td>
<td>Verify Pulse Width</td>
<td></td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>tD</td>
<td>Pulse Sequence Delay</td>
<td></td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>tRESET</td>
<td>Register Reset Time from Valid VCC</td>
<td></td>
<td>1</td>
<td>5</td>
<td>10</td>
<td>µs</td>
</tr>
</tbody>
</table>

Note 1: The SDOUT output buffer is an open drain output. This pin should be terminated to VCC with a 10 kΩ resistor.

Register Preload Waveforms

**The SDOUT output buffer is an open drain output during preload. This pin should be terminated to VCC with a 10 kΩ resistor.

FIGURE 5
OLMC Logic Diagram

FIGURE 6

TABLE II

<table>
<thead>
<tr>
<th>S1</th>
<th>S0</th>
<th>Output Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Registered/Active Low</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Registered/Active High</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Combinatorial/Active Low</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Combinatorial/Active High</td>
</tr>
</tbody>
</table>
GAL22V10 Logic Diagram

JEDEC Logic Array Cell Numbers = Product Line First Cell Number + Input Line Numbers

FIGURE 7
GAL20RA10-15, -20, -25
Generic Array Logic

General Description
The NSC E²CMOS™ GAL® device combines a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The GAL20RA10 is made up of ten Output Logic Macro Cells (OLMC). Four programmable AND array outputs feed into the fixed OR-gate for each OLMC to generate the device's output functions. Four other AND array outputs are used for control functions in the OLMC. With a robust mixture of logic derived controlled functions and selectable output data paths, the GAL20RA10 provides an ideal solution for registered random logic applications.

This device is housed in a 24-pin 300 mil DIP. A 28-pin PCC package is also available. It can be programmed by most PAL programmers.

Programming is accomplished using industry standard available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability of the GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features
- High performance E²CMOS technology
  - 15 ns maximum propagation delay
  - fCLK = 40 MHz
  - 15 ns maximum from clock input to data output
  - TTL compatible 16 mA outputs
  - UltraMOS® III advanced CMOS technology
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (<50 ms)
  - 20 year data retention
- 10 output logic macrocells
  - Maximum flexibility for complex logic designs
  - Programmable output polarity
  - Programmable asynchronous set and reset
  - Individually programmable clocks
  - Programmable and dedicated pin control of output
  - TRI-STATE®
  - Programmable Register bypass
  - TTL level Register preload
- Power-up reset for registered outputs
- JEDEC-compatible programming equipment and development software available
- Preload and power-up reset of all registers
  - 100% functional testability
- Full supported development software
- Electronic signature for identification
- Security fuse prevents direct copying of logic patterns
- JEDEC map identical to Bipolar PAL versions
### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Supply Voltage (VCC)**: -0.5V to +7.0V
- **Input Voltage (Note 2)**: -2.5V to VCC + 1.0V
- **Off-State Output Voltage (Note 2)**: -2.5V to VCC + 1.0V
- **Output Current**: ±100 mA
- **Storage Temperature**: -65°C to +150°C

Ambient Temperature with Power Applied: 65°C to +125°C
Junction Temperature: -65°C to +150°C
Lead Temperature (Soldering, 10 seconds): 260°C
ESD Tolerance: TBD
CZAP = 100 pF
RZAP = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

### Recommended Operating Conditions

**SUPPLY VOLTAGE AND TEMPERATURE**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Military</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>4.5</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Free-Air Temperature</td>
<td>0</td>
<td>25</td>
<td>75</td>
<td>-40</td>
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<tr>
<td>TC</td>
<td>Operating Case Temperature</td>
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</table>

**AC TIMING REQUIREMENTS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GAL20RA10-15</th>
<th>GAL20RA10-20</th>
<th>GAL20RA10-25</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>COM</td>
<td>COM/IND</td>
<td>MIL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>tSU</td>
<td>Set-Up Time (Input or Feedback before Clock)</td>
<td>10</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>tH</td>
<td>Hold Time (Input after Clock)</td>
<td>0</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>tW</td>
<td>Clock Pulse Width (High/Low)</td>
<td>10</td>
<td></td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>tCYCLE</td>
<td>Clock Cycle Period (with Feedback) (Note 3)</td>
<td>25</td>
<td></td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency (Note 4)</td>
<td>40</td>
<td></td>
<td>33</td>
<td></td>
</tr>
<tr>
<td>fI</td>
<td>Input Frequency (Note 5)</td>
<td>66.7</td>
<td></td>
<td>50.0</td>
<td></td>
</tr>
<tr>
<td>tPR</td>
<td>Clock Valid after Power-Up</td>
<td>100</td>
<td></td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

*Preliminary

**Note 1**: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside specified recommended operating conditions.

**Note 2**: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3**: tCYCLE = tSU + tCLK

**Note 4**: fCLK (with feedback) = (tCYCLE) / 1
fCLK (without feedback) = (2 tW) / 1

**Note 5**: \( t = (t_{PD}) / 1 \)
## Electrical Characteristics

Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Temperature Range</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td></td>
<td></td>
<td>2.0</td>
<td>V</td>
<td>VCC + 1</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td></td>
<td></td>
<td>-1.0</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VCC = Min</td>
<td></td>
<td>IOH = -3.2 mA</td>
<td>COM/IND</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IOH = -2.0 mA</td>
<td>MIL</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VCC = Min</td>
<td></td>
<td>IOL = 16 mA</td>
<td>COM/IND</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IOL = 16 mA</td>
<td>MIL</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>IOZH</td>
<td>High Level Off State Output Current</td>
<td>VCC = Max, VO = VCC Max</td>
<td></td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOZL</td>
<td>Low Level Off State Output Current</td>
<td>VCC = Max, VO = GND</td>
<td></td>
<td>-10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ii</td>
<td>Maximum Input Current</td>
<td>VCC = Max, VI = VCC Max</td>
<td></td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current</td>
<td>VCC = Max, VI = VCC Max</td>
<td></td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current</td>
<td>VCC = Max, VI = VCC Max</td>
<td></td>
<td>-10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IQS*</td>
<td>Output Short Circuit Current</td>
<td>VCC = 5.0V, VO = GND</td>
<td></td>
<td>-30</td>
<td>-160</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>f = 15 MHz, VCC = Max</td>
<td></td>
<td>COM</td>
<td>150</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MIL/IND</td>
<td>180</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Ci</td>
<td>Input Capacitance</td>
<td>VCC = 5.0V, VI = 2.0V</td>
<td></td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CI/O</td>
<td>I/O Capacitance</td>
<td>VCC = 5.0V, VI/O = 2.0V</td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*One output at a time for a maximum duration of one second

## Switching Characteristics

Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>GAL20RA10-15</th>
<th>GAL20RA10-20</th>
<th>GAL20RA10-25</th>
</tr>
</thead>
<tbody>
<tr>
<td>fPD</td>
<td>Input or Feedback to Combinatorial Output</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, S1 Closed</td>
<td>15</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Input to Registered Output or Feedback</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, S1 Closed</td>
<td>15</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>fS</td>
<td>Asynchronous Set Input to Registered Output Low</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, S1 Closed</td>
<td>15</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>fR</td>
<td>Asynchronous Reset Input to Registered Output High</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, S1 Closed</td>
<td>15</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>fPZXG</td>
<td>G Pin Output Enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>12</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>fPZG</td>
<td>G Pin Output Disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 5 pF, From VOH: S1 Open, From VOL: S1 Closed</td>
<td>12</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>fPZXI</td>
<td>Input to Output Enabled via Product Term</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Active High: S1 Open, Active Low: S1 Closed</td>
<td>15</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>fPIZI</td>
<td>Input to Output Disabled via Product Term</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 5 pF, From VOH: S1 Open, From VOL: S1 Closed</td>
<td>15</td>
<td>20</td>
<td>25</td>
</tr>
</tbody>
</table>
Ordering Information

- Generic Array Logic
- Number of Array Inputs
- Output Type
  - RA = Register Asynchronous
- Number of Outputs
- Speed
  - -15 = 15 ns
  - -20 = 20 ns
  - -25 = 25 ns
- Packaging Type
  - N = 24-Pin Plastic DIP
  - J = 24-Pin Ceramic DIP
  - V = 28-Lead Plastic Chip Carrier
- Temperature Range
  - C = Commercial (0°C to +75°C)
  - M = Military (−55°C to +125°C)
**Functional Description**

The GAL20RA10 logic array consists of 20 complementary input lines and 80 product-term lines with an EE program­mable cell at each intersection (3200 cell). The product terms are organized into ten groups of eight each. Four of the eight product terms in each group connect into an OR-gate to produce the sum-of-products logic function. The remaining four product terms in each group are used for control functions in the “Output Logic Macro Cell” (OLMC).

As shown in the GAL20RA10 Block Diagram a total of ten output logic functions are available. Under control of an OLMC each output may be designated either as a re­gistered output configuration or combinatorial.

The logic function output passes through a D-type Flip-Flop triggered by the rising edge of the clock which is defined by one product-term line.

Two product-terms are designated to set or reset the output register and to define the output configuration (register or combinatorial).

<table>
<thead>
<tr>
<th>Set</th>
<th>Reset</th>
<th>Output Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Register Mode</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Set</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Combinatorial Mode</td>
</tr>
</tbody>
</table>

All architecture cells are normally configured automatically by the development software.

**Connection Diagram**

**28-Lead PLCC**

The registers can be preloaded from the outputs by using TTL-level signals, in order to simplify functional testing. The preload signal overrides the set and reset signal.

**INDIVIDUALLY PROGRAMMABLE REGISTER BYPASS**

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

**PROGRAMMABLE CLOCK**

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

**PROGRAMMABLE AND HARD-WIRED TRI-STATE OUTPUTS**

The GAL20RA10 provides a product term dedicated to output control. There is also an output control pin (Pin 13). The output is enabled if both the output control pin is low and the output control product term is HIGH. If the output control pin is high all outputs will be disabled or if an output control product term is low, then that output will be disabled.

**PROGRAMMABLE OUTPUT POLARITY**

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-OR gates shown in the GAL20RA10 Logic Diagram. When the output polarity is unprogrammed the lower input to the exclusive-OR gate is high, so the output is active-high. Similarly, when the output polarity cell is 0, or a low impedance connection to GND, the output is active-low. The programmable output polarity features allows the user a high degree of flexibility when writing equations.

**REGISTER PRELOAD**

GAL20RA10 offers register preload for device testability. The registers can be preloaded from the outputs by using TTL-level signals, in order to simplify functional testing. The preload signal overrides the set and reset signal.

**POWER-UP RESET**

The GAL20RA10 device resets all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going transition.

**AC Test Load**

**MIL**

- R1 = 390 kΩ
- R2 = 750 kΩ

**COM/IND**

- R1 = 300 kΩ
- R2 = 300 kΩ

TL/L/10775-4

2-212
Clock/Input Frequency Specifications
The clock frequency (fCLK) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions feed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (fCLK -1 without feedback) is defined as the greater of the minimum “data window” period (tH high + tH low) and the minimum “data window” period (tSU + tSU). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (fCYCLE = fCLK -1 with feedback) is defined as fCLK + tSU. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle. The input frequency (fI) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The fI specification is derived as the inverse of the combinatorial propagation delay (tpd).

Design Development Support
A variety of software tools and programming equipment is available to support the development of designs using GAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible “cell-map” (analogous to a PAL “fuse-map”). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into a variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLANTM software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations. National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device. The special GAL programming algorithm can also program a GAL device using a standard fuse-map developed for any of the emulated PAL products. PAL fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL device into the programming unit (provided the PAL device has not been secured). However, to utilize the full flexibility of the GAL architecture, true GAL development software (such as PLAN software) is recommended.

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL logic array and OLMC are provided for direct map editing and diagnostic purposes (see “Programming Details”). For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

Security Cell
A security cell is provided on all GAL20V8A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell may be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature
Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at anytime independent of the state of the security cell. National’s PLANT development software allows electronic signature data to be entered by the user and down-loaded to the programming equipment.

Bulk Erase
The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection
GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching. To insure that no undesired bias conditions occur with P+ diffusions, a Latch-Lock™ power-up circuitry has been developed. The drain of all P channel devices normally connected to the device supply are now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.
Manufacturer Testing

Because of E²CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to data sheet specifications.

OLMC Configurations

Registered/Active Low

Registered/Active High

Combinatorial/Active Low

Combinatorial/Active High

Output Always Enabled

Programmable

Combination of Programmable and Hard-Wired

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional test include reprogramming each OLMC to all valid architectural configurations.
*Output macrocell shown is configured as an active high register output.

**Functional Description**

**Typical Registered Logic Function Without Feedback**

**Typical Registered Logic Function With Feedback**
FIGURE 1. "RA" Output Logic Macrocell Logic Diagram
GAL6001® Generic Array Logic

General Description

Using a high performance E²CMOS™ technology, National Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24 pin, 300-mil package.

The GAL6001 has ten programmable Output Logic MacroCells (OLMC) and eight programmable "buried" State Logic MacroCells (SLMC). In addition, there are ten input Logic MacroCells (ILMC) and ten I/O Logic MacroCells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows National to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature word is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

Features

- Electrically erasable cell technology
  - Instantly reconfigurable logic
  - Instantly reprogrammable cells
  - Guaranteed 100% yields
- High performance E²CMOS technology
  - Low power: 150 mA maximum
  - High speed:
    - 15 ns max. clock to output delay
    - 25 ns max. setup time
    - 30 ns max. propagation delay
- TTL compatible inputs and outputs
- Unprecedented functional density
  - 10 output logic macrocells
  - 8 state logic macrocells
  - 20 input and I/O logic macrocells
- High-level design flexibility
  - 78 x 64 x 36 FPLA architecture
  - Separate state register and input clock pins
  - Functionally superset existing 24-pin PAL® and IFL™ devices
  - Asynchronous clocking
- High speed programming algorithm
- 24-pin, 300-mil DIP or 28-lead PLCC
- 20-year data retention

Block Diagram - GAL6001

![Block Diagram of GAL6001](image)
Absolute Maximum Ratings

Supply Voltage \( V_{CC} \) \(-0.5\) to \(+7\) V
Input Voltage Applied \(-0.5\) to \(V_{CC} + 1.0\) V
Off-state Output Voltage Applied \(-0.5\) to \(V_{CC} + 1.0\) V
Storage Temperature \(-40^\circ\)C to \(+85^\circ\)C

Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>Supply Voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
</tr>
<tr>
<td>( T_A )</td>
<td>Ambient Temperature</td>
<td>0</td>
<td>75</td>
<td>-40</td>
</tr>
<tr>
<td>( T_C )</td>
<td>Case Temperature</td>
<td>0</td>
<td>75</td>
<td>-40</td>
</tr>
</tbody>
</table>

Capacitance (Note 1) \((T_A = 25^\circ\)C, \(f = 1.0\) MHz)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Maximum*</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_I )</td>
<td>Input Capacitance</td>
<td>( V_{CC} = 5.0) V, ( V_I = 2.0) V</td>
<td>8</td>
<td>pF</td>
</tr>
<tr>
<td>( C_O )</td>
<td>Output Capacitance</td>
<td>( V_{CC} = 5.0) V, ( V_O = 2.0) V</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>( C_B )</td>
<td>Bidirectional Pin Cap</td>
<td>( V_{CC} = 5.0) V, ( V_B = 2.0) V</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

*Guaranteed but not 100% tested.

Switching Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>5 ns (0.3V to 2.7V)</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>See Figure</td>
</tr>
</tbody>
</table>

3-state levels are measured 0.5V from steady-state active level.

GAL6001 Reset Timing Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>( \text{Min} )</th>
<th>Typ</th>
<th>( \text{Max} )</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PR} )</td>
<td>Reset Circuit Power-Up</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{RESET} )</td>
<td>Register Reset Time from Valid ( V_{CC} )</td>
<td>45</td>
<td>( \mu )S</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*\( C_L \) includes jig and probe total capacitance

TL/L/10561-2
Electrical Characteristics over recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Temp Range</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;IH&lt;/sub&gt;, I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Input Leakage Current</td>
<td>GND ≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt; Max</td>
<td>±10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;BZH&lt;/sub&gt;, I&lt;sub&gt;BZL&lt;/sub&gt;</td>
<td>Bidirectional Pin Leakage Current</td>
<td>GND ≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt; Max</td>
<td>±10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Operating Power Supply Current</td>
<td>F = 15 MHz, V&lt;sub&gt;CC&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; Max</td>
<td>IND</td>
<td>180</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Output Short Circuit (Note 1)</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.0V, V&lt;sub&gt;OUT&lt;/sub&gt; = GND</td>
<td>-30</td>
<td>-130</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Output Low Voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; Min</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 16 mA</td>
<td>COM/IND</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>Output High Voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; Min</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -3.2 mA</td>
<td>COM/IND</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Input Low Voltage</td>
<td></td>
<td>2.0</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; + 1</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: One Output at a time for a maximum duration of one second.

Switching Characteristics over recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>6001-30 COM</th>
<th>6001-35 COMM</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;OVQ1&lt;/sub&gt;</td>
<td>Delay from Input or I/O to Output (Note 1)</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 30</td>
<td>Max = 3540 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;OVQ2&lt;/sub&gt;</td>
<td>Delay from Input or I/O to Outputs Off (Disable)</td>
<td>R(Ω) = Infinite, C&lt;sub&gt;L&lt;/sub&gt; = 5 pF</td>
<td>Min = 5</td>
<td>Max = 25 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;DVCH&lt;/sub&gt;</td>
<td>Input or I/O Setup Time to OCLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 25</td>
<td>Max = 30 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;CHDV&lt;/sub&gt;</td>
<td>Input or I/O Hold Time after OCLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = -5</td>
<td>Max = -5 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;CHOV&lt;/sub&gt;</td>
<td>OCLK to Output Valid Delay</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 15</td>
<td>Max = 17.5 ns</td>
<td></td>
</tr>
<tr>
<td>Period 1</td>
<td>OCLK Cycle Time (t&lt;sub&gt;DVCH&lt;/sub&gt; + t&lt;sub&gt;CHDV&lt;/sub&gt;)</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 40</td>
<td>Max = 47.5 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;DVDS&lt;/sub&gt;</td>
<td>Input or I/O Setup Time to Sumterm CLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 7.5</td>
<td>Max = 8 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;DVDS&lt;/sub&gt;</td>
<td>Input or I/O Hold Time after Sumterm CLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 12.5</td>
<td>Max = 15 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;DVQV&lt;/sub&gt;</td>
<td>Sumterm CLK to Output Delay</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 35</td>
<td>Max = 40 ns</td>
<td></td>
</tr>
<tr>
<td>Period 2</td>
<td>STCLK Cycle Time (t&lt;sub&gt;DVDS&lt;/sub&gt; + t&lt;sub&gt;DVQV&lt;/sub&gt;)</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 42.5</td>
<td>Max = 48.5 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;DC1H&lt;/sub&gt;</td>
<td>Input or I/O Setup Time to ICLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 2.5</td>
<td>Max = 3.5 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;C1HD&lt;/sub&gt;</td>
<td>Input or I/O Hold Time after ICLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 5</td>
<td>Max = 6 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;C1H&lt;/sub&gt;</td>
<td>Delay from ICLK to Asynchronous Output Valid</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 35</td>
<td>Max = 40 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;C2H&lt;/sub&gt;</td>
<td>Register Setup Time after ICLK</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 30</td>
<td>Max = 35 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;C2C&lt;/sub&gt;</td>
<td>Input or I/O Setup Time to Latch</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 2.5</td>
<td>Max = 3.5 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;C2D&lt;/sub&gt;</td>
<td>Input or I/O Hold Time after Latch</td>
<td>R(Ω) = 300, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF</td>
<td>Min = 5</td>
<td>Max = 6 ns</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;RESET&lt;/sub&gt;</td>
<td>Input, I/O or Feedback to Reset</td>
<td>R(Ω) = 40, C&lt;sub&gt;L&lt;/sub&gt; = 45 pF</td>
<td>Min =</td>
<td>Max = ns</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: T = Time, D = Data, Q = Output, Z = HI-Z, V = Valid, H = High, L = Low, X = Change, C1 = OCLK, C2 = ICLK, D1 = Sumterm Clock Input

Differential Product Term (DPT) Switching Characteristics

The number of DPT that may switch in the same direction at the same time is limited to a maximum of 15.
The number of DPT for a given design is calculated by subtracting the total number of Product-Terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5 ns period.

\[ \text{DPT} = (\text{P-Terms})_{\text{HI}} - (\text{P-Terms})_{\text{HL}} \]
28-Lead PLCC Connection Diagram

GAL6001 Block Diagram—DIP Connections
Input Logic MacroCell (ILMC) and I/O Logic MacroCell (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2–11) and the IOLMC to the I/O pins (14–23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells (transparent when high) and as a clock for registered macrocells (positive edge triggered).

Configurable input blocks can be used to advantage by system designers. Registered inputs are popular for synchronization and data merging. Transparent latches are useful when the input data is invalid outside a known time window. Direct inputs are used in systems where the input data is well ordered in time. With the GAL6001, external registers and latches are not necessary.

The various configurations of the input and I/O macrocells are controlled by programming four architecture control bits (INLATCH, INSYN, IOLATCH, and IOSYN) within the 68-bit architecture control word. The SYN bits determine whether the macrocells will have register/latch capability or will be strictly asynchronous. The LATCH bits select between latched and registered inputs.

The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages. The truth table associated with each diagram shows the values of the LATCH and SYN bits required to set the macrocell to the configuration shown.

Output Logic MacroCell (OLMC) and State Logic MacroCell (SLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the State Logic MacroCells (SLMC), as they are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic MacroCells (OLMC).

Like the ILMC and IOLMC discussed above, output and state logic macrocells are configured by programming specific bits in the architecture control word (CKS(i), OUTSYN(i), XORD(i), XORER(i)), but unlike the input macrocells which must be configured in blocks, these macrocells are configurable on a macrocell-by-macrocell basis. Throughout this datasheet, \( i = \{14 \ldots 23\} \) for OLMCs and \( i = \{0 \ldots 7\} \) for SLMCs.

State and Output Logic MacroCells may be set to one of three valid configurations: combinational, D-type registered with sum term (asynchronous) clock, or D/E-type registered. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selectable through the XOR(i) architecture bits. Polarity selection is not necessary for SLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all “E” sum terms is selectable through the XOR(i) architecture control bits.

When CKS(i) = 1 and OUTSYN(i) = 0, macrocell “i” is set as “D/E-type registered”. In this configuration, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated “E” sum term. This configuration is useful for building counters and state-machines with state hold functions.

When CKS(i) = 0 and OUTSYN(i) = 0, macrocell “i” is set as “D-type registered with sum term clock”. In this configuration, the register is enabled and its “E” sum term is routed directly to the clock input. This allows for the popular “asynchronous programmable clock” feature, selectable on a register-by-register basis.

When CKS(i) = 0 and OUTSYN(i) = 1, macrocell “i” is set as “combinational”. Configuring a SLMC in this manner turns it into a complement array. Complement arrays are used to construct multi-level logic.

Registers in both the Output and State Logic MacroCells feature a RESET input. This active high input allows the registers to be simultaneously and asynchronously reset from a common signal. The source of this signal is the RESET product term. Registers reset to a logic zero, but since the output buffers invert, a logic one will be present at the device pins.

There are two possible feedback paths from each OLMC: one from before the output buffer (this is the normal path) and one from after the output buffer, through the IOLMCs. The second path is usable as a feedback only when the associated bi-directional pin is being used as an output; during input operations it becomes the input data path, turning the associated OLMC into an additional buried state macrocell.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register construct can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK- or T-register.

The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages. The truth table associated with each diagram shows the bit value of CKS(i) and OUTSYN(i) required to set the macrocell to the configuration shown.
**ILMC/IOLMC Configurations**

**ILMC/IOLMC Generic Block Diagram**

- **INPUT PINS**: 2-11
- **OR**
- **1/0 PINS**: 14-23

**Asynchronous Input**

- **INPUT PINS**: 2-11
- **OR**
- **1/0 PINS**: 14-23

**Registered Input**

- **INPUT PINS**: 2-11
- **OR**
- **1/0 PINS**: 14-23

**Latched Input**

- **INPUT PINS**: 2-11
- **OR**
- **1/0 PINS**: 14-23

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OLMC/SLMC Configurations

OLMC/SLMC Block Diagram

D/E Type Registered

D-Type Registered with Sum Term Asynchronous Clock

CKS(i) | OUTSYN(i)
-------|--------
1      | 0      

CKS(i) | OUTSYN(i)
-------|--------
0      | 0      

TL/L/10561-9

TL/L/10561-10

TL/L/10561-11
**Array Description**

The GAL6001 E\(^2\) reprogrammable array is subdivided into three smaller arrays: AND, OR and Architecture. These arrays are described in detail below.

**AND ARRAY**

The AND array is organized as 78 input terms by 75 product term outputs. The 20 input and I/O logic macrocells, 8 SLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise a total of 39 inputs to this array (each available in true and complemented forms). Product terms 0–63 serve as inputs to the OR array. Product term 64 is the RESET PT; it generates the RESET signal described in the earlier discussion of output and state logic macrocells. Product terms 65–74 are the output enable product terms; they control the output buffers, thus enabling device pins 14–23 to be bi-direction or TRI-STATE\(^\circ\).

**OR ARRAY**

The OR array is organized as 64 inputs by 36 sum term outputs. Product terms 0–63 of the AND array serve as the inputs to this array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 SLMCs, one "D" term and one "E" term to each.

**ARCHITECTURE ARRAY**

The various configurations of the GAL6001 are enabled by programming cells within the architecture control word. This 68-bit word contains all of the chip configuration data. This data includes: XORD(i), XORE(i), CKS(i), OUTSYN(i), INLATCH, INSYN, IOLATCH, and IOSYN. The function of each of these bits has been previously explained.

**Electronic Signature Word**

Every GAL6001 device contains an electronic signature word. The Electronic Signature word is a 72-bit user definable area, which can be used to store inventory control data, pattern revision numbers, manufacture date, etc. Signature data is always available to the user, regardless of the state of the security cell.

**Security Cell**

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns.

Once programmed, this cell prevents further read access to the AND, OR and architecture arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Electronic Signature data is always available to the user, regardless of the state of this control cell.

**Bulk Erase**

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 ms.

**Register Preload**

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal machine operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the input, I/O, and state registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

**Input Buffers**

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristic high impedance, load driving logic much less than "traditional bipolar devices". This allows for a greater fan out from the driving logic.

GAL devices do not possess active pull-ups within their input structures. As a result, National recommends that all unused inputs and TRI-STATE I/O pins be connected to another active input, V\(_{CC}\), or GND. Doing this will tend to improve noise immunity and reduce I\(_{CC}\) for the device.
Power-Up Reset

Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tRESET). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, the following conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the VCC rise must be monotonically. Second, the clock inputs must become a proper TTL level within the specified time (tPR). The registers will reset within a maximum of tRESET time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

- **Generic Array Logic Family**: GAL
- **Device Number**: 6001
- **Speed**:
  - −30 = 30 ns tpd
  - −35 = 35 ns tpd
- **L** = Half Power
  (150 mA for GAL6001)
- **Package Type**:
  - **N** = 24-Pin Plastic DIP
  - **J** = 24-Pin Ceramic DIP
  - **V** = 28-Lead Plastic Chip Carrier (PLCC)
- **Temperature Range**:
  - **C** = Commercial (0°C to +75°C)
  - **I** = Industrial (−40°C to +85°C)

TL/L/10561-13

TL/L/10561-13
General Description

The PAL1016P8/10016P8 is the first member of an ECL programmable logic device family possessing common electrical characteristics, utilizing an easily accommodated programming procedure, and produced with National Semiconductor's advanced oxide-isolated process. This family includes combinatorial, and registered output devices. These devices are fabricated using National's proven Ti-W (Titanium-Tungsten) fuse technology to allow fast, efficient, and reliable programming.

This family allows the designer to quickly implement the defined logic function by removing the fuses required to properly configure the internal gates and/or registers. Product terms with all fuses removed assume a logical high state. All devices in this series are provided with an output polarity fuse that, if removed, will permit any output to independently provide a logic low when the equation is satisfied. When these fuses are intact the outputs provide a logic true (most positive voltage level) in response to the input conditions defined by the applicable equation. All input and I/O pins have on-chip 50 kΩ pull-down resistors.

Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams to create fuse maps representing the programmed device. All devices in this family can be programmed using conventional programmers. After the device has been programmed and verified, an additional fuse may be removed to inhibit further verification or programming. This "security" feature can provide a proprietary circuit which cannot easily be duplicated.

Features
- \( t_{PD} \leq 6 \, \text{ns max} \)
- Eight combinatorial outputs with programmable polarity
- Programmable replacement for conventional ECL logic
- Both 10KH and 100K I/O compatible versions
- Simplifies prototyping and board layout
- 24-pin thin DIP packages.
- Programmed on conventional TTL PLD programmers
- Security fuse to prevent direct copying
- Reliable titanium-tungsten fuses

Ordering Information

Programmable Array Logic Family
- ECL I/O Compatibility
  - 10 = 10KH
  - 100 = 100K
- Number of Array Inputs
- Output Type
  - P = Programmable Polarity
- Number of Outputs
- Package
  - J = 24-Pin Ceramic DIP
- Temperature Range
  - C = Commercial:
    - 0°C to +75°C for 10KH
    - 0°C to +85°C for 100K
Absolute Maximum Ratings
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Temperature Under Bias (Ambient): -55°C to +125°C
- Storage Temperature Range: -65°C to +150°C
- VEE Relative to VCC: -7V to +0.5V
- Any Input Relative to VCC: VEE to +0.5V

Lead Temperature (Soldering, 10 seconds): 300°C
ESD Tolerance: 1000V
CZAP = 100 pF
RZAP = 1500 Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEE</td>
<td>Supply Voltage</td>
<td>10 kH</td>
<td>-5.46</td>
<td>-5.2</td>
<td>-4.94</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 k</td>
<td>-4.73</td>
<td>-4.5</td>
<td>-4.27</td>
<td></td>
</tr>
<tr>
<td>RL</td>
<td>Standard 10 kH/100k Load</td>
<td>50</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL</td>
<td>Standard 10 kH/100k Load</td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating Ambient Temperature</td>
<td>10 kH</td>
<td>0</td>
<td>+75</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 k</td>
<td>0</td>
<td>+85</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics

Over Recommended Operating Conditions. Output Load = 50Ω to -2.0V.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td>Guaranteed input voltage high for all inputs</td>
<td>10 kH</td>
<td>0°C</td>
<td>-1170</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-1130</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-1070</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td>-1165</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed input voltage low for all inputs</td>
<td>10 kH</td>
<td>0°C</td>
<td>-1480</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-1480</td>
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<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-1450</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td>-1810</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VIN = VIH Max. or VIL Min.</td>
<td>10 kH</td>
<td>0°C</td>
<td>-1020</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-980</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-920</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td>-1025</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VIN = VIH Max. or VIL Min.</td>
<td>10 kH</td>
<td>0°C</td>
<td>-1950</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-1950</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-1950</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td>-1810</td>
</tr>
<tr>
<td>IIH</td>
<td>High Level Input Current</td>
<td>VIN = VIH Max.</td>
<td>10 kH</td>
<td>0°C</td>
<td>220</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current</td>
<td>VIN = VIL Min. Except I/O Pins</td>
<td>10 kH</td>
<td>0°C</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td></td>
</tr>
<tr>
<td>IE</td>
<td>Supply Current</td>
<td>VEE = Max. All inputs and outputs open</td>
<td>10 kH</td>
<td>0°C to 75°C</td>
<td>-240</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 k</td>
<td>0°C to 85°C</td>
<td></td>
</tr>
</tbody>
</table>

Note: This product family has been designed to meet the specification in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
Switching Characteristics
Over Recommended Operating Conditions; Output load: \( R_L = 50\Omega \) to \(-2.0\text{V}\), \( C_L = 5\text{pF} \) to GND.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>Input to Output*</td>
<td></td>
<td>4</td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Output Rise Time</td>
<td></td>
<td>0.5</td>
<td>1</td>
<td>2.5</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Fall Time</td>
<td></td>
<td>0.5</td>
<td>1</td>
<td>2.5</td>
<td>ns</td>
</tr>
</tbody>
</table>

*Measure \( t_{pd} \) at threshold points

Connection Diagram

Dual-In-Line Package

![Connection Diagram](image_url)

Top View

PAL Design
The first step in designing a PAL device is the selection of the appropriate device to accommodate the logic equations. This is accomplished by partitioning the system into logic blocks with a defined number of inputs and outputs. Next, a device with an equal or greater I/O capability is selected to implement each logic block. The assignment of inputs and outputs to specific pins follows the device selection.

This device selection procedure is most easily accomplished with the use of computer software such as the PLANTM package of programs by National Semiconductor Corporation, but can be done manually using the logic diagram and logic symbols provided in this document.

Specifying the Fuse Pattern
Once a device with pinout is selected, the fuse pattern may be specified. The best procedure is the use of the PLANT, or a similar software package which will create the fuse pattern from the defined logic for the device and download the pattern to a programmer. Most common device programmers are provided with an RS–232 port which accesses the data provided in JEDEC or a selected HEX format.

Logic diagrams can be translated to PAL logic diagrams if desired. Fuses left intact are indicated on the logic diagram by an "X" at the intersection of the input line and the AND gate product line. A blown fuse is not marked. The PAL logic diagrams are provided with no fuse locations marked, allowing the designer to use the diagram to manually create a fuse map. Actually, the unprogrammed device is shipped with all Xs (fuses) intact. Each fuse node is identified by a product line number and an input line number. Each device in the ECL PAL family has the capability for its output polarity to be user-determined. The selection of output polarity is logically determined by the equations and implemented, if an active low output is required, by removing the fuse representing the appropriate output.

National Masked Logic
If a large number of devices with the same pattern are required, it may be more economical to consider mask programming. These mask-programmed devices will meet or exceed all of the performance specifications of the fuse-programmed devices they replace.

To generate a mask-programmed device, National Semiconductor requires a set of logic equations, written in a format such as PLAN, plus test vectors which the user generates as acceptance criteria for the finished product.
JEDEC logic array cell number = product line first cell number + input line number.
Programming Specification

This specification defines the programming and verification procedure for the first programmable logic devices in National's generic ECL family. The internal fuse array consists of 64 product lines (8 for each output), each containing 32 fuse locations (1 for each of 16 inputs and its complement) for a total of 2048 array fuses. Eight additional fuses exist to allow changing the active output polarity.

Each ECL device is programmed and verified as a 2048x1 TTL PROM. The connection diagrams in Figure 1 illustrate the difference between the logical ECL device and the PROGRAMMABLE TTL device.

For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor.

FIGURE 1. Connection Diagrams
Array Fuse Addressing
When programming or verifying a fuse location, the output (equation) is addressed by the 3 address pins 13, 14, and 15. The eight product lines, within the equation, are selected by the 3 address pins 9, 10, and 11. The fuse pair locations representing the logical inputs are selected by the 4 address pins 2, 3, 22, and 23, with the complementing fuse within the pair by the address pin 1. The programming address data is detailed in Tables I–III.

Table I. Logic Output (Equation) Selection vs. Programming Address Inputs.

<table>
<thead>
<tr>
<th>Output Pin</th>
<th>Address Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>15</td>
</tr>
<tr>
<td>21</td>
<td>0</td>
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<td>4</td>
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<td>20</td>
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<td>5</td>
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<td>18</td>
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<td>7</td>
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<td>17</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>

Note that the sequence of outputs represent the physical, not numeric, order of logical outputs.

Table II. Product Line (within Equation, or Output) vs. Programming Address Inputs.

<table>
<thead>
<tr>
<th>Product Pin</th>
<th>Address Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>11</td>
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<tr>
<td>0</td>
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<tr>
<td>1</td>
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<td>6</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
</tr>
</tbody>
</table>

Table III. Input Line Selection vs. Programming Address Inputs.

<table>
<thead>
<tr>
<th>Input Line</th>
<th>Address Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>23</td>
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<td>0</td>
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<tr>
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<td>30</td>
<td>1</td>
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<tr>
<td>31</td>
<td>1</td>
</tr>
</tbody>
</table>

Note pin 1 affects complementing fuse only.
**Fuse Programming and Verification**

The array and output polarity fuse programming waveform diagram is shown in Figure 2. The 8 output pins $O_N$ are used only to change the polarity of the selected device output and for removing the “security” fuse. Tables 4 and 5 define the voltage and timing requirements.

**Programming Procedure**

1. Power is applied to the device. VCC, VCC1, and VCC2 (pins 24, 6, and 19) go to VCC. (The voltage applied to pin 24 cannot precede the voltage applied to pin 6) The output pins (4, 5, 7, 8, 17, 18, 20, and 21), are open-circuited, or held at a logic low level, while programming the array.

2. After $T_0$, VCC1 (pin 6) can be raised from 5.0 to 10.75V at a slew rate not to exceed 10V/$\mu$s, or not less than 1V/$\mu$s.

3. The 11 address inputs (pins 1–3, 9–11, 13–15, 22, and 23) will define the location of the array fuse to be opened or the applicable output pin will define the polarity fuse to be opened.

4. After VCC1 has been stable at 10.75V for period $T_1$ and the address has been stable defining the applicable fuse location for period $T_2$, VCC2 (pin 19) may slew from 5.0 to 10.75V at a slew rate of 1 to 10V/$\mu$s.

5. VCC2 must remain stable at 10.75V for the duration of the programming pulse ($T_P$) before returning to 5.0V.

6. With VCC1 at 10.75V and after VCC2 has been stable at 5.0V for the period $T_3$, VER pin (16) may be sampled. If the fuse was properly opened, a logic low level will be observed. If the fuse did not open, steps 4 through 6 may be repeated up to 15 times.

7. If additional locations are to be addressed, steps 3 through 6 must be repeated for each fuse to be opened while observing the maximum power up time and duty cycle.

**Fuse Verification**

Fuse verification may be performed independent of programming. As seen in Figure 2, with VCC1 at VCCP and VCC2 at VCC verification may occur within the defined timing constraints. (See Table V)

---

**Figure 2. Array/Polarity Programming Diagram**
### TABLE IV. DC Requirements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Pin 24 Voltage While Programming or Verifying (Pin 19 Verifying) (Note 1)</td>
<td>4.75</td>
<td>5.00</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Icc</td>
<td>Pin 24 Current While Programming (Note 2)</td>
<td>200</td>
<td>300</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>VCCP</td>
<td>VCC1/VCC2 (Pins 6 and 19) Voltage While Programming (Note 3)</td>
<td>10.50</td>
<td>10.75</td>
<td>11.00</td>
<td>V</td>
</tr>
<tr>
<td>ICC1</td>
<td>VCC1 (Pin 6) Current While Programming (Note 2)</td>
<td>300</td>
<td>450</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>ICC2</td>
<td>VCC2 (Pin 19) Current While Programming (Note 2)</td>
<td>10</td>
<td>25</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Level - If Left Open, Pins 4, 5, 7, 8, 17, 18, 20, and 21 are Held Low by Internal 50K Resistor</td>
<td>0</td>
<td>0.8</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>IlL</td>
<td>Input LOW Current - Pins; 1–3, 9–11, 13–15, 22, and 23 ( VCC/VCC1/VCC2 = \max, V_{IN} = 0.4\text{V} )</td>
<td>-1.0</td>
<td>-1.5</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Current - Pins; 4, 5, 7, 8, 17, 18, 20, and 21 ( VCC/VCC1/VCC2 = \max, V_{IN} = 0.8\text{V} )</td>
<td>-0.25</td>
<td>-1.5</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>VIL</td>
<td>Input HIGH Level</td>
<td>2.20</td>
<td>-</td>
<td>( VCC )</td>
<td>V</td>
</tr>
<tr>
<td>IhL</td>
<td>Input HIGH Current ( VCC/VCC1/VCC2 = \max, V_{IN} = VCC \text{Max} ) ( \text{Pins 1–3, 9–11, 13–15, 22, and 23} )</td>
<td>90</td>
<td>300</td>
<td>-</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>VIL</td>
<td>Input HIGH Current ( VCC/VCC1/VCC2 = \max, V_{IN} = VCC \text{Max} ) ( \text{Pins 4, 5, 7, 8, 17, 18, 20, and 21} )</td>
<td>3</td>
<td>5</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>VOH</td>
<td>Output (Pin 16) LOW Level ( VCC/VCC1/VCC2 = \min, I_{OL} = 4\text{mA} )</td>
<td>0.8</td>
<td>-</td>
<td>2.20</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output (Pin 16) HIGH Level ( VCC/VCC1/VCC2 = \max, I_{OH} = -0.6\text{mA} )</td>
<td>0.8</td>
<td>-</td>
<td>2.20</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 1:** While programming/verifying, power can be applied to the device for 5 mS maximum with a duty cycle of 20% maximum.

**Note 2:** Current measurements are taken with \( VCC/VCC1/VCC2 \) at maximum and with all device inputs and outputs open.

**Note 3:** The difference between \( VCC \) and \( VCCp \) must not exceed 6V.

**Note 4:** If \( V_{IN} (VII) \) is less than 0.8 volts at pins 4, 5, 7, 8, 17, 18, 20, or 21, means must be provided to limit the current sourced by the device pins to 10 mA.

**Note 5:** All programming and verification to be performed at 25°C ±5°C.

### TABLE V. Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TO</td>
<td>Power-Up Before Raising ( VCC1 ) (Note 1)</td>
<td>0</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T1</td>
<td>( VCC1 ) at ( VCCp ) Before Raising ( VCC2 )</td>
<td>400</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T2</td>
<td>Address Set-Up Time to ( VCC2 &gt; VCCP )</td>
<td>400</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T3</td>
<td>VER Valid After ( VCC2 ) at ( VCC ) (Note 2)</td>
<td>200</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T4</td>
<td>( VCC2 ) at ( VCC ) Before Lowering ( VCC1 )</td>
<td>400</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T5</td>
<td>VER Valid After Raising ( VCC1 ) (Note 2)</td>
<td>200</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T5b</td>
<td>Address Set-Up Time to VER Valid (Note 2)</td>
<td>200</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T6</td>
<td>VER Valid Hold Time From Address</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T7</td>
<td>( VCC2 ) at ( VCC ) Before Address Change</td>
<td>400</td>
<td>500</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T8</td>
<td>VER Valid Hold Time From ( VCC2 &gt; VCCP ) (Note 2)</td>
<td>0</td>
<td>100</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>T9</td>
<td>( VCC1 ) at ( VCC ) Before Power Down</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>TP</td>
<td>Programming Pulse</td>
<td>10</td>
<td>10</td>
<td>30</td>
<td>( \mu\text{s} )</td>
</tr>
</tbody>
</table>

**Note 1:** Observe the maximum power-up time or 5 ms and duty cycle of 20% for \( VCC/VCC1/VCC2 \) during programming.

**Note 2:** VER is valid when \( VCC2 = VCC \) and \( VCC1 = VCCP \).
Security Fuse Programming
The security fuse is opened using the same procedure as used for changing the output polarity, except all 8 outputs (pins 4, 5, 7, 8, 17, 18, 20, and 21) must be selected with the application of $V_{IH}$. Verification is determined by the inability to further verify the array.

FIGURE 3. Security Fuse Programming Diagram
PAL10/10016P8-3 (DIP Only)
3 ns ECL ASPECT™ Programmable Array Logic

General Description
The PAL10/10016P8-3 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of applications—specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016P8-3 logic array has a total of 16 complementary input pairs, 64 product terms and 8 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features
- High speed: $t_{PD} = 3$ ns max
- Programmable replacement for ECL logic
- Both 100K and 10 KH I/O compatible versions
- Eight output functions with programmable polarity
- Improved programmability tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully supported by PLAN™ software
- Commercial and Military ranges

Ordering Information

- Programmable Array Logic Family
- ECL I/O Compatibility:
  - 10 = ECL 10K
  - 100 = ECL 100K
- Number of Array Inputs
- Output Type:
  - P = Programmable Polarity
- Number of Outputs
- Speed Version: $-3 = 3$ ns $t_{PD}$
- Packaging:
  - N = 24-Pin Plastic DIP
  - J = 24-Pin Ceramic DIP
  *Note: For PLCC see PAL10/10016PE8-3
- Temperature Range:
  - C = Commercial:
    - 0°C to +75°C for 10K
    - 0°C to +85°C for 100K
  - M = Extended (Military):
    - -55°C to +125°C for 10K
    - 0°C to +125°C for 100K

Block Diagram

TL/L/10714-1
### Absolute Maximum Ratings

- **Output Current**: $-50\, \text{mA}$
- **Temperature under Bias**: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
- **Storage Temperature Range**: $-65^\circ\text{C}$ to $+150^\circ\text{C}$
- **$V_{\text{EE}}$ Relative to $V_{\text{CC}}$**: $-7\, \text{V}$ to $+0.5\, \text{V}$
- **Input Voltage**: $V_{\text{EE}}$ to $+0.5\, \text{V}$

### Lead Temperature (Soldering, 10 Seconds)
- 300°C

### ESD Tolerance
- $C_{\text{ZAP}} = 100\, \text{pF}$
- $R_{\text{ZAP}} = 1500\, \Omega$

### Test Specification
- Human Body Model
- Test Specification: NSC SOP-5-028

### Storage Temperature Range
- $65^\circ\text{C}$ to $+150^\circ\text{C}$

### Recommended Operating Conditions for Commercial Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_A$</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{EE}}$</td>
<td>Supply Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>10KH</td>
<td>$0^\circ\text{C}$</td>
<td>$-1170$</td>
<td>$-840$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High for All Inputs</td>
<td>10KH</td>
<td>$+25^\circ\text{C}$</td>
<td>$-1130$</td>
<td>$-810$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$+75^\circ\text{C}$</td>
<td>$-1070$</td>
<td>$-735$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Guaranteed Input Voltage</td>
<td>10KH</td>
<td>$0^\circ\text{C}$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low for All Inputs</td>
<td>10KH</td>
<td>$+25^\circ\text{C}$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$+75^\circ\text{C}$</td>
<td>$-1950$</td>
<td>$-1450$</td>
</tr>
<tr>
<td></td>
<td>Operating Temperature (Note)</td>
<td></td>
<td>10KH</td>
<td>$0^\circ\text{C}$ to $+85^\circ\text{C}$</td>
<td>$-1165$</td>
<td>$-880$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ\text{C}$ to $+85^\circ\text{C}$</td>
<td>$-1810$</td>
<td>$-1475$</td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Conditions

#### Output Load = 50Ω to $-2\, \text{V}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_A$</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{IH}}$</td>
<td>High Level Input Current</td>
<td>$V_{\text{IN}} = V_{\text{IH}}, \text{Max}$</td>
<td>10KH</td>
<td>$0^\circ\text{C}$</td>
<td>220</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ\text{C}$ to $+85^\circ\text{C}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{IL}}$</td>
<td>Low Level Input Current</td>
<td>$V_{\text{IN}} = V_{\text{IL}}, \text{Min}$</td>
<td>10KH</td>
<td>$0^\circ\text{C}$</td>
<td>0.5</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ\text{C}$ to $+85^\circ\text{C}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{EE}}$</td>
<td>Supply Current</td>
<td>$V_{\text{EE}} = \text{Min}$</td>
<td>10KH</td>
<td>$0^\circ\text{C}$ to $+75^\circ\text{C}$</td>
<td>$-220$</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All Inputs and Outputs Open</td>
<td>100K</td>
<td>$0^\circ\text{C}$ to $+85^\circ\text{C}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Operating temperatures for circuits in J and N packages are specified as ambient temperatures ($T_A$) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
### Absolute Maximum Ratings

- **Temperature under Bias:** 
  - $-55^\circ C$ to $+125^\circ C$
- **Storage Temperature Range:** 
  - $-65^\circ C$ to $+150^\circ C$
- **$V_{EE}$ Relative to $V_{CC}$:** 
  - $-7V$ to $+0.5V$
- **Input Voltage:** 
  - $V_{EE}$ to $+0.5V$

- **Output Current:** 
  - 50 mA
- **Lead Temperature (Soldering, 10 Seconds):** 
  - 300°C
- **ESD Tolerance:** 
  - TBD
- **$C_{ZAP} = 100 \ pF$**
- **$R_{ZAP} = 1500\Omega$**
- **Test Method:** Human Body Model
- **Test Specification:** NSC SOP-5-028

### Recommended Operating Conditions

#### for Extended (Military) Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Unit</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{EE}$</td>
<td>Supply Voltage</td>
<td>$V$</td>
<td>10KH</td>
<td>$-5.46$</td>
<td>$-5.2$</td>
<td>$-4.94$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$-4.80$</td>
<td>$-4.5$</td>
<td>$-4.20$</td>
</tr>
<tr>
<td>$T$</td>
<td>Operating Temperature (Note)</td>
<td>$^\circ C$</td>
<td>10KH</td>
<td>$-55$</td>
<td>+125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0</td>
<td>+125</td>
<td></td>
</tr>
</tbody>
</table>

#### Electrical Characteristics

Over Recommended Operating Conditions Output Load = 50kΩ to −2.0V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_A$</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
</table>
| $V_{IH}$ | High Level Input Voltage | Guaranteed Input Voltage 
High for All Inputs | $10KH$ | $-55^\circ C$ | $-1250$ | $-930$ | mV |
|         |                                |           |      | $+25^\circ C$ | $-1130$ | $-810$ |
|         |                                |           |      | $+125^\circ C$ | $-1000$ | $-660$ |
|         |                                |           | 100K | $0^\circ C$ to $+125^\circ C$ | $-1165$ | $-880$ |
| $V_{IL}$ | Low Level Input Voltage   | Guaranteed Input Voltage 
Low for All Inputs | $10KH$ | $-55^\circ C$ | $-1950$ | $-1480$ | mV |
|         |                                |           |      | $+25^\circ C$ | $-1950$ | $-1480$ |
|         |                                |           |      | $+125^\circ C$ | $-1950$ | $-1420$ |
|         |                                |           | 100K | $0^\circ C$ to $+125^\circ C$ | $-1810$ | $-1475$ |
| $V_{OH}$ | High Level Output Voltage  | $V_{IN} = V_{IH}$ Max or $V_{IL}$ Min | $10KH$ | $-55^\circ C$ | $-1110$ | $-930$ | mV |
|         |                                |           |      | $+25^\circ C$ | $-980$ | $-810$ |
|         |                                |           |      | $+125^\circ C$ | $-830$ | $-660$ |
|         |                                |           | 100K | $0^\circ C$ to $+125^\circ C$ | $-1025$ | $-880$ |
| $V_{OL}$ | Low Level Output Voltage | $V_{IN} = V_{IH}$ Max or $V_{IL}$ Min | $10KH$ | $-55^\circ C$ | $-1950$ | $-1630$ | mV |
|         |                                |           |      | $+25^\circ C$ | $-1950$ | $-1630$ |
|         |                                |           |      | $+125^\circ C$ | $-1950$ | $-1570$ |
|         |                                |           | 100K | $0^\circ C$ to $+125^\circ C$ | $-1810$ | $-1620$ |
| $I_{IH}$ | High Level Input Current | $V_{IN} = V_{IH}$ Max | $10KH$ | $-55^\circ C$ | 220 | $\mu A$ |
|         |                                |           |      | $+125^\circ C$ |      |       |
| $I_{IL}$ | Low Level Input Current  | $V_{IN} = V_{IL}$ Min | $10KH$ | $-55^\circ C$ | 0.5 | $\mu A$ |
|         |                                |           |      | $+125^\circ C$ |      |       |
| $I_{EE}$ | Supply Current            | $V_{EE} = \text{Min}$ 
All Inputs and Outputs Open | $10KH$ | $-55^\circ C$ to $+125^\circ C$ | $-220$ | mA |
|         |                                |           | 100K | $0^\circ C$ to $+125^\circ C$ |       |       |

**Note:** Operating temperatures for circuits in J and N packages are specified as ambient temperatures ($T_A$) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

*Extended (Military) range available in J package only.*
Switching Characteristics

Over Recommended Operating Conditions, Output load: \( R_L = 50\Omega \) to \(-2.0V\), \( C_L = 5 \) pF to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured Test Conditions</th>
<th>Comm</th>
<th>Mil</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Input to Output</td>
<td>Measured at Threshold Points (Note 1)</td>
<td>3.0</td>
<td>4.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Output Rise Time</td>
<td>Measured between 20% and 80% Points</td>
<td>0.25</td>
<td>1.25</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Fall Time</td>
<td></td>
<td>0.25</td>
<td>1.25</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: All AC Measurements are to be made from Threshold Point.

\[ V_{IH} = \text{Threshold} + 400 \text{mV} \]

\[ V_{IL} = \text{Threshold} - 400 \text{mV} \]

\[ \text{Threshold} = \frac{V_{IN\text{Min}} + V_{IL\text{Max}}}{2} \]

<table>
<thead>
<tr>
<th>Part</th>
<th>Temp</th>
<th>( V_{IN\text{Min}} )</th>
<th>( V_{IL\text{Max}} )</th>
<th>Threshold</th>
<th>( V_{IH} )</th>
<th>( V_{IL} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kH</td>
<td>-55°C</td>
<td>-1250</td>
<td>-1480</td>
<td>-1365</td>
<td>-965</td>
<td>-1765</td>
</tr>
<tr>
<td></td>
<td>0°C</td>
<td>-1170</td>
<td>-1480</td>
<td>-1325</td>
<td>-925</td>
<td>-1725</td>
</tr>
<tr>
<td></td>
<td>25°C</td>
<td>-1130</td>
<td>-1480</td>
<td>-1300</td>
<td>-900</td>
<td>-1700</td>
</tr>
<tr>
<td></td>
<td>75°C</td>
<td>-1070</td>
<td>-1450</td>
<td>-1260</td>
<td>-860</td>
<td>-1660</td>
</tr>
<tr>
<td></td>
<td>125°C</td>
<td>-1000</td>
<td>-1420</td>
<td>-1210</td>
<td>-810</td>
<td>-1610</td>
</tr>
<tr>
<td>100k</td>
<td>All</td>
<td>-1165</td>
<td>-1475</td>
<td>-1300</td>
<td>-900</td>
<td>-1700</td>
</tr>
</tbody>
</table>

Timing Measurements

Test Load

Connection Diagram
Functional Testing
As with all field-programmable devices, the user of the ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that devices be functionally tested before being installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor's Application Note #351 and the Programmable Logic Design Guide.

Design Development Support
A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be downloaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL10/10016P8-3 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Programmer Support

<table>
<thead>
<tr>
<th>Advin Systems</th>
<th>Sailor PAL</th>
<th>V8.40</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data I/O</td>
<td>Unisile 40</td>
<td>V2.20</td>
</tr>
<tr>
<td>Digelec</td>
<td>Model 860</td>
<td>VA-3.2</td>
</tr>
<tr>
<td>International Microsystems</td>
<td>ECL-2</td>
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</tr>
<tr>
<td>Logical Devices</td>
<td>Allpro</td>
<td>V1.44C</td>
</tr>
<tr>
<td>SMS</td>
<td>Palpro 2x</td>
<td>V4.0</td>
</tr>
<tr>
<td>Stag Microsystems</td>
<td>Sprint Plus</td>
<td>V3.2J</td>
</tr>
<tr>
<td></td>
<td>ZL30A</td>
<td>V31</td>
</tr>
</tbody>
</table>
National Semiconductor

PAL10/10016PE8-3 (PLCC Only)
3 ns ECL ASPECT™ Programmable Array Logic

General Description

The PAL10/10016PE8-3 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of applications—specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016PE8-3 logic array has a total of 16 complementary input pairs, 64 product terms and 8 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard conventional TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features

- High speed: $t_{PD} \leq 3 \text{ ns max}$
- Full 28-pin function (all pins used)
- Programmable replacement for ECL logics
- Both 100K and 10 KH I/O compatible versions
- Eight output functions with programmable polarity
- Security fuse to prevent direct copying
- Fully supported by PLAN and other industrial software
- High density-high performance 28-pin PLCC package

Ordering Information

Programmable Array Logic Family
ECL I/O Compatibility:
10 = ECL 10KH
100 = ECL 100K
Number of Array Inputs
Output Type:
PE = Expanded Programmable Polarity (No I/O Pins/PLCC only)
Number of Outputs
Speed Version: $-3 = 3 \text{ ns } t_{PD}$
Packaging: V = 28-Pin PLCC
Note: For DIP see PAL10/10016P8-3 datasheet
Temperature Range:
C = Commercial:
0°C to +75°C for 10KH
0°C to +85°C for 100K

Block Diagram
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Temperature under Bias: $-55^\circ C$ to $+125^\circ C$
- Storage Temperature Range: $-65^\circ C$ to $+150^\circ C$
- $V_{EE}$ Relative to $V_{CC}$: $-7V$ to $+0.5V$
- Input Voltage: $V_{EE}$ to $+0.5V$

Output Current: $-50mA$
Lead Temperature (Soldering, 10 Seconds): TBD
ESD Tolerance: $C_{2AP} = 100 \ pF$
$R_{2AP} = 15000$
Test Method: Human Body Model
Test Specification: NSC SOP-5028

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$TA$</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{EE}$</td>
<td>Supply Voltage</td>
<td>10KH</td>
<td>Min</td>
<td>$-5.46$</td>
<td>$-5.2$</td>
<td>$-4.94$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>Min</td>
<td>$-4.80$</td>
<td>$-4.5$</td>
<td>$-4.20$</td>
<td>V</td>
</tr>
<tr>
<td>$T$</td>
<td>Operating Temperature (Note)</td>
<td>10KH</td>
<td>Min</td>
<td>$0$</td>
<td>$75$</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>Min</td>
<td>$0$</td>
<td>$85$</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics

Over Recommended Operating Conditions Output Load = $50\Omega$ to $-2.0V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$TA$</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>Guaranteed Input Voltage High for All Outputs</td>
<td>10KH</td>
<td>$0^\circ C$</td>
<td>$-1170$</td>
<td>$-1130$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-1170$</td>
<td>$-735$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-1170$</td>
<td>$-735$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1165$</td>
<td>$-880$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed Input Voltage Low for All Inputs</td>
<td>10KH</td>
<td>$0^\circ C$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1810$</td>
<td>$-1475$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{IN} = V_{IH}$ Max or $V_{IL}$ Min</td>
<td>10KH</td>
<td>$0^\circ C$</td>
<td>$-1020$</td>
<td>$-840$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-980$</td>
<td>$-810$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-920$</td>
<td>$-735$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1025$</td>
<td>$-880$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{IN} = V_{IH}$ Max or $V_{IL}$ Min</td>
<td>10KH</td>
<td>$0^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$1810$</td>
<td>$1620$</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{IN} = V_{IH}$ Max</td>
<td>10KH</td>
<td>$0^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$220$</td>
<td>$220$</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{IN} = V_{IH}$ Min</td>
<td>10KH</td>
<td>$0^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$1950$</td>
<td>$1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$0.5$</td>
<td>$0.5$</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Supply Current</td>
<td>$V_{EE} = Min$ All Inputs and Outputs Open</td>
<td>10KH</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-220$</td>
<td>$-220$</td>
</tr>
</tbody>
</table>

Note: Operating temperatures for circuits in PLCC packages are specified as ambient temperatures ($TA$) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
Switching Characteristics
Over Recommended Operating Conditions, Output load: \( R_L = 50 \Omega \to -2.0V \), \( C_L = 5 \text{ pF} \) to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured Test Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Input to Output</td>
<td>Measured at Threshold Points (Note 1)</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Output Rise Time</td>
<td>Measured between 20% and 80% Points</td>
<td>0.25</td>
<td>1.25</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Fall Time</td>
<td></td>
<td>0.25</td>
<td>1.25</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: All AC Measurements are to be made from Threshold Point.

\[ V_{IH} = \text{Threshold} + 400 \text{ mV} \]
\[ V_{IL} = \text{Threshold} - 400 \text{ mV} \]

\[ \text{Threshold} = \frac{V_{IH_{Min}} + V_{IL_{Max}}}{2} \]

<table>
<thead>
<tr>
<th>Part</th>
<th>Temp</th>
<th>( V_{IH_{Min}} )</th>
<th>( V_{IH_{Max}} )</th>
<th>Threshold</th>
<th>( V_{IH} )</th>
<th>( V_{IL} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kH</td>
<td>0°C</td>
<td>-1170</td>
<td>-1480</td>
<td>-1325</td>
<td>-925</td>
<td>-1725</td>
</tr>
<tr>
<td>10 kH</td>
<td>25°C</td>
<td>-1130</td>
<td>-1480</td>
<td>-1300</td>
<td>-900</td>
<td>-1700</td>
</tr>
<tr>
<td>10 kH</td>
<td>75°C</td>
<td>-1070</td>
<td>-1450</td>
<td>-1260</td>
<td>-860</td>
<td>-1660</td>
</tr>
<tr>
<td>100k</td>
<td>All</td>
<td>-1165</td>
<td>-1475</td>
<td>-1300</td>
<td>-900</td>
<td>-1700</td>
</tr>
</tbody>
</table>

Timing Measurements

Connection Diagram

Test Load

Top View

Order Number PAL1016PE8-3/PAL10016PE8-3
See NS Package Number V28A

TL/L/10712-3

TL/L/10712-4

2-244
Functional Testing
As with all field-programmable devices, the user of the ECL PAL devices provides the final manufacturing step. While National’s PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user’s pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that devices be functionally tested before being installed in your system. Even though the number of postprogramming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor’s Application Note #351 and the Programmable Logic Design Guide.

Design Development Support
A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible “fuse maps”. The industry-standard JEDEC format ensures that the resulting fuse-map files can be downloaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL10/10016PE8-3 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Programmer Support
Advin Systems Sailor PAL V8.40
Data I/O Unisite 40 V2.7
International Microsystems ECL-2, ECL-1
Logical Devices Allpro V1.48C
Stag Microsystems ZL30A V31

Programming
Most programmers listed below are able to directly program the 28-lead PLCC package. If programming from a DIP socket the following adapter wiring is required:

<table>
<thead>
<tr>
<th>PLCC Pin</th>
<th>DIP Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No Connect</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>10</td>
<td>No Connect</td>
</tr>
<tr>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>13</td>
<td>11</td>
</tr>
<tr>
<td>14</td>
<td>12</td>
</tr>
<tr>
<td>15</td>
<td>No Connect</td>
</tr>
<tr>
<td>16</td>
<td>13</td>
</tr>
<tr>
<td>17</td>
<td>14</td>
</tr>
<tr>
<td>18</td>
<td>15</td>
</tr>
<tr>
<td>19</td>
<td>16</td>
</tr>
<tr>
<td>20</td>
<td>No Connect</td>
</tr>
<tr>
<td>21</td>
<td>17</td>
</tr>
<tr>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td>23</td>
<td>19</td>
</tr>
<tr>
<td>24</td>
<td>20</td>
</tr>
<tr>
<td>25</td>
<td>21</td>
</tr>
<tr>
<td>26</td>
<td>22</td>
</tr>
<tr>
<td>27</td>
<td>23</td>
</tr>
<tr>
<td>28</td>
<td>24</td>
</tr>
</tbody>
</table>

PLCC pins 1, 10, 15 and 20 are not connected to the DIP pins because these are the additional ECL inputs. If using such an adaptor, a 0.1 µF capacitor should be added from PLCC pin 23 to PLCC pin 14.
Logic Diagram—PAL1016PE8-3/PAL10016PE8-3

JEDEC logic array cell number = product line first cell number + input line number

2-246
PAL10/10016P4A
4 ns ECL Programmable Array Logic

General Description
The PAL1016P4A and PAL10016P4A are members of the National Semiconductor ECl PAL® family. The PAL10/10016P4A is a functional subset of the PAL10/10016P8 (6 ns tpd) and is compatible in pinout, JEDEC map format, and programming algorithm. The ECL PAL family utilizes National Semiconductor's advanced oxide-isolated process and proven Titanium-Tungsten (Ti-W) fuse technology to provide user-programmable logic to replace conventional ECl SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1. This family allows the systems engineer to customize his chip by opening fuse links to configure AND and OR gates to perform his desired logic function. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can easily be modified during prototype checkout or production. The PAL transfer function is the familiar sum-of-products implemented with a single array of fusible links. The PAL device incorporates a programmable AND array driving a fixed OR array. The AND term logic matrix incorporates 16 complementary inputs and 32 product terms. The 32 product terms are grouped into four OR functions with eight product terms each. All devices in this series are provided with output polarity fuses. These fuses permit the designer to configure each output independently to provide either a logic true (by leaving the fuse intact) or a logic false (by programming the fuse) when the equation defining that output is satisfied. Product terms with all fuses programmed assume a logical high state, while product terms connected to both the true and complement of any input assume a logical low state. All product terms in an unprogrammed part are logically low. Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams for logic editing. These ECl PAL devices may be programmed on many PLD programmers. Programming is accomplished using TTL voltage levels. Once programmed and verified, an additional fuse may be programmed to disable further verification. This feature gives the user a proprietary circuit which is difficult to copy.

Features
- High speed: Combinatorial outputs
tpd = 4 ns max
- Both 10 KH and 100K I/O compatible versions
- Four output functions; sixteen dedicated inputs
- Individually programmable polarity for all logic outputs
- Reliable titanium-tungsten fuses
- Security fuse to prevent direct copying
- Programmed on many PLD programmers
- Fully Supported by PLANTM Software
- Packaging:
  24-pin thin DIP (0.300")
  24-pin QUAD CERPAK

Applications
- Programmable replacement for ECL logic
- Address or instruction decoding

Ordering Information
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

```
Programmable Array Logic Family
ECL I/O Compatible
10 = 10 KH
100 = 100k
Number of Array Inputs
Output Type
P = Combinatorial with Programmable Polarity
Number of Outputs
Speed Range
No Symbol = Standard Speed (6 ns)
A = High Speed (4 ns)
Package
J = Ceramic DIP
W = Quad Cerpack
Temperature Range
C = 0°C to +75°C for 10 KH
0°C to +85°C for 100k
```
Absolute Maximum Ratings
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Lead Temperature (Soldering, 10 seconds) 300°C
- ESD Tolerance 1000V
- C ZAP = 100 pF
- R ZAP = 1500Ω
- Test Method: Human Body Model
- Test Specification: NSC SOP-5-028

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>TA</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEE</td>
<td>Supply Voltage</td>
<td>Guaranteed Input Voltage High For All Inputs</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1170</td>
<td>-840 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1165</td>
<td>-880 mV</td>
</tr>
<tr>
<td>T</td>
<td>Operating Temperature (Note)</td>
<td>Guaranteed Input Voltage Low For All Inputs</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1950</td>
<td>-1480 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1950</td>
<td>-1480 mV</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics Over Recommended Operating Conditions
Output Load = 50Ω to -2.0V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>TA</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td>Guaranteed Input Voltage High For All Inputs</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1020</td>
<td>-840 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1025</td>
<td>-880 mV</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed Input Voltage Low For All Inputs</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1950</td>
<td>-1630 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1950</td>
<td>-1630 mV</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>V IN = VIH Max. or VIL Min.</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1020</td>
<td>-840 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1025</td>
<td>-880 mV</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>V IN = VIH Max. or VIL Min.</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1950</td>
<td>-1620 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1950</td>
<td>-1620 mV</td>
</tr>
<tr>
<td>IH</td>
<td>High Level Input Current</td>
<td>V IN = VIH Max.</td>
<td>10 KH</td>
<td>0°C</td>
<td>220 μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>220 μA</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Low Level Input Current</td>
<td>V IN = VIL Min.</td>
<td>10 KH</td>
<td>0°C</td>
<td>0.5 μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>0.5 μA</td>
<td></td>
</tr>
<tr>
<td>IEE</td>
<td>Supply Current</td>
<td>VEE = Min.</td>
<td>10 KH</td>
<td>0°C to +85°C</td>
<td>-220 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All Inputs and Outputs Open</td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-220 mA</td>
<td></td>
</tr>
</tbody>
</table>

Note: Operating temperatures for circuits in Dual-In-Line packages are specified as ambient temperatures (T A) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Operating temperatures for circuits packaged in QUAD CERPAK are specified as case temperatures (T O). All specifications apply after thermal equilibrium has been established.
Switching Characteristics
Over Recommended Operating Conditions, Output load: $R_L = 50 \Omega$ to $-2.0V$, $C_L = 5 \text{ pF}$ to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured Test Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD}$</td>
<td>Input to Output</td>
<td>Measured at threshold points (Note 1)</td>
<td>4</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Output Rise Time</td>
<td>Measured between 20% and 80% points</td>
<td>0.5</td>
<td>2.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Output Fall Time</td>
<td></td>
<td>0.5</td>
<td>2.5</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** All AC measurements are to be made from threshold point.

\[ V_{IH} = \text{Threshold} + 400 \text{ mV} \]

\[ V_{IL} = \text{Threshold} - 400 \text{ mV} \]

\[ \text{Threshold} = \frac{V_{IH\text{Min}} + V_{IL\text{Max}}}{2} \]

### Timing Measurements

![Timing Diagram](image)

**Connection Diagram**

![Connection Diagram](image)
**Functional Testing**

As with all field-programmable devices, the user of the ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that devices be functionally tested before being installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. Refer to National Semiconductor's Application Note #351 and the Programmable Logic Design Guide for more information about the functional testing of PAL devices.

Please contact your local sales office for a list of current programming support tools for ECL PAL devices.
PAL10/10016P4-2 (DIP Only)
2 ns ECL ASPECT™ Programmable Array Logic

General Description
The PAL10/10016P4-2 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor’s ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016P4-2 logic array has a total of 16 complementary input pairs, 32 product terms and 4 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features
- Highest speed: \( t_{PD} = 2.5 \text{ ns max} \)
- Programmable replacement for ECL logic
- Both 100K and 10 KH I/O compatible versions
- Four output functions with programmable polarity
- Improved programmability tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- Commercial and Military ranges

Block Diagram PAL10/10016P4-2
Absolute Maximum Ratings
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Output Current -50 mA
Lead Temperature (Soldering, 10 seconds) 300°C
ESD Tolerance TBD

Temperature Under Bias -55°C to +125°C
Storage Temperature Range -65°C to +150°C

V_{EE} Relative to V_{CC} -7V to +0.5V
Input Voltage V_{EE} to +0.5V

Recommended Operating Conditions for Commercial Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{EE}</td>
<td>Supply Voltage</td>
<td>10 KH</td>
<td>-5.46</td>
<td>-5.2</td>
<td>-4.94 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>-4.80</td>
<td>-4.5</td>
<td>-4.20</td>
</tr>
<tr>
<td>T</td>
<td>Operating Temperature (Note)</td>
<td>10 KH</td>
<td>0</td>
<td>+75</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0</td>
<td>+85</td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics Over Recommended Operating Conditions
Output Load = 50Ω to -2.0V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>( T_A )</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH}</td>
<td>High Level Input Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1170</td>
<td>-840 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High For All Inputs</td>
<td></td>
<td>+25°C</td>
<td>-1130</td>
<td>-810 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-1070</td>
<td>-735 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1165</td>
<td>-880 mV</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1950</td>
<td>-1480 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low For All Inputs</td>
<td></td>
<td>+25°C</td>
<td>-1950</td>
<td>-1480 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-1950</td>
<td>-1450 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1810</td>
<td>-1475 mV</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>High Level Output Voltage</td>
<td>( V_{IN} = V_{IH} ) Max. or ( V_{IL} ) Min.</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1020</td>
<td>-840 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-980</td>
<td>-810 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-920</td>
<td>-735 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1025</td>
<td>-880 mV</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Low Level Output Voltage</td>
<td>( V_{IN} = V_{IH} ) Max. or ( V_{IL} ) Min.</td>
<td>10 KH</td>
<td>0°C</td>
<td>-1950</td>
<td>-1630 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-1950</td>
<td>-1630 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+75°C</td>
<td>-1950</td>
<td>-1600 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1810</td>
<td>-1620 mV</td>
<td></td>
</tr>
<tr>
<td>I_{IH}</td>
<td>High Level Input Current</td>
<td>( V_{IN} = V_{IH} ) Max.</td>
<td>10 KH</td>
<td>0°C to +75°C</td>
<td>220 µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Low Level Input Current</td>
<td>( V_{IN} = V_{IL} ) Min.</td>
<td>10 KH</td>
<td>0°C to +75°C</td>
<td>0.5 µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{EE}</td>
<td>Supply Current</td>
<td>( V_{EE} = ) Min. All Inputs and Outputs Open</td>
<td>10 KH</td>
<td>0°C to +75°C</td>
<td>-220 mA</td>
<td></td>
</tr>
</tbody>
</table>

Note: Operating temperatures for circuits in N and J packages are specified as ambient temperatures \( T_A \) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
**Absolute Maximum Ratings**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Output Current**: 
  - Military/Aerospace: 50 mA

- **Lead Temperature (Soldering, 10 seconds)**: 300°C

- **ESD Tolerance**: TBD

- **CZAP**: 100 pF

- **RZAP**: 150 kΩ

- **Test Method**: Human Body Model

- **Test Specification**: NSC SOP-5-028

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**Recommended Operating Conditions for Extended (Military) Range**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEE</td>
<td>Supply Voltage</td>
<td></td>
<td>10 K</td>
<td>-5.46</td>
<td>-5.2</td>
<td>-4.94</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>-4.80</td>
<td>-4.5</td>
<td>-4.20</td>
</tr>
<tr>
<td>T</td>
<td>Operating Temperature</td>
<td></td>
<td>10 K</td>
<td>-55</td>
<td></td>
<td>+125</td>
</tr>
<tr>
<td></td>
<td>(Note)</td>
<td></td>
<td>100K</td>
<td>0</td>
<td></td>
<td>+125</td>
</tr>
</tbody>
</table>

---

**Electrical Characteristics** Over Recommended Operating Conditions

- **Output Load**: 50Ω to -2.0V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>TA Min</th>
<th>TA Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High Level Input Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>-55°C</td>
<td>-1250</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High For All Inputs</td>
<td>+25°C</td>
<td>-930</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+125°C</td>
<td>10°C</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>-1165</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0°C to +125°C</td>
<td>-880</td>
<td>mV</td>
</tr>
<tr>
<td>VIL</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>-55°C</td>
<td>-1950</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low For All Inputs</td>
<td>+25°C</td>
<td>-1480</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+125°C</td>
<td>-1480</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>-1420</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0°C to +125°C</td>
<td>-1475</td>
<td>mV</td>
</tr>
<tr>
<td>VOH</td>
<td>High Level Output Voltage</td>
<td>VIN = VIH Max. or VIL Min.</td>
<td>-55°C</td>
<td>-1110</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-930</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+125°C</td>
<td>-810</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>-830</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0°C to +125°C</td>
<td>-660</td>
<td>mV</td>
</tr>
<tr>
<td>VOL</td>
<td>Low Level Output Voltage</td>
<td>VIN = VIH Max. or VIL Min.</td>
<td>-55°C</td>
<td>-1950</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-1630</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+125°C</td>
<td>-1630</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>-1570</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0°C to +125°C</td>
<td>-1620</td>
<td>mV</td>
</tr>
<tr>
<td>IIH</td>
<td>High Level Input Current</td>
<td>VIN = VIH Max.</td>
<td>-55°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0°C to +125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Low Level Input Current</td>
<td>VIN = VIL Min.</td>
<td>-55°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0°C to +125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IEE</td>
<td>Supply Current</td>
<td>VIN = Min.</td>
<td>-55°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All Inputs and Outputs Open</td>
<td>+125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>-220</td>
<td></td>
</tr>
</tbody>
</table>

Note: Operating temperatures for circuits in J and N packages are specified as ambient temperatures (T_A) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

*Note: Extended (Military) Range available in J package only.*
Switching Characteristics
Over Recommended Operating Conditions, Output load: \( R_L = 50\Omega \) to \(-2.0V\), \( C_L = 5 \) pF to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured Test Conditions</th>
<th>Commerical</th>
<th>Military</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>( t_{PD} )</td>
<td>Input to Output</td>
<td>Measured at Threshold Points (Note 1)</td>
<td>2.5</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>( t_r )</td>
<td>Output Rise Time</td>
<td>Measured between 20% and 80% points</td>
<td>0.25</td>
<td>1.25</td>
<td>0.25</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Fall Time</td>
<td></td>
<td>0.25</td>
<td>1.25</td>
<td>0.25</td>
</tr>
</tbody>
</table>

Note 1: All AC Measurements are to be made from Threshold Point.

\[ V_{IH} = \text{Threshold} + 400 \text{ mV} \]
\[ V_{IL} = \text{Threshold} - 400 \text{ mV} \]
\[ \text{Threshold} = \frac{V_{IH_{\text{Min}}} + V_{IL_{\text{Max}}}}{2} \]

Timing Measurements

Test Load

Connection Diagram
Functional Testing
As with all field-programmable devices, the user of the ECL PAL devices provides the final manufacturing step. While National’s PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user’s pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that devices be functionally tested before being installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor’s Application Note #351 and the Programmable Logic Design Guide.

Design Development Support
A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible “fuse maps”. The industry-standard JEDEC format ensures that the resulting fuse-map files can be downloaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer’s Boolean logic equations.

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL10/10016P4-2 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Programmer Support

<table>
<thead>
<tr>
<th>Software Tool</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advin Systems</td>
<td>V8.40</td>
</tr>
<tr>
<td>Data I/O</td>
<td>V2.20</td>
</tr>
<tr>
<td>Digielec</td>
<td>VA-3.2</td>
</tr>
<tr>
<td>International Microsystems</td>
<td>V1.44C</td>
</tr>
<tr>
<td>Logical Devices</td>
<td>V4.0</td>
</tr>
<tr>
<td>SMS</td>
<td>V31</td>
</tr>
<tr>
<td>Stag Microsystems</td>
<td>V32.J</td>
</tr>
<tr>
<td>Sprint Plus</td>
<td></td>
</tr>
</tbody>
</table>

Ordering Information

- **Programmable Array Logic Family**
- **ECL I/O Compatibility:**
  - 10 = ECL 10 KH
  - 100 = ECL 100K
- **Number of Array Inputs**
- **Output Type:**
  - C = Complementary
  - P = Programmable Polarity
- **Number of Outputs**
- **Speed Version:** - 2 = 2.5 ns tP
- **Packaging:**
  - N = 24-Pin Plastic DIP
  - J = 24-Pin Ceramic DIP
  *Note: For PLCC see PAL10/10016C4-2 datasheet
- **Temperature Range:**
  - C = Commercial:
    - 0°C to +75°C for 10 KH
    - 0°C to +85°C for 100K
  - M = Extended (Military):
    - -55°C to +125°C for 10 KH
    - 0°C to +125°C for 100K
JEDEC logic array cell number = product line first cell number + input line number
PAL10/10016C4-2 (PLCC Only)
2 ns ECL ASPECT™ Programmable Array Logic

General Description
The PAL10/10016C4-2 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly ECL Technology) Process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016C4-2 logic array has a total of 16 complementary input pairs, 32 product terms and 4 complementary output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state. Complementary outputs eliminate the need for external inverters and allow for more convenient output OR-tying. They are also suitable for differential sensing for increased noise immunity. All input pins have on-chip 50 kΩ pull-down resistors.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by several conventional TTL PLD programming units. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features
- Highest speed: tPD = 2 ns max
- Full 28-pin function
- Programmable replacement for ECL logic
- Both 100K and 10 KH I/O compatible versions
- Four output functions with complementary outputs
- Improved programmability tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- High density-High performance 28-pin PLCC package

Ordering Information

<table>
<thead>
<tr>
<th>PAL</th>
<th>100</th>
<th>16</th>
<th>C</th>
<th>4</th>
<th>-2</th>
<th>V</th>
<th>C</th>
</tr>
</thead>
</table>

Programmable Array Logic Family
ECL I/O Compatibility:
10 = ECL 10 KH
100 = ECL 100K

Number of Array Inputs

Output Type:
C = Complementary
P = Programmable Polarity

Number of Outputs

Speed Version: -2 = 2 ns tPD

Packaging: V = 28-Pin PLCC
* Note: For DIP see PAL10/10016 P4-2 datasheet.

Temperature Range:
C = Commercial:
0°C to + 75°C for 10 KH
0°C to + 85°C for 100K

Block Diagram

V_{EE} = 14, V_{CC} = 28, V_{CCD} (5, 6, 8, 9) = 7
V_{CCD} (21, 22, 24, 25) = 23
Pinout applies to 28-pin PLCC
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<tbody>
<tr>
<td>Temperature Under Bias</td>
<td>-55°C</td>
<td>+125°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C</td>
<td>+150°C</td>
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<tr>
<td>V_{EE} Relative to V_{CC}</td>
<td>-7V</td>
<td>+0.5V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>V_{EE}</td>
<td>+0.5V</td>
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</tr>
<tr>
<td>Output Current</td>
<td>-50mA</td>
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<tr>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>300°C</td>
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</tr>
<tr>
<td>ESD Tolerance</td>
<td>TBD</td>
<td></td>
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</tr>
<tr>
<td>C_{ZAP}</td>
<td>100 pF</td>
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</tr>
<tr>
<td>R_{ZAP}</td>
<td>1500Ω</td>
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<td>Test Method: Human Body Model</td>
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<td>Test Specification: NSC SOP-5-028</td>
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Recommended Operating Conditions

<table>
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<tbody>
<tr>
<td>V_{EE}</td>
<td>Supply Voltage</td>
<td>-5.46</td>
<td>-5.2</td>
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<td>V</td>
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<tr>
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<td>10 KH</td>
<td>-4.80</td>
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<td>100K</td>
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<tr>
<td>T</td>
<td>Operating Temperature (Note)</td>
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<td>°C</td>
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Electrical Characteristics

Over Recommended Operating Conditions

Output Load = 50Ω to -2.0V

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<thead>
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<th>TA</th>
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<tr>
<td>V_{IH}</td>
<td>High Level Input Voltage</td>
<td>Guaranteed Input Voltage High For All Inputs</td>
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<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>10 KH</td>
<td>0°C</td>
<td>-1170</td>
<td>-840</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+25°C</td>
<td>-1130</td>
<td>-810</td>
<td></td>
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<td></td>
<td></td>
<td>+75°C</td>
<td>-1070</td>
<td>-735</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1165</td>
<td>-880</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed Input Voltage Low For All Inputs</td>
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<td>-1950</td>
<td>-1480</td>
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<td></td>
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<td>+25°C</td>
<td>-1950</td>
<td>-1480</td>
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<td>-1950</td>
<td>-1450</td>
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<td>0°C to +85°C</td>
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<td>-1475</td>
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<td>V_{OH}</td>
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<td>V_{IN} = V_{IH} Max. or V_{IL} Min.</td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td>10 KH</td>
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<td>+25°C</td>
<td>-980</td>
<td>-810</td>
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<td>+75°C</td>
<td>-920</td>
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<td>-880</td>
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<td>V_{OL}</td>
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<td>0°C</td>
<td>-1950</td>
<td>-1630</td>
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<td>+25°C</td>
<td>-1950</td>
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</tr>
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<td>+75°C</td>
<td>-1950</td>
<td>-1600</td>
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<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
<td>-1810</td>
<td>-1620</td>
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<tr>
<td>I_{IH}</td>
<td>High Level Input Current</td>
<td>V_{IN} = V_{IH} Max.</td>
<td></td>
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<td>μA</td>
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<td></td>
<td>10 KH</td>
<td>0°C to +75°C</td>
<td>220</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>0°C to +85°C</td>
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</tr>
<tr>
<td>I_{IL}</td>
<td>Low Level Input Current</td>
<td>V_{IN} = V_{IL} Min.</td>
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<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 KH</td>
<td>0°C to +75°C</td>
<td>0.5</td>
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<td>100K</td>
<td>0°C to +85°C</td>
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<td>I_{EE}</td>
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<td>V_{EE} = Min.</td>
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<td>-220</td>
<td>mA</td>
</tr>
<tr>
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<td></td>
<td>All Inputs and Outputs Open</td>
<td>10 KH</td>
<td>0°C to +75°C</td>
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</tr>
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<td>100K</td>
<td>0°C to +85°C</td>
<td></td>
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</tr>
</tbody>
</table>

Note: Operating temperatures for circuits in PLCC packages are specified as ambient temperatures (T_A) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
Switching Characteristics
Over Recommended Operating Conditions, Output load: \( R_L = 50\,\Omega \) to \(-2\,\text{V}\), \( C_L = 5\,\text{pF} \) to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured Test Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
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<tr>
<td>( t_{PD} )</td>
<td>Input to Output</td>
<td>Measured at 50% points</td>
<td>2.0</td>
<td>ns</td>
<td></td>
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<tr>
<td>( t_{r} )</td>
<td>Output Rise Time</td>
<td>Measured between 20% and 80% points</td>
<td>0.25</td>
<td>1.25</td>
<td>ns</td>
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<tr>
<td>( t_{f} )</td>
<td>Output Fall Time</td>
<td></td>
<td>0.25</td>
<td>1.25</td>
<td>ns</td>
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</table>

Timing Measurements

Test Load

Connection Diagram

Order Number PAL1016C4-2/PAL10016C4-2
See NS Package Number V28A
Functional Testing
As with all field-programmable devices, the user of the ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that devices be functionally tested before being installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor's Application Note #351 and the Programmable Logic Design Guide.

Design Development Support
A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be downloaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL10/10016C4-2 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.
JEDEC logic array cell number = product line first cell number + input line number
General Description

The registered ECL PAL10/10016RD8 is offered in 10KH or 100K compatible versions. A maximum propagation delay of 6 ns (input to output) characterizes the performance of this ECL PAL® series. The ECL PAL family utilizes National Semiconductor's advanced oxide-isolated process and proven Titanium Tungsten (Ti-W) fuse technology to provide user-programmable logic to replace conventional ECL SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1.

This family allows the system engineer to customize the chip by opening fuse links to configure AND and OR gates to perform the desired logic function. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can easily be modified during prototype checkout or production.

The PAL transfer function is the familiar sum-of-products implemented with a single array of fusible links. The PAL device incorporates a programmable AND array driving a fixed OR array. The AND term logic matrix incorporates 16 complementary inputs and 64 product terms. The 64 product terms are grouped into eight OR functions with eight product terms each. All devices in this family are provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied. In addition, the ECL PAL family offers these options:

- Output registers
- Dual (split) clocks

Product terms with all fuses programmed assume a logical high state, while product terms connected to both the true and complement of any input assume a logical low state. All product terms in an unprogrammed part are logically low. All input and I/O pins have on-chip 50 kΩ pull-down resistors. Registers consist of D-type flip-flops which are loaded in response to the low-to-high transition of the clock input(s).

Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams for logic editing.

These ECL PAL devices may be programmed on several TTL PLD programmers. Programming is accomplished with TTL voltage levels. Once the PAL is programmed and verified, an additional security fuse may be programmed to defeat verification. This feature gives the user a proprietary circuit which is difficult to copy.

Features

- High speed:
  - Combinatorial outputs
    \[ \text{tpd} = 6 \text{ ns max} \]
  - Registered outputs
    \[ \text{tsu} = 5 \text{ ns min} \]
    \[ \text{t\textsubscript{Clk}} = 3.5 \text{ ns max} \]
    \[ f\text{max} = 117 \text{ MHz max} \]
- Both 10 KH and 100K I/O compatible versions
- Eight output functions with feedback; eight dedicated inputs
- Eight registered outputs
- Individually programmable polarity on all logic outputs
- Output enable gate on all registered outputs
- Reliable Titanium Tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLANT™ Software
- Packaging:
  - 24-pin thin DIP (0.300"")
  - 24-pin QUAD CERPAK

Applications

- Programmable replacement for ECL logic
- Programmable state machine
- Address or instruction decoding
### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Temperature Under Bias (Ambient): -55°C to +125°C
- Storage Temperature Range: -65°C to +150°C
- $V_{EE}$ Relative to $V_{CC}$: -7V to +0.5V
- Input Voltage: $V_{EE}$ to +0.5V

#### Output Current
- $-50 \text{ mA}$

#### Lead Temperature (Soldering, 10 seconds)
- 300°C

#### ESD Tolerance
- 1000V

#### C$_{ZAP}$
- 100 pF

#### R$_{ZAP}$
- 1500Ω

#### Test Method: Human Body Model

#### Test Specification: NSC SOP-5-028

### Electrical Characteristics

**Over Recommended Operating Conditions (Note 1)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Conditions</th>
<th>$T_A$</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage Guaranteed Input Voltage High For All Inputs</td>
<td>10 KH</td>
<td>$0°C$</td>
<td>$-1170$</td>
<td>$-840$</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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<td>$+25°C$</td>
<td>$-1130$</td>
<td>$-810$</td>
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<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0°C$ to $+85°C$</td>
<td>$-1165$</td>
<td>$-880$</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage Guaranteed Input Voltage Low For All Inputs</td>
<td>10 KH</td>
<td>$0°C$</td>
<td>$-1020$</td>
<td>$-840$</td>
<td>mV</td>
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</tr>
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<td></td>
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<td>$+25°C$</td>
<td>$-980$</td>
<td>$-810$</td>
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<td></td>
<td></td>
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<td>$+75°C$</td>
<td>$-920$</td>
<td>$-735$</td>
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<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0°C$ to $+85°C$</td>
<td>$-1025$</td>
<td>$-880$</td>
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</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage $V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.</td>
<td>10 KH</td>
<td>$0°C$</td>
<td>$-1020$</td>
<td>$-840$</td>
<td>mV</td>
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<td></td>
<td></td>
<td>$+25°C$</td>
<td>$-980$</td>
<td>$-810$</td>
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<td></td>
<td></td>
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<td>$+75°C$</td>
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<td>$-735$</td>
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<td>100K</td>
<td>$0°C$ to $+85°C$</td>
<td>$-1025$</td>
<td>$-880$</td>
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</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage $V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.</td>
<td>10 KH</td>
<td>$0°C$</td>
<td>$-1950$</td>
<td>$-1630$</td>
<td>mV</td>
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<td>$+25°C$</td>
<td>$-1950$</td>
<td>$-1630$</td>
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<td>$-1630$</td>
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<td>100K</td>
<td>$0°C$ to $+85°C$</td>
<td>$-1810$</td>
<td>$-1620$</td>
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<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current (Note 3) $V_{IN} = V_{IH}$ Max.</td>
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<td>100K</td>
<td>$0°C$ to $+85°C$</td>
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</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current $V_{IN} = V_{IL}$ Min. Except I/O Pins</td>
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<td>$0°C$</td>
<td>$0.5$</td>
<td></td>
<td>μA</td>
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<td>$+75°C$</td>
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<td>100K</td>
<td>$0°C$ to $+85°C$</td>
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<td>$I_{EE}$</td>
<td>Supply Current $V_{EE} = Min.$ All Inputs and Outputs Open</td>
<td>LD8, LD4, RD4, RC4</td>
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<td>mA</td>
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<td>RD8, RC8</td>
<td>$-280$</td>
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### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>$V_{EE}$</td>
<td>Supply Voltage</td>
<td>10 KH</td>
<td>$-5.46$</td>
<td>$-5.2$</td>
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<td>100K</td>
<td>$-4.73$</td>
<td>$-4.5$</td>
<td>$-4.27$</td>
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<tr>
<td>$T$</td>
<td>Operating Temperature (Note 2)</td>
<td>10 KH</td>
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<td>°C</td>
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<td>100K</td>
<td>0</td>
<td>$+85$</td>
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<td>$R_L$</td>
<td>Standard 10 KH/100K Load</td>
<td>10 KH</td>
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<td></td>
<td>Ω</td>
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<td></td>
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<td>50</td>
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<td>$C_L$</td>
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</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time of Input or Feedback</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{H}$</td>
<td>Input Hold Time</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{W}$</td>
<td>Clock or Enable Pulse Width</td>
<td>4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WMR}$</td>
<td>Master Reset Pulse Width</td>
<td>4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** This product family has been designed to meet the specification in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

**Note 2:** Operating temperatures for circuits in Dual-In-Line packages are specified as ambient temperatures ($T_A$) with circuits mounted in socket or printed circuit board and transverse airflow exceeding 500 linear feet per minute. Operating temperatures for circuits packaged in QUAD CERPAK are specified as case temperatures ($T_C$).

**Note 3:** Except for clock inputs (350 μA) and MR (1 mA).
Ordering Information

- Programmable Array Logic Family
- ECL I/O Compatibility
  - 10 = 10 KH
  - 100 = 100K
- Number of Array Inputs
- Output Type
  - RD = Registered w/Dual Clocks
- Number of Registered Outputs
- Package
  - J = Ceramic DIP
  - W = Quad Cerpak
- Temperature Range
  - C = Commercial: 0°C to +75°C for 10 KH, 0°C to +85°C for 100K

Switching Characteristics

Over Recommended Operating Conditions
Output Load: \( R_L = 50\, \Omega \) to \(-2.0\, \text{V}\), \( C_L = 5\, \text{pF} \) to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured From</th>
<th>Measured To</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{CLK}} ) (Note 1)</td>
<td>Clock to Output or Feedback</td>
<td>( C_n \uparrow )</td>
<td>( Q )</td>
<td>3.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{PD}} ) (Note 2)</td>
<td>Input or Feedback to Output</td>
<td>( I )</td>
<td>( Q ) or I/O</td>
<td>6</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{PLH}} ) (Note 1)</td>
<td>Output Enable</td>
<td>( \overline{G} \downarrow )</td>
<td>( Q \uparrow )</td>
<td>4.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{PHL}} ) (Note 1)</td>
<td>Output Disable</td>
<td>( \overline{G} \uparrow )</td>
<td>( Q \downarrow )</td>
<td>4.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{MR}} ) (Note 1)</td>
<td>Master Reset to Output</td>
<td>MR ( \uparrow )</td>
<td>( Q \downarrow )</td>
<td>5.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( f_{\text{MAX}} ) (Notes 1, 3)</td>
<td>Maximum Frequency</td>
<td></td>
<td></td>
<td>117</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( t_r )</td>
<td>Output Rise Time</td>
<td>Measured Between</td>
<td></td>
<td>0.5</td>
<td>2.5</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Fall Time</td>
<td>( 20% ) and ( 80% ) points</td>
<td></td>
<td>0.5</td>
<td>2.5</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: Applies to registered outputs.
Note 2: Applies to combinatorial outputs.
Note 3: \( f_{\text{MAX}} = (t_{\text{SU}} + t_{\text{CLK}})^{-1} \)

Test Load

![Test Load Diagram]
Timing Waveform—All Registered Outputs

Connection Diagram

24-Pin Dual-In-Line Package

PAL1016RD8/PAL10016RD8

Pin Descriptions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Eight dedicated inputs to logic array.</td>
</tr>
<tr>
<td>Q</td>
<td>Eight outputs from registered logic functions.</td>
</tr>
<tr>
<td>C1</td>
<td>Clock input for registers on output pins* 4, 5, 7 and 8 on dual-clock devices; Data is written into registers on rising edge of clock.</td>
</tr>
<tr>
<td>C2</td>
<td>Clock input for registers on output pins* 17, 18, 20 and 21 on dual-clock devices; Data is written into registers on rising edge of clock.</td>
</tr>
<tr>
<td>MR</td>
<td>Master Reset input. Asynchronously resets all registers to the low state while MR is high (overrides clock).</td>
</tr>
<tr>
<td>G</td>
<td>Output enable input. Enables output drivers while G is low; forces all registered output drivers to the low state as long as G is high. Register contents and feedbacks are not affected. Combinatorial outputs are not affected.</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply voltage.</td>
</tr>
<tr>
<td>VEE</td>
<td>Ground for internal circuitry.</td>
</tr>
<tr>
<td>VCCO</td>
<td>Ground for output drivers (4 outputs per VCCO).</td>
</tr>
</tbody>
</table>

*Corresponds to DIP pinout
Logic Diagram PAL1016RD8/PAL10016RD8

JEDEC logic array cell number = product line first cell number + input line number.
Functional Testing
As with all field-programmable devices, the user of ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.
To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that PAL devices be functionally tested before they are installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. Refer to National Semiconductor's Application Note #351 and the Programmable Logic Design Guide for more information about the functional testing of PAL devices.
For a list of current programming support tools for ECL PAL devices, please contact your local National Semiconductor sales office.
National Semiconductor

PAL10/10016RM4A
ECL Registered Programmable Array Logic

General Description
The PAL10/10016RM4A is a member of the National Semiconductor ECL PAL® family. The ECL PAL Series-A is characterized by 4 ns maximum propagation delays (combinatorial input-to-output). The pinout, JEDEC fuse-map format and programming algorithm of these devices are compatible with those of all prior ECL PAL products from National. Series-A ECL PAL devices are manufactured using National Semiconductor's advanced oxide-isolated process with proven titanium-tungsten fuse technology to provide high-speed user-programmable replacements for conventional ECL SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016RM logic array has a total of 16 complementary input pairs, 32 product terms and four output functions; each output function is the OR-sum of 8 product terms. The 16RM4A provides an edge-triggered D-type register on each of its four outputs. Registers allow the PAL device to implement sequential logic circuits. Polarity fuses allow each output to be active-high or active-low.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by several conventional TTL PLD programming units. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features
- High speed:
  - $t_{SU} = 3$ ns min
  - $t_{CLK} = 2$ ns max
  - $f_{MAX} = 200$ MHz max (registered)
  - $t_{PD} = 4$ ns max (combinatorial)
- Programmable replacement for ECL SSI/MSI logic
- Both 10 KH and 100K I/O compatible versions
- Four registered output functions with I/O pin feedback; twelve dedicated inputs
- Individually programmable polarity on all logic outputs
- Reliable Titanium Tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLANTM Software
- Packaging:
  - 24-pin thin DIP (0.300")
  - 24-pin Quad Cerpak

Ordering Information
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10 kH</td>
</tr>
<tr>
<td>100</td>
<td>100 K</td>
</tr>
<tr>
<td>RM</td>
<td>Registered with Multiple Clocks</td>
</tr>
<tr>
<td>A</td>
<td>4 ns $t_{PD}$</td>
</tr>
<tr>
<td>J</td>
<td>24-Pin Ceramic DIP</td>
</tr>
<tr>
<td>W</td>
<td>24-Pin Quad Cerpak</td>
</tr>
<tr>
<td>C</td>
<td>Commercial: 0°C to +75°C for 10 kH, 0°C to +85°C for 100K</td>
</tr>
</tbody>
</table>

Block Diagram

![Block Diagram](image_url)

$V_{EE} = 12, V_{CC} = 24, V_{CCO} (5,7) = 6, V_{CCO} (18,20) = 19$
Pinout applies to 24-pin DIP.
Absolute Maximum Ratings
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Temperature Under Bias: $-55^\circ C$ to $+125^\circ C$
- Storage Temperature Range: $-65^\circ C$ to $+150^\circ C$
- $V_{EE}$ Relative to $V_{CC}$: $-7V$ to $+0.5V$

Input Voltage: $V_{EE}$ to $+0.5V$
Output Current: $-50 mA$
Lead Temperature (Soldering, 10 seconds): $300^\circ C$
ESD Tolerance: $1000V$

$C_{ZAP} = 100 \mu F$
$R_{ZAP} = 1500 \Omega$

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{EE}$</td>
<td>Supply Voltage</td>
<td>10 KH</td>
<td>$-5.46$</td>
<td>$-5.2$</td>
<td>$-4.94$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100K</td>
<td>$-4.73$</td>
<td>$-4.5$</td>
<td>$-4.27$</td>
<td></td>
</tr>
<tr>
<td>$T$</td>
<td>Operating Temperature</td>
<td>10 KH</td>
<td>0</td>
<td>+75</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Note)</td>
<td>100K</td>
<td>0</td>
<td>+85</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_L$</td>
<td>Standard 10 KH/100K Load</td>
<td></td>
<td>50</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$C_L$</td>
<td>Standard 10 KH/100K Load</td>
<td></td>
<td>5</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$t_{SU}$</td>
<td>Setup Time of Input or Feedback</td>
<td></td>
<td>3.0</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_H$</td>
<td>Input Hold Time</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_W$</td>
<td>Clock or Enable Pulse Width</td>
<td></td>
<td>2.0</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{WMR}$</td>
<td>Master Reset Pulse Width</td>
<td></td>
<td>2.0</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_A$</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>10 KH</td>
<td>$0^\circ C$</td>
<td>$-170$</td>
<td>$-840$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High For All Inputs</td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-1130$</td>
<td>$-810$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-1070$</td>
<td>$-735$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1165$</td>
<td>$-880$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>Guaranteed Input Voltage</td>
<td>10 KH</td>
<td>$0^\circ C$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low For All Inputs</td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-1950$</td>
<td>$-1480$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-1950$</td>
<td>$-1450$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1810$</td>
<td>$-1475$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.</td>
<td>10 KH</td>
<td>$0^\circ C$</td>
<td>$-1020$</td>
<td>$-840$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-980$</td>
<td>$-810$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-920$</td>
<td>$-735$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1025$</td>
<td>$-880$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.</td>
<td>10 KH</td>
<td>$0^\circ C$</td>
<td>$-1950$</td>
<td>$-1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+25^\circ C$</td>
<td>$-1950$</td>
<td>$-1630$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$+75^\circ C$</td>
<td>$-1950$</td>
<td>$-1600$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100K</td>
<td>$0^\circ C$ to $+85^\circ C$</td>
<td>$-1810$</td>
<td>$-1620$</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{IN} = V_{IH}$ Max.</td>
<td>Inputs, I/Os and MR, Clocks</td>
<td>220</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{IN} = V_{IL}$ Min. Except I/O Pins</td>
<td></td>
<td>0.5</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Supply Current</td>
<td>$V_{EE} = Min.$, All Inputs and Outputs Open</td>
<td></td>
<td>$-240$</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Note: Operating temperatures for circuits in Dual-In-Line packages are specified as ambient temperatures ($T_A$) with circuits mounted in socket or printed circuit board and transverse airflow exceeding 500 linear feet per minute. Operating temperatures for circuits packaged in Quad Cerpak are specified as case temperatures ($T_C$). All specifications apply after thermal equilibrium has been established.
## Switching Characteristics

Over Recommended Operating Conditions

Output Load: \( R_L = 50\,\Omega \) to \(-2.0V\), \( C_L = 5\,pF \) to GND

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Measured</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{CLK}} )</td>
<td>Clock to Output or Feedback</td>
<td>( C_n \uparrow )</td>
<td>I/O</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{PD}} )</td>
<td>Input or Feedback to Output</td>
<td>( I )</td>
<td>I/O</td>
<td>4.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{MR}} )</td>
<td>Master Reset to Output</td>
<td>( \text{MR} \uparrow )</td>
<td>I/O ( \downarrow )</td>
<td>3.5</td>
<td>ns</td>
</tr>
<tr>
<td>( f_{\text{MAX}} ) (Note 1)</td>
<td>Maximum Frequency</td>
<td>Measured Between 20% and 80% points</td>
<td>0.5</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Output Rise Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_f )</td>
<td>Output Fall Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** \( f_{\text{MAX}} = (t_{SU} + t_{CLK})^{-1} \)

---

### Test Load

![Test Load Diagram](TL/L/9772-3)

### Timing Waveform

**PAL10/10016RM4A**

![Timing Waveform Diagram](TL/L/9772-4)
Connection Diagrams

24-Pin Dual-In-Line Package
PAL10/10016RM4A

Pin Descriptions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Twelve dedicated inputs to logic array.</td>
</tr>
<tr>
<td>I/O</td>
<td>Four outputs from registered provides feedback and may be used for additional inputs to logic array.</td>
</tr>
<tr>
<td>C1</td>
<td>Clock input ORed with CC to control registers on output pins* 5 and 7. Data is written into registers on rising edge of clock.</td>
</tr>
<tr>
<td>C2</td>
<td>Clock input ORed with CC to control registers on output pins* 18 and 20. Data is written into registers on rising edge of clock.</td>
</tr>
<tr>
<td>CC</td>
<td>Common Clock input (see C1, C2).</td>
</tr>
<tr>
<td>MR</td>
<td>Master Reset input. Asynchronously resets all registers to the low state while MR is high (overrides clock input).</td>
</tr>
<tr>
<td>VEE</td>
<td>Supply voltage.</td>
</tr>
<tr>
<td>VCC</td>
<td>Ground for internal circuitry.</td>
</tr>
<tr>
<td>VCCO</td>
<td>Ground for output drivers (2 outputs per VCCO). *Corresponds to DIP pinout</td>
</tr>
</tbody>
</table>

Functional Description

The PAL10/10016RM consists of a single programmable AND-gate array with fixed OR-gate connections. The AND array consists of 16 complementary pairs of input lines crossing 32 product-term lines with a programmable fuse at each intersection (1024 fuses). The product terms are organized into four groups of eight each. The eight product terms in each group are connected into an OR-gate to produce the sum-of-products logic function.

An unprogrammed fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term. Programming the fuse removes the connection. A product term is satisfied (logically true) while all the input lines connected to it (via intact fuses) are in the proper logic state. Therefore, if both the true and complement of at least one array input are left connected to a product line, that product term would always be held in the low logic state (which is the state of all product terms in an unprogrammed device).

The four outputs of the PAL10/10016RM pass through D-type registers triggered on the high-going edge of the appropriate clock input. The four registers are separated into two pairs. A separate clock input is provided for each pair. An additional common clock input is ORed with each (see logic diagrams which follow).

The AND-OR logic functions can be optionally inverted before the registers. Polarity inversion is controlled by an individual “polarity fuse” associated with each output function (the original unprogrammed state produces active-high logic functions). Device output pins always indicate active-high register outputs.

The I/O pins used for outputting the registered logic functions also feed back into the logic array as additional inputs. This is useful, for example, to implement sequential circuits with registered parts. Any of these I/O pins may, instead, be used as an additional dedicated input pin. By leaving the associated logic function unprogrammed, the output driver would remain in the low logic state allowing an externally-applied signal to control the array input.

Logic functions requiring more than eight product terms can be implemented conveniently by OR-tying two (or more) device outputs. Partial sums are formed on each of the OR-tied output functions. Each function, however, must be programmed for active-high output polarity, and the associated registers should be controlled by the same clock signal. Each of the array inputs fed back from the OR-tied I/O pins would indicate the correct final logic function. All input and I/O pins have on-chip 50 kΩ pull-down resistors.

Functional Testing

As with all field-programmable devices, the user of ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that PAL devices be functionally tested before they are installed in your system. Even though the number of post-programming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor’s Application Note #351 and the Programmable Logic Design Guide.
Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLANT™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the PAL10/10016RM are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Logic Diagram—PAL1016RM4A/PAL10016RM4A

JEDEC logic array cell number = product line first cell number + input line number.
PART II
DESIGN GUIDE

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Section 3
Designing with Programmable Logic

Programmable logic has evolved over the last decade into a design tool permitting digital logic designs with a minimal number of packages and a maximum of flexibility. The key to PLDs is the use of embedded programmable cells (typically fuse-links) which allow logic components to be configured into specific designs in the field. This permits logic consolidation with quick implementation and equally quick design revision often without board layout changes.

While Programmable Logic Devices (PLDs) do not offer the density of standard VLSI or custom circuits, they are far more flexible than the former and more cost-efficient than the latter. They have found extensive use in varied applications. They are both inexpensive and space-saving in replacing less efficient “glue logic”, which was one of the more popular original uses of PLDs. But they are also capable of efficiently implementing complex functions and state machines.

3.1 Background to PLDs

The use of programmable logic in digital design began with the diode matrix with aluminum fuses at the crosspoints in the early 1960s. This evolved into the PROM through the addition of a decoder at the inputs. The result was an addressable memory which could also be seen as a universal logic device with a fixed AND matrix (the decoder) feeding a programmable OR matrix (the diode array). A representative PROM circuit is shown in Figure 3-1(b) as implementing, for example, a simple set of equations given in Figure 3-1(a). The disadvantage of a PROM used as a logic device derives from its universality. The number of product terms available is 2^n, where n is the number of input variables. Each additional variable (input pin) doubles the size of the matrix. As a result, commercial PROMs offer limited input (i.e. address pins). This approach rapidly degrades performance due to the decode logic and the array dimensions required, and increases cost through inefficient use of silicon. Many logic applications require more inputs, but not the flexibility of a full decoder.

This dilemma was solved by introducing a second fuse matrix in place of the fixed decoder, allowing selection only of those product terms required by the design. This made much more efficient use of the programmable matrix. Like the PROM, it was made using fuses which could be configured in the field and was therefore called the Field Programmable Logic Array (FPLA or just PLA). The basic PLA architecture is shown in Figure 3-1(c). Unlike the PROM, the PLA can handle logic functions requiring more input variables with much less than 2^n product terms.

However, the additional fuses of the second matrix in the PLA require additional selection and programming circuitry, which makes it intrinsically more expensive than a comparable PROM. This can lead to cost inefficiencies when only a few product terms are being used. Also, a programmable array imposes a longer delay than a hardwired decoder and is the dominant factor in signal delay through a PLD. Therefore, it is difficult for a PLA with programmable AND and OR arrays to compete with the speed of a PROM of similar size.

Cost efficiencies comparable to the PROM were achievable only by reducing the overhead circuitry necessary. One solution was to hardwire the OR array and allow the user to program only the AND array. This arrangement is known as the Programmable Array Logic (PAL®) architecture shown in Figure 3-1(d). The introduction of the PAL device was the key which unlocked the potential of efficient programmable logic for designers. The PAL device could be made more cost-effectively than the PLA and could substitute flexibility in the OR array by being offered in a variety of basic configurations. Also, since the number of programmable arrays through which a logic signal needed to pass was reduced from two to one, device performance improved considerably.

Development of the initial PAL concept has led to families of products in several technologies, offering a range of design building blocks, power requirements and performance. Developments in cell technology beyond the original metal fuse-links have led to the “vertical fuse” programming cell, offering higher programming yields and faster signal propagation.

The advantages of the one-time programmable (OTP) devices described above hinge on the ability to configure integrated circuits in the field. Once blown, the cells cannot be reconfigured. More cost savings would be available if PLDs could be reconfigured. This would permit device reuse and exhaustive factory testing for yet higher programming yield and improved reliability. Recent developments in semiconductor technology have made electrically erasable cells available for memory and logic products. Such reconfigurable cells have been used to make “Generic Array Logic” (GAL®) devices. Basic GAL devices offer not only all the logic configurations likely to be required but also allow modification of prototypes for development debug and also of systems in the field for reconfiguration or upgrade.

3.2 Design Advantages

Digital logic designers have always worked under constraints. Reduction of system size and cost demand efficient, compact designs. System reliability forces designers to compromise between evolving solutions and existing proven methods. Future revisions demand a degree of flexibility which must be anticipated. Yet the systems themselves increase in complexity, components sophistication requires ever more sophisticated tools and conceiving the optimal design for so many parameters requires a range of skills which must constantly be developed.
FIGURE 3-1. Comparison of Programmable Logic Basic Architectures

(a) Desired Logic Functions

LOGIC EQUATIONS

\[
\begin{align*}
F_1 &= A \\
F_2 &= \overline{A}B \\
F_3 &= A + \overline{B} \\
F_4 &= \overline{A}B + A\overline{B}
\end{align*}
\]

(b) PROM Architecture with Fixed AND (Decoder) and Programmable OR Array

(c) PLA Architecture with Programmable AND & OR Arrays

(d) PAL Architecture with Programmable AND Array and Fixed OR-Gate Connections
PLDs do not solve all of these problems. But they do provide a method of dealing with some of the major issues in an effective way by providing a uniform methodology. This section discusses some of the major advantages available to designers through the use of PLDs.

SIMPLIFIED SYSTEM DESIGN
The semi-custom approach of PLDs allows the user to specify exactly the functions which will be implemented in the logic. This avoids the problem of interconnecting various SSI/MSI components to achieve the same result. At the same time, PLDs offer speed advantages through reduction of interconnects. The methodology becomes one of writing the equations for the desired function with the help of the software tools and using such equations to configure the appropriate devices. This methodology accelerates both the conception and implementation of the design. Since the software tools available handle all the details regarding device configuration, the designer is left free to focus on the design of the application itself. An additional benefit is that many of the changes which usually need to be incorporated in a design after implementation can often be accommodated by altering the PLD’s internal configuration, thus avoiding rewiring of prototype and printed circuit boards.

INCREASED FUNCTIONAL DENSITY
Despite the development of LSI and VLSI devices which package an amazing amount of logic on a single chip, system designers have still had to contend with the power, space and drive problems associated with a myriad of SSI/MSI packages used either for “glue” or for specific design requirements not available in off-the-shelf parts. Ordinarily, this will decrease the functional density.

PLDs, however, offer a compact solution with high functionality and less waste in I/O and interconnect lines, so that functional density can approach that of custom logic without the associated engineering charges. On the other hand, the combination of several functions on a single chip reduces power as well as space and has the added benefit of boosting system performance through a reduction of interconnects.

3.3 Manufacturing Advantages
While PLDs offer a number of advantages over SSI/MSI for the designer, there are a number of considerations which only become apparent when system volume production is examined. These include:

- Cost of Inventory
- Cost of Ownership
- Cost of Upgrades/Modifications
- Reliability
- Cost of Upgrades/Modifications
- Reliability

COST OF INVENTORY
A hidden cost associated with many designs is the inventory of parts required in order to sustain it in production. PLDs are able to reduce this cost by offering a substantial reduction in the number of different part types which are otherwise required to build a given system using standard logic parts. This is particularly true for GAL devices. Users may find that the inventory cost advantages of GAL devices tend to offset the slight difference in price of GAL over standard PAL devices.

COST OF OWNERSHIP
The cost of ownership of a particular part is more subtle than the simple price at which it is available on the market. In fact, the cost of ownership includes the cost of those devices which fail and which must be replaced. This cost increases dramatically as the discovery of failures occurs later in the production process.

The additional cost of a failed part at incoming inspection is relatively minor. However, PLDs must be programmed to the user’s pattern before any meaningful functional testing can be done by the user. Therefore, the first detectable device failure for a PLD will be a programming failure detected during device verification on the programming equipment. This is the most frequent of all failure modes for PLDs. Vertical-fuse PAL devices and electrically-erasable GAL devices have a much higher factory testability and an inherently more reliable programming technology. This gives these advanced technology products a strong advantage at this early stage of production.

Once devices have been verified, functional testing can be performed while still loaded in the programming unit or on production IC testers. Otherwise, the device functionality is tested in-circuit. Both involve further production costs which contribute to cost of ownership, particularly if the device is already soldered in place.

Failures beyond this may occur at the board or system level. This sometimes occurs despite testing at previous stages and happens to standard non-programmable products as much as to PLDs. Most are detected in production, but are increasingly costly to correct.

The final location at which device failure over product lifetime can occur is in the field. Field failures are attributed primarily to device reliability. Since field failures have the highest associated cost, National Semiconductor performs extensive reliability testing on all PLD products, processes and packages. Continuing developments in circuit and programming technologies are creating inherently more reliable PLDs, as exemplified by the vertical-fuse PAL devices.
COST OF UPGRADES AND MODIFICATIONS
Unlike standard SSI/MSI, PLDs offer some degree of flexibility in permitting alterations to a circuit which is already in production. At its simplest level, all PLDs permit some degree of reconfiguration within the existing printed circuit board and device pinout. Even if the original one-time-programmable (OTP) PLD cannot be reconfigured, subsequent production can alter the circuit by altering the fuse map without any other changes. Where the change is more dramatic, the use of a pin-compatible GAL device may still offer a change which requires no circuit board alterations. Field alterations are then limited to replacing a device and do not require the standard time-consuming cut-and-jumper approach.

HIGHER RELIABILITY
The higher levels of integration associated with contemporary digital design have brought reliability and testability to the fore as issues in system design. Increased system and integrated circuit complexity have made it crucial that an acceptable design debug and system test methodology be included as part of the development process. PLDs help in this by being both flexible and versatile in design debug, particularly reconfigurable GAL devices.

It has also been shown that system reliability is a function of the number of components used and the pins and wiring necessary to interconnect them. The decreased package count over standard SSI/MSI devices through the use of PLDs therefore helps maximize system reliability.

Recent advances in PLD circuit design and processing technology have greatly improved the long-term reliability of both OTP and reprogrammable E2CMOS products. Sophisticated test circuitry built into these products allows increased testability of on-chip circuit elements and programming cells to ensure long-term reliability.

3.4 Alternative Methodologies
Since the introduction of LSI, there has been a growing “complexity gap” between high-density, high-functionality devices and the low-density device available to interconnect them or provide non-standard design alternatives. The advent of PLDs has helped somewhat to bridge that gap.

STANDARD LSI
Advances in this area have been made at the cost of device flexibility and support software complexity. A hidden disadvantage has been the need to interface such devices into a given system, often resulting in a disproportionately high package count and power supply problems. PLDs can be used for package reduction of the inevitable “glue logic” around LSI applications. But also, frequently design requirements may be for a controller which doesn’t require microprocessor complexity or cannot accept the slower microprocessor speeds. While standard LSI attempts to be a universal solution, the system under design may require a much simpler solution and/or special functions not provided in available LSI. PLDs can often provide a more appropriate, higher-performance, cost-effective and compact design in such cases.

STANDARD SSI/MSI
While having mounting competition from other design methodologies, SSI/MSI logic continues to be used in many designs where specialized functions are required in lower production volumes. PLDs offer a more effective means of implementing these functions in all but the most trivial examples because of their ability to reduce package count, increase performance, offer design support tools and simplify revisions and upgrades. Where systems require absolute minimum delays through short logic paths or standard logic functions, standard SSI/MSI devices are often an indispensible solution. However, in most other “glue logic” applications, the long-term efficiency and flexibility of PLDs tend to outweigh any initial parts cost savings derived from using SSI/MSI, especially when design revision is considered.

FULL CUSTOM
These provide an excellent solution to well-defined, low-to-medium complexity logic which is expected to be produced in very high volume. The risks involved in committing both the time and money mean it is seldom used in practice unless extreme performance/density is required or extreme high volume is expected.

SEMI-CUSTOM ASIC’s
The success of this semi-custom approach depends on the efficiency of use of the gates available. This requires skilful partitioning of the logic and careful selection of the gate array. It has far less development time and cost associated with it than full custom, but fixed costs must still be considered, along with the difficulty of correcting any problem in the logic once committed to silicon.

Even though prototype development time for gate arrays has been significantly reduced over the past few years, almost any redesign requirements can imply mask revision and have a devastating effect on system introduction.

3.5 PLD Architecture Overview
All of the PLDs currently offered by National are PAL-type architectures (except the GAL59V16 which will be a PLA architecture). This section describes some of the basic architectural features found in the various PAL-like devices (including the GAL devices). For more detailed descriptions of the architectures of specific devices, refer to the appropriate datasheet in Section 2.

LOGIC ARRAY STRUCTURE
The PAL architecture is based on a single programmable AND-gate array with fixed OR-gate connections. The AND array consists of a number of “input lines” running in one dimension across a number of “product-term lines” running in the orthogonal dimension with programmable interconnection cells at all intersections. For every input signal (logical input variable) applied to the array, a true and complement pair of input lines are provided.

A product term is satisfied (logically true) while all input lines connected to it (via programmable cells) are high. If neither the true nor complement of an array input is connected to a product line, then that array input represents a “don’t care” value with respect to that product term.

In all PAL-based devices covered in this book, all product terms are dedicated to specific device outputs. The number of product terms allocated to each output logic function varies from device to device.

In many devices, all of the product terms allocated to each output are simply ORed together to produce the output logic function. The original PAL devices, which have become known as the “Small PAL Family”, are based on this simple architecture alone. Figure 3-2 shows a representative Small-PAL architecture, that of the PAL12H6. Such devices are commonly used for address decoding, multiplexers and random control logic applications.
FIGURE 3-2. Logic Diagram of a Typical "Small PAL Family" Device—PAL12L6
In other devices, one or more of the product lines are used to control other attributes of the corresponding output signal, such as TRI-STATE® enable. Devices in the "Medium PAL Family" have TRI-STATE outputs with a feedback path from the device pin into the logic array. This allows a pin to perform bidirectional I/O or to act as an additional dedicated input.

The fundamental transfer function of a PAL-like device is INVERT-AND-OR, and may be specified directly by a sum-of-products Boolean equation.

**REGISTERED OUTPUTS**

In addition to higher densities and TRI-STATE I/Os, the Medium-PAL devices also provide edge-triggered registers on some logic function outputs. The output of each register is also fed back into the logic array to facilitate the design of sequential circuits such as state machines, counters, shifters, etc. Figure 3-3 shows the architecture of a typical Medium-PAL device, the PAL16R4, with both registered and combinatorial outputs.
EXCLUSIVE-OR GATES
Some PAL architectures add an XOR gate, combining two small AND-OR functions, to each output, as shown in Figure 3-4. The XOR gates combined with output registers facilitate design of counters, state machines and small arithmetic functions.

FIGURE 3-4. PAL20X10 Block Diagram
PROGRAMMABLE OUTPUT POLARITY

Several more recent PLD families provide programmable output polarity. Additional programming cells are included in the output logic paths to optionally invert the individual output signals. This allows more convenient system interfacing by eliminating the need for external inverters. The output inversions in conjunction with the complementary array inputs also allow product-of-sums logic equations to be directly implemented using DeMorgan's theorem. This may result in more compact logic minimization for some applications.

Programmable polarity is provided in the TTL Polarity PAL Family, Registered-Asynchronous (RA) PAL devices, all GAL devices and all ECL PAL devices.

ADVANCED PRODUCT FEATURES

Advanced features appearing in some of the newer PLD architectures generally fall into two categories: 1) more diversified use of logic terms for on-chip control functions, and 2) more non-array programming cells used to invoke optional peripheral logic paths.

Just as traditional Medium PAL devices use one product term per output to control the TRI-STATE enable, the Registered-Asynchronous devices, PAL16RA8 and PAL20RA10, use three additional “specialized” product terms to control the clocking, reset and preset of each output register (Figure 3-5). This type of PLD is primarily useful in random control logic applications which would normally be implemented using SSI/MSI Gates and flip-flops, such as 74LS74.

GAL devices use additional programming cells to redirect their output logic paths to emulate a wide variety of TTL PAL architectures, plus other original configurations. These “architecture cells” select registered vs. combinatorial outputs, TRI-STATE control signals, I/O feedback paths, and output polarity. The term “Output Logic Macrocell” (OLMC) is commonly used to describe such sophisticated peripheral logic which is user-configurable by means of programmable architecture switches. Figure 3-6 shows the complete logic schematic of a GAL OLMC. Fortunately, the logic paths and architecture switches are automatically configured by design development software according to the designer’s familiar logic equations.

FIGURE 3-5. Registered-Asynchronous (RA) Macrocell
3.6 Programmable Logic from National

National Semiconductor offers a broad range of products in the PLD field. From the original PROM devices, the line has expanded to include both the standard lateral fuse-link and the new vertical-fuse PAL devices and now the highly flexible GAL devices.

TTL PROMS

These memory devices can be used as logic devices in instances where the number of inputs is low and the number of product terms required is high. PROM products most frequently used in logic applications belong to the high-speed bipolar family with depths ranging from 32 to 1024 and widths of either 4 or 8 bits. Detailed information on National PROM products is available in a separate databook.

LATERAL FUSE TTL PAL PRODUCTS

These are the workhorses of the PLD product line. They include devices which offer a wide range of function, price and performance. Implemented in advanced bipolar TTL, they use the more traditional titanium-tungsten (TiW) lateral fuse and are available at prices competitive with standard MSI logic. For most applications requiring moderate functional density and medium to high speed, these offer the optimal cost-effective solution.

VERTICAL FUSE TTL PAL PRODUCTS

This innovation, begun at Fairchild Semiconductor, was developed to address the need for the highest performance required in TTL system environments. A vertical fuse structure on the die not only reduces die size, but also decreases propagation time due to more compact circuitry. Vertical fuse technology is used to implement the highest speed PAL devices ("Series-D" and faster). At the same time, this technology offers increased reliability, testability and programming yield. A more detailed discussion of the technology involved is given in Section 6.1.

ECL PAL PRODUCTS

A large range of the traditional PAL architectures are available in ECL for those system designers taking advantage of this technology. In very high speed applications where ECL is typically used, logic optimization becomes crucial and the delays involved in off-chip wiring become more pronounced as a fraction of the total delay. The SSI/MSI logic families available in ECL are not as robust as those in TTL and tend to consume larger system board areas in implementation. Both problems can be more effectively reduced through the use of ECL PLDs. Consolidating logic into PLDs moves local logic interconnections on-chip eliminating the associated wire delays. Also, by reducing board area consumed by the logic implemented in the PLD, remaining on-board logic becomes more compact thereby reducing the trace lengths of interconnections among surrounding logic. This adds to the speed advantage. Reducing required board area also allows the system designer to increase the amount of on-board logic.
E2CMOS GAL PRODUCTS
The CMOS technology offers advantages over standard TTL in some applications. Modern CMOS technologies require considerably less power with little speed penalty. The recent developments in electrically erasable CMOS devices (E2CMOS) offer additional advantages in flexibility and testability. Using a cell which can be reprogrammed multiple times, a GAL device offers increased ease in system prototyping.

A GAL device also has a powerful feature in its reconfigurable output macrocells. This permits it to replace a variety of more conventional PAL devices, thus reducing inventory requirements. The intrinsic higher device reliability and ability to be fully tested in the factory with guaranteed yields of 100% can replace customer incoming device inspection.

PRE-PROGRAMMED AND MASK-PROGRAMMED PRODUCTS
As the volume of system production increases and the confidence in the design solidifies, it may make economic sense to consider using one of the pre-programmed device programs from National. For production flows which require quantities of PLDs which cannot be programmed cost-effectively at the customer site, National Semiconductor offers a program which ships PAL devices already programmed to customers for immediate inclusion in the system.

For production runs in high volume for which designs are no longer liable to change, it may make economic sense to use the National Masked Logic (NML) program. This is an arrangement whereby PAL devices are manufactured with a given logic configuration already fixed in the metallization step. The relationship of NML to PLDs is similar to that of ROMs to PROMs. Eliminating all dependency on programmable cells (fuses) and the supporting programming circuitry means less on-chip circuitry is liable to cause device failure. The resulting increase in functional yield at the factory allows NML devices to be offered at more competitive prices with respect to standard PLDs, once initial engineering costs are recovered.

Both programs avoid the manufacturing costs associated with device programming and related programming failures. They also considerably enhance device reliability due to the thorough factory test performed on functional devices before shipment using the customer's test patterns. Because of the resulting increase in product quality levels, further manufacturing costs may be saved by eliminating incoming component inspection.

3.7 Design Development Tools
Design development with PLDs involves the use of a few tools which assist both in the design conception and implementation stages. A more detailed discussion of design tools is given in Section 5. Competition in the PLD support market has considerably reduced the investment necessary to acquire the appropriate hardware and software tools.

PROGRAMMING HARDWARE
PLDs are typically configured on a piece of hardware known as a programmer. The selection has widened due to the proliferation of PLD types and now includes an extensive variety of both device-general and device-specific programmers. Several major manufacturers sell general programmers, either as a stand-alone system or as an add-in to an existing computer such as an IBM® PC, and in a broad range of feature complements and price.

To be able to handle a variety of PLDs, the socket into which the PLD is placed can usually handle different device and package types. Some have multiple sockets built in. Most general programmers are capable of configuring a wide variety of PLD products when equipped with the necessary adapter or software cartridge/diskette. Special-purpose device-specific programmers have been introduced with newer PLD products which, due to advanced circuit or programming technology, require waveforms not immediately accommodated by existing programmers.

While it is still possible to configure cells "by hand", the bulk of PLDs are now configured with the help of a logic assembler which presents the programmer with a standard or JEDEC file. This is a fuse map for a specific device which, when downloaded, permits the programmer to configure a given device in the socket. The JEDEC file conforms to an industry-wide standard and ensures that files generated by virtually any software can be used to configure PLDs on almost any hardware.

National provides periodic information on available programming hardware, indicating which models accommodate the various PLD families and which models have been certified to meet the programming requirements for NSC parts. Please contact your local National Semiconductor sales office or distributor for information on suppliers currently offering support for PLDs of interest. In the rest of this design guide, only device-general programmers will be discussed since these are usually capable of handling the entire PLD product line from National Semiconductor.

DEVELOPMENT SOFTWARE
These are software packages available for certain computers which allow the user to enter the design through the keyboard in a number of ways. Most packages permit the use of Boolean logic equations and truth tables. Assemblers are from specific PLD suppliers, programmer vendors or third party vendors.

NATIONAL SEMICONDUCTOR PLAN™ SOFTWARE
National Semiconductor offers a PLD assembler known as PLAN software, which is a package optimized for use with the PLDs available from NSC and includes most industry-standard PAL architectures. PLAN software is available to operate primarily on IBM-compatible PC under MS-DOS and uses Boolean equations as the method of design entry. Unlike others, the PLAN assembler allows designs to be specified independent of specific device architectures and will optionally select an appropriate device which will accommodate the final design. Refer to Section 5.3 for a more in-depth discussion of the PLAN package.

OTHER ASSEMBLERS/COMPILERS
High-level assemblers provide many automatic features that are not found in other assemblers. They are usually device and manufacturer-independent and some tools may be usable with other software packages. While they are still capable of accepting Boolean equation data entry, they offer other input alternatives, such as gate-level graphics and higher-level state machine descriptive language, and allow features such as set-definition and automated logic reduction. Several higher-level packages designed for use with all PLDs are generally available. Two of the most popular are CPU® software from Logical Devices and ABEL® software from Data I/O.
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Section 4
Programmable Logic Design Methodology

PLDs offer a number of design advantages to the designer. But in order to make use of these, the designer must apply a specific design methodology in order to maximize the effectiveness of the PLD tools available. This chapter outlines the steps by which this is done and illustrates their use by specific examples. Details of the use of the most important tools are given in Section 5. For more diverse examples without as much emphasis on methodology, refer to Section 7—Applications.

4.1 Design Development Process

The design development process for PLDs proceeds in three main phases:

• Logic design
• Design implementation
• Design/Logic verification

Within each phase, an experienced designer will pass through a number of steps. While the process may appear involved at first, it is mostly a stylization of good design practices and efficient use of the PLD tools available to the designer.

Within the Logic Design phase, the steps involved are common procedure for any digital design engineer and can be tailored to suit the individual taste and design requirements. The main steps are:

• Define the system problem
• Generate a block diagram
• Implement the function logically
• Derive the Boolean equations describing the design

These are largely self-explanatory. For readers requiring some background information on logic design principles, refer to Appendix A.

Design Implementation consists largely of selecting and using the tools to translate the results of the first phase into a configured PLD. It consists of steps:

• PLD family and device selection
• Partitioning the logic to fit the devices selected
• Equation entry
• Running development software and JEDEC file creation
• Platform and programmer configuration
• JEDEC file transfer
• Device programming

The preparation of software, platform and programmer need be done only for the initial use of PLDs. Following that, the other functions are all straightforward operations often handled automatically by the PLD tools selected and not requiring involvement on the part of the designer.

Design verification is the final phase during which the correct programming of the device is checked, along with the generation of test procedures which verify that the device itself implements what was originally required. The steps in this phase are:

• Device programming verification
• Design test vector generation
• Device simulation
• Device functional test
• Design documentation

The effort involved in each depends both on the design complexity and the tools available. As with any other design, the verification phase can be too easily overlooked in the entire design process, but effort spent in judicious testing and adequate documentation is normally well spent.

Each of these steps is described in detail later in this section.

4.2 Logic Design

This section gives a detailed account of the steps involved in generating the initial theoretical design, illustrated by reference to an example of a 6-bit bidirectional shift register.

DEFINING THE PROBLEM

As with any other design methodology, the first step involved is a clear definition of the problem to be solved. In the case of the shift device, what is required is a device with the following characteristics:

• 6-bit wide right/left shift register
• Parallel input and output ports
• Clock input
• Control lines for mode selection
• Ability to be cascaded via two bidirectional serial ports

Additional criteria which might play a role in selection of the final solution are the need for low parts count, power and speed considerations, and the need to interface with or mop up other logic in the area. For the purpose of this example, assume these criteria impose no special constraints.

DESIGNING THE LOGIC

Based on the above criteria, the block diagram of the logic can be generated directly, as shown in Figure 4-1. The signal names are given to permit unambiguous reference to their function and any considerations of logic context within the system should be incorporated here.
From the block diagram, the designer derives the detailed functional description of the intended behavioral concept. This may take a number of forms, depending on the application and the preference of the designer. One common method of expressing the detailed operation of a registered application such as this is a function table, which is shown in Figure 4-2 for reference. Another common method is the use of timing waveforms which are omitted for this example due to its simplicity. The target function is further defined by deriving a detailed logic schematic (as shown in Figure 4-3), combinatorial truth table, or direct expression in Boolean equations.

**FIGURE 4-1. Block Diagram Showing 3 Cascaded Shift Registers**

<table>
<thead>
<tr>
<th>Function</th>
<th>SL</th>
<th>SR</th>
<th>RILO</th>
<th>Q5</th>
<th>Q4</th>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
<th>Q0</th>
<th>LIRO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hold</td>
<td>0</td>
<td>0</td>
<td>Z</td>
<td>Q5</td>
<td>Q4</td>
<td>Q3</td>
<td>Q2</td>
<td>Q1</td>
<td>Q0</td>
<td>Z</td>
</tr>
<tr>
<td>Shift Right</td>
<td>0</td>
<td>1</td>
<td>RI</td>
<td>RI</td>
<td>Q5</td>
<td>Q4</td>
<td>Q3</td>
<td>Q2</td>
<td>Q1</td>
<td>Q0</td>
</tr>
<tr>
<td>Shift Left</td>
<td>1</td>
<td>0</td>
<td>Q5</td>
<td>Q4</td>
<td>Q3</td>
<td>Q2</td>
<td>Q1</td>
<td>Q0</td>
<td>LI</td>
<td>LI</td>
</tr>
<tr>
<td>Parallel Load</td>
<td>1</td>
<td>1</td>
<td>Z</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>Z</td>
</tr>
</tbody>
</table>

**FIGURE 4-2. Functional Operation Table for Shifter Example**
DERIVING BOOLEAN EQUATIONS
In order to provide a definition of the circuit which the design tools can handle, it is usually necessary to express the design in terms of Boolean equations. The fundamental transfer function of a PAL device is the sum-of-products or, through DeMorgan inversion, product-of-sums form. Logic equations can be derived directly from the function table shown in Figure 4-2, the logic schematic in Figure 4-3, or from the method of logic implementation preferred.
For any TRI-STATE output, including bidirectional I/O lines, additional equations may need to be specified to define the control functions of these lines. This is illustrated in the example of the 6-bit shift register.

FIGURE 4-3. Gate-Level Logic Schematic of Shifter
For the 6-bit shift register example, the equations are:

\[
\begin{align*}
Q_0 & \leftarrow Q_0 \cdot \overline{SR} \cdot SL + Q_1 \cdot SR \cdot SL + LIRO \cdot \overline{SR} \cdot SL + D_0 \cdot SR \cdot SL \\
Q_i & \leftarrow Q_i \cdot SR \cdot SL + Q_{i+1} \cdot SR \cdot SL + Q_{i-1} \cdot SR \cdot SL + D_i \cdot SR \cdot SL, \quad i = 1 \ldots 4 \\
Q_5 & \leftarrow Q_5 \cdot SR \cdot SL + RLO \cdot SR \cdot SL + Q_4 \cdot SR \cdot SL + D_5 \cdot SR \cdot SL \\
LIO\text{OUTPUT} & = Q_0; \quad LIRO\text{ENABLE} = SR \cdot SL \\
LIO\text{OUTPUT} & = Q_5; \quad LIRO\text{ENABLE} = SR \cdot SL
\end{align*}
\]

The device logic requirements are now unambiguously defined in a form acceptable to PLD design tools.

**LOGIC MINIMIZATION**

It is generally good practice to minimize the logic equations to eliminate any extraneous variables or unnecessary redundant min-terms. Non-minimized logic does not interfere with proper device functionality. However, it may result in a design requiring more resources than available in a particular device which could otherwise accommodate the reduced equations. Also, logic redundancy could render some gates or nodes within the programmed device untestable.

On the other hand, intentional use of redundant terms may be a convenient method of avoiding logic hazards in combinatorial (unsynchronized) logic functions. For a more thorough discussion of logic minimization and avoiding hazards, refer to Appendix A.

**4.3 Design Implementation**

Now that the basic theoretical design has been completed, the next stage is to transfer this design into a physical device. This requires the selection of the device to be used and a number of tools with which the transfer is accomplished. Refer to Section 5 for a more detailed discussion of PLD tools and their use. The example of the 6-bit shift register is again used for the purpose of illustration of the principles.

**SELECTING A DEVICE**

Once the logic design is defined, a PLD needs to be found which can most efficiently accommodate the logic required. Some design tools, such as PLAN™ software, provide this function automatically. Otherwise, a manual selection must be made among the devices available.

The first criterion to consider is the family type required. PLDs come in a variety of technologies and speeds and offer a spectrum of possible categories from which the device is selected. If the design requires ECL compatibility, CMOS low-power or very high speed, this narrows the choice down to a device available in that category.

If the target logic is too complex to fit into any single PLD, then the design must be partitioned. A decision which must be made at this point is between using more complex, expensive and slower parts, and the more traditional medium PAL devices. Partitioning criteria are heavily dependent on the goals of a specific design.

Once the family has been selected, the initial selection within the family is determined by examining the application's block diagram, function table and logic equations. Based on these, the following parameters are established:

- Number of registered outputs required
- Number of combinatorial outputs required
- Number of inputs required
- Clocking requirements
- Complexity of each logic equation (number of min-terms required)

For our 6-bit shift register, it can be seen that the requirements are:

- Six registered outputs (for the parallel-out lines)
- Two combinatorial bidirectional I/O lines (for the serial ports)
- Six parallel data inputs plus two mode control inputs
- Single master clock
- No more than four product terms per output function

Referring to the selection tables in Section 1.1, select the family which complies with the overall system requirements. Then select a device which furnishes all the requirements. For this example, the PAL16R6 and the GAL16V8 both fulfill the requirements. Note that others like the PAL20R6 would also be capable of implementing the design, but would involve a 24-pin rather than a 20-pin part and higher power dissipation.

At this stage, the appropriateness of the device is also checked by examining its detailed block diagram (see Section 1.3 or the appropriate datasheet in Section 2). While most initial device selections, particularly for simpler designs, will be correct, difficulty can arise with a design, such as a priority encoder, which requires a large number of product terms. In such a case, while I/O requirements might suggest a particular PLD, it may not offer enough product terms to accommodate the design. The PLAN software, which accepts device-independent Boolean equations selects, if possible, the least complex device which conforms to all requirements automatically.

For our design example, either the PAL16R6 or GAL16V8 would be appropriate. Where power-dissipation or highest quality levels are of importance, the GAL® solution offers more flexibility with reduced cost of ownership. For simplicity, we will assume the PAL16R6 is selected.

**DESIGN/EQUATION ENTRY**

Before proceeding further, the software tools will need to be run on the computing platform selected. This normally involves installing an assembler such as PLAN software onto a PC in preparation for the entry of the programming information in the form described below. Refer to the individual software documentation for details.

The equations derived earlier must now be entered into the software tool selected. Higher-level packages provide a sophisticated user interface to do this. The PLAN assembler will accept a text file created with a common editor utility as an input file. Other packages have varying degrees of flexibility. The syntax requirements of the software package must be adhered to, although virtually all provide a parsing and evaluation feature with associated error messages to correct errors in the input file.

Using the example of the 6-bit Shift Register, the method of entering the data to the PLAN package involves first converting the equations derived earlier into PLAN syntax. This follows the original very closely and is shown in Figure 4-4. This information can be generated using any convenient editor, such as EDLIN, or even a word processing package.
Title: 6-Bit Cascadable Shift Register

Pattern: 6SHFT

Revision: A

Author: Tarif Engineer

Company: National Semiconductor Corporation

Date: 11/28/1989

Chip: 6SHIFT PAL16R6

Pin: 1 2 3 4 5 6 7 8 9 10

/CLK, SR, D0, D1, D2, D3, D4, D5, SL, GND

Pin: 11 12 13 14 15 16 17 18 19 20

/G, RILO, Q5, Q4, Q3, Q2, Q1, Q0, LIRO, VCC

Equations:

/00 := /00 * /SR * /SL
+ /01 * SR * /SL
+ /LIRO * /SR * SL
+ /D0 * SR * SL
/01 := /01 * /SR * /SL
+ /02 * SR * /SL
+ /00 * /SR * SL
+ /D1 * SR * SL
/02 := /02 * /SR * /SL
+ /03 * SR * /SL
+ /01 * /SR * SL
+ /02 * SR * SL
/03 := /03 * /SR * /SL
+ /04 * SR * /SL
+ /02 * /SR * SL
+ /03 * SR * SL
/04 := /04 * /SR * /SL
+ /05 * SR * /SL
+ /03 * /SR * SL
+ /04 * SR * SL
/05 := /05 * /SR * /SL
+ /RILO * SR * /SL
+ /04 * /SR * SL
+ /05 * SR * SL
/LIRO := Q0
/LIRO.TRST := SR * /SL
/RILO := /05
/LIRO.TRST := /SR * SL

End of 6SHFT

FIGURE 4-6. Chip Diagram (DIP)

FIGURE 4-4. PLAN™ Input File for Shifter Example
FIGURE 4-5. JEDEC File for Shifter Example Produced by PLAN Software
COMPILATION—CREATING THE JEDEC FILE
At this stage, pin assignment is normally made, either manually or automatically by the software. PLAN offers an automatic assignment, which can then be edited manually, if desired.

Once the equation file has been entered and pin assignments resolved, the assembly is performed on the platform, the results of which are a JEDEC fuse map for downloading to the programmer.

In order for the equations to be converted into a bit pattern from which the cells of a PLD can be systematically programmed, the initial equations must be converted into a form, known as the JEDEC file. The JEDEC file is an industry-wide standard accepted by all programming hardware. It consists of a formatted table indicating all of the cells (fuses) in the PLD to be programmed to implement the specified logic functions. This is done by a module within the software tool known as the assembler. Details of operation of the assembler varies from one package to another, but each provides syntax checking and an evaluation of whether the design can be implemented in the device chosen, as well as the JEDEC file itself, which is normally stored on disk ready for downloading to a programmer.

The actual form of the JEDEC file is usually of little interest to the system designer. Its only purpose is to provide a uniform interface between commercial PLD software and hardware tools and no real information for the designer is provided by its details. It may occasionally be useful as a debugging aid to isolate any problems occurring between equation entry and functional test.

PROGRAMMING HARDWARE PREPARATION
Before the cell data can be transferred, the programmer needs to be connected to the software platform and fitted with any socket adapters required to accommodate the blank sample device.

For the purpose of this example, a PAL16R6 is being programmed with a Data I/O Model 29 programmer equipped with Logic-Pack. In order to do this, connect the System 29 to the platform via an RS232C cable, according to the system documentation. An outline of this is given in Section 5. A PAL16R6 requires the 303A-011A adapter to be installed on the Logic-Pack. Look up the PAL16R6 on the device chart to determine and enter the family and pinout code.

DEVICE PROGRAMMING
This step involves transferring the prepared JEDEC file across a communication link from the platform to the hardware programmer. Each programmer differs slightly, but generally each requires that a number of prompts be answered with such information as file name, device type and manufacturer. Usually, a test is run at this time on the device by the programmer which ensures that the device is correctly oriented in the socket and is in fact blank and able to be programmed. The correctness of data transfer is verified by means of a checksum transmitted with the file.

For the purposes of our example, the System 29 provides all the prompts required to do this.

Now that all relevant information has been entered into the programmer, it is a matter of simply invoking the Program function.

This translates the JEDEC file into addresses, data patterns and programming pulses, which, when applied to the pins of the device in the socket, will configure the cells of the device in a pattern which will cause the device to operate in accordance with the original design. The implementation of the design in the PLD has now been completed.

Again, for the purposes of our example, the System 29 provides all the prompts required to do this.

4.4 Logic Verification
Verification is required to ensure not only that the device has been configured exactly as intended, but also that the programmer has functioned correctly and that the design performs as originally intended. Again, this takes the form of several steps.
PATTERN VERIFICATION

This may be performed automatically by the programmer. If not, it is recommended that a manual verification run is performed while the device is still in the programmer to ensure that the pattern set in the device corresponds to that specified by the fuse map in the JEDEC file. This is a simple step which is done by the programmer itself. The programmer reads the pattern directly from the PLD, similar to reading a PROM, and compares this directly with the original JEDEC file still resident in the programmer.

TEST VECTOR GENERATION

Particularly with more complex designs, it is recommended that some consideration for a set of device exercises, generally known as test vectors, be given as early as the equation entry stage above. Some advanced software tools may provide automatic generation of test vectors from the equations as they are entered. Otherwise, vectors must be generated by hand. Even in the case of automatic test vector generation, some designers prefer to add their own additional vectors to verify application-specific operations.

For a design of the complexity of our 6-bit shift register, test vectors are easily generated by hand, as shown in Figure 4-7. In this case, a test such as walking ones and zeroes is probably sufficient to prove functionality of the device beyond reasonable doubt. For more complex designs, it may be helpful to employ fault-grading software to ensure adequate coverage of all design paths and gates by the test vectors.

DESIGN SIMULATION

This optional step generates the device output vectors which allow verification of correct design operation. This can be done manually, or with the help of the simulator module of the software tool, to predict the output configuration for the device based on the original software model entered as Boolean equations.

The output vectors from the simulation must be examined to confirm that the model operates correctly. They also provide the output states, which must accompany the test vectors for functional testing of the device.

Beyond device-level simulation, additional software is becoming available to generate models of the programmed PLDs for use in system-level simulations. Such simulations are typically performed on CAD workstations and, more recently, personal computers.

DEVICE FUNCTIONAL TESTING

The device is evaluated fully for correct performance of the function desired. In the case of the 6-bit shift register, this would involve checking all the functions outlined in the function table in Figure 4-2.

Varying from one software tool to another, the test vectors are entered (if not generated automatically) into the software, which appends them in the proper format to the JEDEC file, as shown in Figure 4-8. The test vector entry/generation typically follows the equation entry step, so that the combined JEDEC file is down-loaded to the programmer. Later, following device programming and pattern verification steps, the programmer performs the functional test on the PLD while still in the socket. The input vector waveforms are applied to the device pins while in the normal operational mode, and the device output signals are compared with the expected output vectors.

As a final step, most PLDs include a "security cell/fuse" which, when programmed, disables further programming and verifying. This prevents direct copying of the logic patterns resulting in proprietary custom circuits that are difficult to copy or reverse engineer.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Bidirectional I/O</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL</td>
<td>SR</td>
<td>D5</td>
<td>D4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Key: 0 = Apply Low Input, 1 = Apply High Input
L = Expect Low Output,  H = Expect High Output

Note: The device is clocked after applying each input vector. Outputs on the same line are strobed and compared after the clock.

FIGURE 4-7. Functional Test Pattern for 6-Bit Shift Register Example
FIGURE 4-8. JEDEC File Combining Logic Array and Test Vectors for 6-Bit Shifter Example
FIGURE 4-9. PAL16R6 Logic Diagram Showing Fuse Pattern of Shifter Example

TL/L/9988-3
Section 5
PLD Design
Development Tools
Section 5 Contents

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  Selecting the development software

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5.1 Selecting Development Tools

PROGRAMMING HARDWARE SELECTION
The hardware tool used for PLDs is the programmer which physically configures PLDs. There is a wide selection, but due to the continual change in tool availability, details cannot be kept current in a design guide such as this. However, a listing of several programmer manufacturers and models currently available and in development appears in Table 5-1. For information on current tools available, contact your local National Semiconductor sales office.

Generally, programmers are stand-alone devices which interconnect with the computing platform by means of an RS232C link down which the cell configuration is loaded in the standard form of a JEDEC file. While most programmers handle the standard PLDs, as with software, the more specialized or novel the device chosen, the more restricted is the choice of tools available. Device-specific programmers are typically provided for immediate support of newer PLDs requiring programming algorithms significantly different from those already implemented by general-purpose programmers.

SELECTING THE DEVELOPMENT SOFTWARE
When PLDs were first introduced, fuse maps were derived manually. Now, the convenience of assembly-type development software renders the manual approach obsolete. Before PLD design development begins, the appropriate software tool is selected. The software provides the facility of converting the design into a format understandable by device programmers. Depending on the package chosen, a number of other features are offered as well. Software tools reside in a computer, frequently using a PC as a platform.

Most common packages will handle all of the standard PLDs and several are flexible enough to handle many of the less common types as well. Generally speaking, the more specialized or novel the device selected, the narrower the range of software tools available. In the case of our example, almost any software will handle the PAL16R6 device.

The PLANTM software package supports all PLD devices available from National Semiconductor. Ordinarily, newer PLDs with advanced architecture features or original combinations of features take some time to be incorporated into new revisions of general-purpose, third-party software tools. However, software tools provided directly by the PLD manufacturers (such as NSC PLAN software) generally provides support for new products at the time of introduction.

5.2 PLD Programmers

A large selection of programmers are available for use as hardware tools in PLD design and development. They vary in complexity and capability.

TYPES OF PROGRAMMERS
Generally, programmers fall into two categories—device-general and device-specific. Device-general programmers are available from established third-party suppliers, such as Data I/O, and are capable of handling standard PLDs and many specialized ones. This section is concerned mainly with device-general tools as they provide the support necessary for most NSC parts. Device-specific programmers are normally produced by the manufacturer of a non-standard PLD to ensure the availability of tools and are not discussed here in detail. Virtually all programmers conform to the JEDEC fuse map standard.

Device-general programmers have developed from tools which were initially used to configure PROMs. Many of the first-generation programmers show this heritage and require considerable operator intervention to complete the programming function. Developments have since produced tools of increasing sophistication and culminating in systems such as the Data I/O Unisite.

Almost all programmers consist of a stand-alone cabinet, which houses the control electronics and which is connected to the software platform by a communications link for fuse map down-loading in JEDEC file form. The control panel usually includes a keyboard for manual data entry and a universal connector into which are placed adapters which may contain circuitry, algorithm software and/or sockets for specific device types. More recent programmers now have universal sockets equipped with software-configurable pin drivers, which can handle all PLD package types.

Virtually all programmers require a communications port connection to the platform and the installation of communications software in the platform to provide intelligent control of fuse map file transfer. Some involve circuit cards which are installed into PC-type platforms with direct connection to external programming modules. The details vary with the type of programmer.

PROGRAMMER CERTIFICATION
National Semiconductor maintains a program of programmer certification for use with NSC parts. Tools are classified according to the level of support provided for each family of PLDs from National.

For information on current tools available, please contact your local National Semiconductor sales office for information on the latest listings.

Descriptions of some of the more popular programmers which are able to program most or all of National’s PLD product line follow.
Table 5-1. Programmer Manufacturers and Models Certified for National PLDs

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<thead>
<tr>
<th>Manufacturer</th>
<th>Model</th>
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5.3 National PLAN™ Software

The PLAN software package was developed by National Semiconductor for customer support. It is now being offered directly to customers to facilitate the use of all National PLDs. PLAN uses a device independent Boolean equation syntax with extensions to describe advanced features available in new National PLD products such as the GAL6001. Combined with the automatic pin-list generation option, the device independent boolean equation syntax allows a single design file to be compiled into different PLDs without requiring a detailed knowledge of the target PLD architecture.

PLAN software consists of three modules. The assembler "EQN2JED" translates Boolean equations to JEDEC maps and creates documentation files. The dis-assembler "JED2EQN" translates JEDEC maps into a device independent Boolean equation file which can be accepted by the assembler. The GAL translator "PAL2GAL" uses software cross-programming techniques to convert a PAL JEDEC map into a pin compatible GAL JEDEC map. When using PAL2GAL, test vectors in the PAL JEDEC map can be automatically transferred to the GAL JEDEC map.

A synopsis of the available options for each module is displayed when the module name (EQN2JED, JED2EQN, PAL2GAL) is entered by itself on the command line. A complete on-disk instruction manual is provided for reference. Example files are provided that illustrate the assembler syntax. In addition, the disassembler provides a way to create an example file from an existing JEDEC map for all supported devices.

FEATURES OF PLAN SOFTWARE

The main advantages to the designer of the PLAN software are:

- PLAN inputs may be from any standard editor or word processor
- PLAN equations are device independent
- Automatic pin-list generation
- Reverse compilation of existing device maps
- Facilitates PAL-to-GAL JEDEC map conversion
- Design documentation
- Accepts ABEL™ CUPL™ or PALASM™ Boolean equation operators

PLAN software runs on an IBM®/PC or compatible platform, which must include at least 256 kbytes of free memory and MS-DOS version 2.0 (or later).

To illustrate the operation of the PAL2GAL utility, let's run the JEDEC file previously created for the 6-bit shift register example in a PAL16R6 (Figure 4-7) to derive a new JEDEC file suitable for programming the same function using a GAL16V8. The resulting JEDEC map is shown in Figure 5-1.
FIGURE 5-1. JEDEC File for 6-Bit Shift Register Example Converted from PAL16R6 to GAL16V8 Using PAL2GAL Utility Software
5.4 Other Assemblers/Compilers

ABEL™ SOFTWARE

The ABEL package is an example of the second-generation PLD development tools which are usually referred to as high-level assemblers.

From an early version, which supported many PLD devices with logic reduction, simulation and generation of design documentation, it has become one of the standard software tools, capable of supporting a wide variety of PLDs, including PROMs. The most important feature which the most recent developments of ABEL software have added include:

- Revised simulation to support asynchronous devices and macrocells
- Syntax support of multiple-feedback paths
- Library of device-specific macros and functions
- JEDEC-to-ABEL conversion (for recovering undocumented designs)

ABEL software is available for platforms like the IBM/PC, VAX™ and others. The design can be entered using any standard text editor. Any combination of Boolean equations, truth tables or state diagrams can be used. The description falls into four main sections:

- Declarations section, where sets are defined
- Equations section, where Boolean equations are entered
- Truth Table section, where functional tables are entered
- Test Vector section, where the behavior during simulation is given

ABEL automatically performs logic reduction, simulation and conversion to a JEDEC file without requiring further intervention unless some error is encountered.

CUPL™ SOFTWARE

The CUPL package is a high-level compiler similar to ABEL software, which provides a number of functions not normally found in a standard PLD assembler. The input syntax is based on the C programming language. The high-level PLD support language in CUPL software permits development of designs using a systems approach. To this end, several features are supplied, including:

- self-documenting syntax
- state machine input option
- macro substitution
- flexible format
- use of symbolic names
- bit-field capability
- pre-processor functions
- output polarity selection

The macro substitution allows for considerable reduction in the number of keystrokes required for data entry, particularly for more complex functions. The pre-processor function allows the source file to be written in a much more generalized manner up until the actual compilation by the main assembler. This includes definition of the functions in state machine syntax and generalized arguments.

LOG/ICTM Software

LOG/IC is a PLD synthesis tool featuring all the high level design entry formats required for easy and efficient designs. LOG/IC’s HYPERPLD concept allows the user to first enter, simulate and process design, without a need to pinpoint a specific device.

The proprietary PLD optimizer used for logic reduction is an exact PLD optimizer that is fast enough to be applicable for large designs. So, the actual minimal number of product terms is found, ensuring the most cost-effective hardware design.

After the reduction process, LOG/IC’s PLD Data Base may be used to select the best device for the application. This selection process is based on the results of the HYPERPLD optimization as well as on additional interactive parameters like speed, power consumption, packaging, etc.

LOG/IC supports the mainline PALs, GALs as well as ECL devices. The library of supported parts is updated regularly. There is also a LOG/IC-GATES compiler available which accepts the same PLD design files ensuring an easy growth path to gate array designs.

LOG/IC is available on a number of hosts like IBM-PC, SUN3, SUN4, SUN386, APOLLO, HP-9000 and VAX workstations/mainframes. On all hosts, LOG/IC is operated through the same menu driven interface with online help available. An integrated communications program eases the device programmer operation and the downloading of JEDEC files.
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Fabrication of
Programmable Logic
Section 6 Contents

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   ECL PAL devices
   “Series-D/-7” TTL PAL devices with vertical fuses
   E²CMOS GAL devices

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   Test circuitry
   Normal PLD factory test
   Pre-programmed PLD factory test
   NML factory test
   Customer handling and test
Section 6
Fabrication of Programmable Logic

6.1 PLD Technologies
National Semiconductor is a broad-based supplier of programmable logic products. PLD's are offered in a wide range of circuit and programming technologies to address the diverse needs of most customer applications. PLD's can be seen as a stage of sophistication in the continuum from standard TTL logic to full-custom circuits. To provide the flexibility of configurable logic, PLD's make use of a number of circuit and programming technologies. These vary, depending on the type of PLD.

STANDARD, "SERIES-A" AND "SERIES-B" TTL PAL DEVICES
These are the earliest PLD families manufactured by National Semiconductor. The devices are fabricated using a traditional Schottky-TTL process similar to that used in the low-power Schottky (LS) TTL logic family of standard SSI/MSI functions. The addition of Titanium-Tungsten (TiW) fuse-links to the basic circuit technology allows the logic to be configured in the field after manufacturing is complete. This is the same programming technology as used in LS TTL PROM devices.

The fuse-links used in this programming technology are also referred to as "lateral fuses". The actual programming cell consists of a transistor with a fuse element in series with its emitter (as shown in Figure 6-1). It physically consists of a path, laid down during the metallization stage of the process, which is designed to pass a limited amount of current. When a higher current is passed, the metal heats to its melting point and surface tension draws the two sides of the fuse apart, leaving no electrical connection across the fuse. While this is a reliable process, it is a one-time effect and therefore cannot be tested fully before the device is in the field. The first attempt to blow a fuse must be successful, otherwise the current passing through a partly-blown fuse will not be sufficient to blow it completely on successive attempts.

ECL PAL DEVICES
For ECL systems, high-speed PAL devices have been implemented with ECL I/Os using an oxide-isolated process known as OXISS. OXISS is a fully ion-implanted Schottky bipolar process with a 2 micron minimum feature size and two-layer metal interconnect. The ECL PAL products use the same Titanium-Tungsten lateral fuses as used in the original standard, Series-A and Series-B TTL PAL devices. The ECL PAL products are also available with both 10 KH and 100K compatibility.

More recent developments are based on National's ASPECT (Advanced Single-Poly Emitter-Coupled Technology) process. This is an oxide-isolated, self-aligned, contactless poly-emitter process which uses a single poly and two metal interconnect layers. The smaller geometries result in both lower gate power requirements and a higher device speed.

"SERIES-D/-7" TTL PAL DEVICES WITH VERTICAL FUSES
National "Series-D" PAL devices, and faster TTL PAL devices being developed at National, use a new technology offering more compact geometries and higher overall device speeds than seen in the preceding TTL PAL products. The technology used in Series-D devices is based on National Semiconductor's "FAST-Z" fully ion-implanted, isoplanar, Schottky-TTL process, similar to that used in the FAST® logic family.

Advances in programming technology have led to an improvement over the basic TiW lateral fuses used in the standard TTL PAL devices described earlier. This new technique uses a programming cell referred to as a "vertical fuse".

![Figure 6-1. Lateral Fuse Circuit](TL/L/0099-1)
Instead of a transistor and fuse-link in series, as shown in Figure 6-1, the vertical fuse cell consists of an open-base transistor connecting an input line (I) to a product line (P), as shown in Figure 6-2. Due to the high impedance of the transistor, the input line is not logically connected to the product line until the cell has been "programmed". Programming produces a short circuit through the emitter-base junction of the transistor establishing the connection. The initial state of a vertical fuse is therefore opposite that of the lateral fuse-link.

The programming mechanism is driven by Avalanche-Induced Migration (AIM). If the cell is considered a pair of back-to-back diodes, forcing a controlled current through the emitter of the cell eventually induces avalanche breakdown of the emitter-base junction. Heat generated locally causes the Aluminum/Silicon interface to reach eutectic temperature. This causes the Aluminum to diffuse through the emitter to the emitter-base junction, which causes a permanent short circuit.

There are several advantages to this approach. First, the cell can be tested during device factory screening since the cell need not be programmed to verify that it operates. A test current can allow tracing of the I-V characteristics of the connecting diode. A metallic fuse, as used in lateral fuse-links, cannot have any measurable voltage drop tested across it before it is blown. Second, programming is performed by a series of pulses of increasing strength, between which the fuse is tested to see if the connection has been made yet. This ensures a very high programming yield. A comparison of the methods of programming fuse-links and AIM vertical fuse cells is shown in Figure 6-3. The vertical fuse structure is also inherently reliable because once an adequate connection is established during programming, any degree of aluminum migration during continued operation can not adversely affect cell integrity.
The programming algorithm for the vertical fuse devices in the programming equipment compensates for the opposite initial state of vertical fuses. Therefore the same JEDEC map as for all other standard PAL devices can be used without alteration.

**E²CMOS GAL DEVICES**

Electrically-Erasable CMOS offers many advantages as a technology for PLDs. Most importantly, it offers the ability to erase and reprogram devices. This allows lower part usage, particularly at the development and prototype stages, by allowing the same device to be re-used or revised. This extends into manufacturing because the technology allows 100% factory testability without encountering the cycling difficulties or windowed packages associated with UV-based devices. 100% programming and functional yields are possible.

The power requirements of such a technology are very low when compared to standard bipolar. The technology has developed to a point where performance is comparable to standard PLDs, if not to the higher-speed parts. The low-power characteristics permit higher circuit density and higher reliability, which are particularly important in remote or power-conscious environments, such as in telecommunications.

The E²CMOS technology is under further development to allow such devices to be programmed while in circuit, which will add even more to their flexibility and usefulness in manufacturing since they can be assembled in-circuit with all other components before being configured.

**6.2 Quality and Factory Testing**

**PRODUCT RELIABILITY**

National Semiconductor implements a reliability program for all of its integrated circuits. Reliability data is available for individual parts from the local sales office. It consists of:

- New product, package and process qualifications
- Existing product, package and process change qualifications
- Existing product, package and process monitoring

Product qualification testing performed by National meets or exceeds MIL standard 883. For a more thorough discussion of product quality and reliability, refer to the National Semiconductor Reliability Handbook.

**TEST CIRCUITRY**

All standard bipolar and ECL PAL devices from National Semiconductor are fabricated with a number of test fuses and dedicated test circuitry as a part of the device. During final testing of each device, the functional paths, electrical integrity, cell programmability and the programming circuitry are all verified. The special test circuitry is accessed under non-operational modes during functional testing.

**NORMAL PLD FACTORY TEST**

Most commercial grade PLDs are available under the “A+” product enhancement program. This includes burn-in testing under bias and temperature cycling. For details of the “A+” program, refer to the “National Semiconductor A+ / B+ Product Enhancement Programs” Brochure.

The standard procedure for unprogrammed PAL devices through National Semiconductor’s factory is shown in Figure 6-4.

**FIGURE 6-4. Final Test Flow for Unprogrammed PLD**

**PRE-PROGRAMMED PLD FACTORY TEST**

As discussed earlier, National provides the service of providing devices already configured with fuse map configuration to customers in a fully-tested state. The procedure for doing this is shown in Figure 6-5.

**FIGURE 6-5. Pre-Programmed PLD Final Test Flow**
NML FACTORY TEST
For volume production, National Semiconductor offers the mask-option approach to PLD production, known as National Masked Logic (NML). The procedure for the NML process is shown in Figure 6-6.

CUSTOMER HANDLING AND TEST
PLD devices are more sensitive to handling than most other integrated circuits. Care should be exercised to prevent static buildup when handling parts, particularly CMOS devices. Handling is the primary cause of defective material. To minimize the problems with production, the number of steps during which parts are handled should be kept to an absolute minimum.

A variety of approaches on device test are available to the manufacturer of systems using PLDs. For smaller production quantities, the programming hardware used for development described in Section 5 may offer an adequate solution. As quantities become larger, some programmer vendors offer add-on auto-handler packages which can handle devices in volume.

For more extensive manufacturing flows, programs are available for most of the common IC tester systems which allow the tester to perform device programming as a part of normal device flow. Other than this, National offers pre-programmed devices as described earlier.

FIGURE 6-6. NML Final Test Flow

*1st metal fuse mask pattern
FIGURE 6-7. PAL Device Electrical Test Sequence

1For sample only
*For NML/PROGRAMMED PAL
Section 7

Application Examples
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Section 7
Application Examples*

7.1 Basic Gates
This example demonstrates how fusible logic can implement the basic inverter, AND, OR, NAND, NOR and exclusive-OR functions. The PAL12H6 is selected because it has 12 inputs and 6 outputs.

*Applications contained in this section are for illustration purposes only and National makes no representation or warranty that such applications will be suitable for the use specified without further testing or modification.
7.1 Basic Gates (Continued)

PLANTM INPUT FILE

title Basic gate
pattern GATES
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/28/1989

chip GATES PAL12H6

; pin 1 2 3 4 5 6 7 8 9 10
C D F G M N P Q I GND
; pin 11 12 13 14 15 16 17 18 19 20
J K L R O H E B A VCC

equations

B = /A
E = C * D
H = F + G
L = /I + /J + /K
O = /M * /N
R = P * /O
+ /P * Q

; end of GATES

PLANTM JEDEC FILE

PAL12H6

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<tr>
<td>5</td>
<td>M</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>N</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>P</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>Q</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>I</td>
<td>ground pin</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>com input</td>
</tr>
<tr>
<td>11</td>
<td>J</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>K</td>
<td>com input</td>
</tr>
<tr>
<td>13</td>
<td>L</td>
<td>pos, com output</td>
</tr>
<tr>
<td>14</td>
<td>R</td>
<td>pos, com output</td>
</tr>
<tr>
<td>15</td>
<td>O</td>
<td>pos, com output</td>
</tr>
<tr>
<td>16</td>
<td>H</td>
<td>pos, com output</td>
</tr>
<tr>
<td>17</td>
<td>E</td>
<td>pos, com output</td>
</tr>
<tr>
<td>18</td>
<td>B</td>
<td>pos, com output</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>com input</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>

Chip Diagram (DIP)
7.1 Basic Gates (Continued)

Inputs (0–31)

Product Terms (0–63)

FIGURE 7.1.2. PAL12H6 Logic Diagram Showing Fuse Pattern of Basic Gates Example
7.2 Basic Flip-Flops

DESCRIPTION
In the Basic Gates application on the preceding pages, each 'gate' was directly connected to an output pin. Here, the output registers of the GAL16V8 are used. A simple RS latch, a T (Toggle) flip-flop, a D flip-flop, and a JK flip-flop are incorporated into a GAL16V8 (Figure 7.2.1). Each is shown with its truth table and defining equations in Figures 7.2.2–7.2.5. Note that all 3 flip-flops have synchronous preset (PR) and clear (CLR) inputs, while the RS latch does not. Also, the RS latch is not connected to the clock input; this was done to show the versatility of the GAL16V8—with a GAL device, the user is not locked in to a specific architecture.

The CUPL design input file (Figure 7.2.6) and simulation file (Figure 7.2.7) are constructed by the designer. Each output must be given a distinct name, and any clocked circuit must be denoted with an appropriate extension (.0) in the logic equations. The simulation file is again provided for design verification.

This example has some subtle requirements that may not be apparent to the first-time user. When the RS latch is not being tested, it must remain in its latched state with the output levels specified, or with the variable N (not tested) specified instead. Also, when executing a preset or clear, remember that it will affect all flip-flops; even those not being tested will still respond. Finally, all output levels should be specified or marked with the variable N; the variable X, which indicates a 'don't care' condition, will not suffice.

![FIGURE 7.2.1. Basic Flip-Flops Pinout](image)

![FIGURE 7.2.2. RS Latch](image)

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q₀</th>
<th>Q₀⁺</th>
<th>Q₀⁻⁺</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Invalid</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Set</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Latch</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

TL/L/9991-9
7.2 Basic Flip-Flops (Continued)

\[ Q_{N+1} = PR + (\text{CLR} \cdot T \cdot Q_N) + (\text{CLR} \cdot T \cdot \overline{Q_N}) \]

\[ \overline{Q_{N+1}} = \text{CLR} + (PR \cdot T \cdot \overline{Q_N}) + (PR \cdot T \cdot Q_N) \]

**FIGURE 7.2.3. T Flip-Flop**

\[ Q_{N+1} = PR + (\text{CLR} \cdot D) \]

\[ \overline{Q_{N+1}} = \text{CLR} + (PR \cdot \overline{D}) \]

**FIGURE 7.2.4. D Flip-Flop**

\[ Q_{N+1} = PR + (\text{CLR} \cdot J \cdot Q_N) + (\text{CLR} \cdot K \cdot \overline{Q_N}) \]

\[ \overline{Q_{N+1}} = \text{CLR} + (PR \cdot J \cdot \overline{Q_N}) + (PR \cdot K \cdot Q_N) \]

**FIGURE 7.2.5. JK Flip-Flop**

<table>
<thead>
<tr>
<th>PR</th>
<th>CLR</th>
<th>T</th>
<th>QN</th>
<th>QN+1</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>Invalid</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Clear</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Hold</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Set</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PR</th>
<th>CLR</th>
<th>J</th>
<th>K</th>
<th>QN</th>
<th>QN+1</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>Invalid</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Clear</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Hold</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Set</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Toggle</td>
</tr>
</tbody>
</table>
7.2 Basic Flip-Flop (Continued)

/*******************************************************/
/* CUPL INPUT FILE */
/* Flip-flops and latches implemented in a GAL16V8 */
/* */
/*******************************************************/
PARTNO 456STX;
NAME FLIPFLOP;
REV 1;
DATE 4/11/86;
DESIGNER Joe Engineer;
COMPANY National Semiconductor;
ASSEMBLY Clock Board;
LOCATION U238;

/* RS latch */
   pin [2,3,19,18] = [S,R,QST,QSC];

/* T flip-flop */
   pin [5,17,16] = [T, QTT, QTC];

/* D flip-flop */
   pin [6,15,14] = [D, QDT, QDC];

/* JK flip-flop */
   pin [7,8,13,12] = [J,K,QJT,QJC];

/* control */
   pin [1,4,9,11] = [CLK, PR, CLR, OE];

/* logic equations */
/* RS latch */
   /* */
   QST = !S # (R & QST);
   QSC = !R # (S & QSC);

/* T flip-flop */
   QTT.D = PR # (!CLR & !T & QTT) # (!CLR & T & QTC);
   QTC.D = CLR # (!PR & !T & QTC) # (!PR & T & QTT);

/* D flip-flop */
   QDT.D = PR # (D & !CLR);
   QDC.D = CLR # (!D & !PR);

/* JK flip-flop */
   QJT.D = PR # (J & QJC & !CLR) # (!K & QJT & !CLR);
   QJC.D = CLR # (!J & QJC & !PR) # (K & QJT & !PR);

FIGURE 7.2.6. CUPL Input File
7.2 Basic Flip-Flops (Continued)

/* *************************************************************/
/* CUPL SIMULATION FILE */
/* Flip-flops and latches implemented in a GAL16V8 */
/* *************************************************************/

PARTNO 456STX;
NAME FLIPFLOP;
REV 1;
DATE 4/11/86;
DESIGNER Joe Engineer;
COMPANY National Semiconductor;
ASSEMBLY Clock Board;
LOCATION U238;

/* The Order statement specifies the layout of the vector table. */
/* n = n spaces inserted between variables. */
order: OE,%1,CLK,%2,S,R,%1,QST,QSC,%2,PR,%1,CLR,%2,
T,%1,QTT,QTC,%2,D,%1,QDT,QDC,%2,J,K,%1,QJT,QJC;

vectors:

/* RS-latch */

order:

/* T-FF */

vectors:

/* D-FF */

vectors:

/* JK-FF */

vectors:

FIGURE 7.2.7. CUPL Simulation File
7.2 Basic Flip-Flops (Continued)

FIGURE 7.2.8. GAL16V8 Logic Diagram Showing Basic Flip-Flops Pattern
7.3 Memory-Mapped I/O Address Decoder

Memory-mapped I/O is an interface technique that treats the I/O devices' physical addresses the same as memory address space. That is, no Memory-I/O decoding is required. Furthermore, most computers have more instructions to manipulate the contents of memory than they have I/O instructions. Therefore, the use of memory mapping can make I/O control much more flexible. PAL devices can be used to make memory-mapped I/O implementation easy, even if changes in memory addresses are required.

**FUNCTIONAL DESCRIPTION**

Figure 7.3.1 shows a circuit that is typical of those found in memory-mapped I/O applications. The inputs to the decode logic are the system memory address lines, AB0–ABF. The logic shown compares the address on the memory bus with the programmed comparison address. When an address on the bus matches, the corresponding I/O port enable signal is set. In conjunction with other system control signals, this enable can be used to transfer data to and from the system data bus.
7.3 Memory-Mapped I/O Address Decoder (Continued)

PAL\textsuperscript{\textregistered} DEVICE DESIGN
One PAL16L2 can be used to monitor a 16-bit address bus, fully decode addresses, and furnish enables to two ports, each of which can be anywhere within 64k of address space. Partial decoding for a larger number of ports can be done using other members of the PAL device family.

Typical logic equations for the memory-mapped I/O logic are as follows:

Port 0 = /AB0*/AB1*/AB2*AB3*AB4*AB5*AB6*/AB7
       *AB8*AB9*ABA*ABB*ABC*/ABD*/ABE*/ABF

The above example shows address decoding for memory locations IF78H and IF79H. The equation terms could be changed to accommodate any 16-bit address.
7.3 Memory-Mapped I/O Address Decoder (Continued)

**PLANT™ JEDEC FILE**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ABO</td>
<td>com input</td>
</tr>
<tr>
<td>2</td>
<td>AB1</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>AB2</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>AB3</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>AB4</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>AB5</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>AB6</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>AB7</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>AB8</td>
<td>com input</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>ground pin</td>
</tr>
<tr>
<td>11</td>
<td>AB9</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>ABA</td>
<td>com input</td>
</tr>
<tr>
<td>13</td>
<td>ABB</td>
<td>com input</td>
</tr>
<tr>
<td>14</td>
<td>ABC</td>
<td>com input</td>
</tr>
<tr>
<td>15</td>
<td>PORT1</td>
<td>neg, com output</td>
</tr>
<tr>
<td>16</td>
<td>PORT0</td>
<td>neg, com output</td>
</tr>
<tr>
<td>17</td>
<td>ABD</td>
<td>com input</td>
</tr>
<tr>
<td>18</td>
<td>ABE</td>
<td>com input</td>
</tr>
<tr>
<td>19</td>
<td>AFI</td>
<td>com input</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>

**Chip Diagram (DIP)**

![Chip Diagram](image-url)
7.3 Memory-Mapped I/O Address Decoder (Continued)

FIGURE 7.3.2. PAL16L2 Logic Diagram Showing Address Decoder Fuse Pattern
7.4 Quad 4-to-1 Multiplexer

DESCRIPTION
Widely used in computer and data communications circuits, multiplexers route one of several input banks to an output, based on the condition of select inputs. This particular version has 4 input banks, each 4-bits wide (Figure 7.4.1); therefore, two select lines are required to choose 1 of 4 inputs, as shown in the function table of Figure 7.4.2. Possible applications for our multiplexer include bus selection in a multibus computer environment, or data manipulation in an arithmetic/logic circuit.

With a total of 16 multiplexer inputs and two Select inputs, this design is well suited for the GAL20V8. The pinout chosen for this example is shown in Figure 7.4.3; actual pin placement of the multiplexer outputs is not critical since the versatility of the GAL20V8 allows the designer to choose that combination of output pins that best suits the board layout. The device was programmed using ABEL; the logic design input files are shown in Figure 7.4.4, with reduced equations shown in the document-generator file of Figure 7.4.5. The ‘fuse’ map is shown in Figure 7.4.6.

<table>
<thead>
<tr>
<th>S₁</th>
<th>S₀</th>
<th>AOUT</th>
<th>BOUT</th>
<th>COUT</th>
<th>DOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A₀</td>
<td>B₀</td>
<td>C₀</td>
<td>D₀</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>A₁</td>
<td>B₁</td>
<td>C₁</td>
<td>D₁</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A₂</td>
<td>B₂</td>
<td>C₂</td>
<td>D₂</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A₃</td>
<td>B₃</td>
<td>C₃</td>
<td>D₃</td>
</tr>
</tbody>
</table>

**FIGURE 7.4.1. Block Diagram**

**FIGURE 7.4.2. Function Table**

<table>
<thead>
<tr>
<th>S₀</th>
<th>S₁</th>
<th>B₀</th>
<th>B₁</th>
<th>B₂</th>
<th>B₃</th>
<th>AOUT</th>
<th>COUT</th>
<th>DOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A₀</td>
<td>B₀</td>
<td>C₀</td>
<td>D₀</td>
<td>GAŁ20V8</td>
<td>19</td>
<td>COUT</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>A₁</td>
<td>B₁</td>
<td>C₁</td>
<td>D₁</td>
<td>19</td>
<td>COUT</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A₂</td>
<td>B₂</td>
<td>C₂</td>
<td>D₂</td>
<td>18</td>
<td>DOUT</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A₃</td>
<td>B₃</td>
<td>C₃</td>
<td>D₃</td>
<td>18</td>
<td>DOUT</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A₀</td>
<td>B₀</td>
<td>C₀</td>
<td>D₀</td>
<td>17</td>
<td>D₃</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A₁</td>
<td>B₁</td>
<td>C₁</td>
<td>D₁</td>
<td>16</td>
<td>D₂</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>A₀</td>
<td>B₀</td>
<td>C₀</td>
<td>D₀</td>
<td>15</td>
<td>D₁</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>A₁</td>
<td>B₁</td>
<td>C₁</td>
<td>D₁</td>
<td>14</td>
<td>D₀</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>A₀</td>
<td>B₀</td>
<td>C₀</td>
<td>D₀</td>
<td>15</td>
<td>C₃</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>A₁</td>
<td>B₁</td>
<td>C₁</td>
<td>D₁</td>
<td>13</td>
<td>C₂</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 7.4.3. Pinout Diagram**
module quad_4to1_mux

title 'ABEL INPUT FILE
Quad 4 to 1 Multiplexer in a GAL20V8
National Semiconductor

April 17, 1986
Joe Eng'

"device declaration

"location keyword device declaration
U8

"pin declaration

"inputs
A0, A1, A2, A3 pin 1, 2, 3, 4;
B0, B1, B2, B3 pin 5, 6, 7, 8;
C0, C1, C2, C3 pin 9, 10, 11, 13;
D0, D1, D2, D3 pin 14, 15, 16, 17;

"outputs
Aout, Bout, Cout, Oout pin 21, 20, 19, 18;

"control
S0, S1 pin 22, 23;

equations

Aout = ( !S1 & !S0 & A0) # ( !S1 & S0 & A1) #
                 (S1 & !S0 & A2) # (S1 & S0 & A3);

Bout = ( !S1 & !S0 & B0) # ( !S1 & S0 & B1) #
                 (S1 & !S0 & B2) # (S1 & S0 & B3);

Cout = ( !S1 & !S0 & C0) # ( !S1 & S0 & C1) #
                 (S1 & !S0 & C2) # (S1 & S0 & C3);

Dout = ( !S1 & !S0 & D0) # ( !S1 & S0 & D1) #
                 (S1 & !S0 & D2) # (S1 & S0 & D3);

test_vectors

([S1, S0, A0, A1, A2, A3, B0, B1, B2, B3, C0, C1, C2, C3, D0, D1, D2, D3] ->
 [Aout, Bout, Cout, Oout])

" S S A A B B C C D D outputs
" 1 0 0 1 2 3 0 1 2 3 0 1 2 3 A B C D

[0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 1] -> [1, 0, 0, 0];
[0, 1, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 1] -> [0, 1, 0, 0];
[1, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 1] -> [0, 0, 1, 0];
[1, 1, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 1] -> [0, 0, 0, 1];

[0, 0, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 0, 1, 1] -> [1, 1, 0, 0];
[0, 1, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 0, 1, 1] -> [1, 1, 0, 1];
[1, 0, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 0, 1, 1] -> [1, 0, 1, 1];
[1, 1, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 0, 1, 1] -> [0, 1, 1, 1];

FIGURE 7.4.4. ABEL Input File
7.4 Quad 4-to-1 Multiplexer (Continued)

Reduced Equations:

Aout = (A0 & !S0 & !S1
# A1 & S0 & !S1
# A2 & !S0 & S1
# A3 & S0 & S1);

Bout = (B0 & !S0 & !S1
# B1 & S0 & !S1
# B2 & !S0 & S1
# B3 & S0 & S1);

Cout = (C0 & !S0 & !S1
# C1 & S0 & !S1
# C2 & !S0 & S1
# C3 & S0 & S1);

Dout = (D0 & !S0 & !S1
# D1 & S0 & !S1
# D2 & !S0 & S1
# D3 & S0 & S1);

FIGURE 7.4.5. Reduced ABEL Equations
7.4 Quad 4-to-1 Multiplexer (Continued)

```
OPH* 0F2706*
111111011101111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
7.5 Dual 8-to-1 Multiplexer

The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B and C. The true data is output on Y when strobed by S. The circuit is implemented using a PAL20L2.

FUNCTION TABLE

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select</td>
<td>Strobe</td>
</tr>
<tr>
<td>C B A S</td>
<td></td>
</tr>
<tr>
<td>X X X</td>
<td>H</td>
</tr>
<tr>
<td>L L L</td>
<td>L</td>
</tr>
<tr>
<td>L L H</td>
<td>L</td>
</tr>
<tr>
<td>L H L</td>
<td>L</td>
</tr>
<tr>
<td>L H H</td>
<td>L</td>
</tr>
<tr>
<td>H L L</td>
<td>L</td>
</tr>
<tr>
<td>H L H</td>
<td>L</td>
</tr>
<tr>
<td>H H L</td>
<td>L</td>
</tr>
<tr>
<td>H H H</td>
<td>L</td>
</tr>
</tbody>
</table>

Pinout
7.5 Dual 8-to-1 Multiplexer (Continued)

LOGIC DIAGRAM

Dual 8:1 Mux

Diagram of a dual 8-to-1 multiplexer with inputs A, B, C, and S, and outputs 0 to 17.
7.5 Dual 8-to-1 Multiplexer (Continued)

PLANTM INPUT FILE

title DUAL 8 to 1 multiplexer
pattern mux8t1
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/15/1989
chip mux8t1 PAL20L2

; pin 1 2 3 4 5 6 7 8 9 10 11 12
1D0 1D1 1D2 1D3 1D4 1D5 1D6 1D7 2D0 2D1 2D2 GND
; pin 13 14 15 16 17 18 19 20 21 22 23 24
2D3 2D4 2D5 2D6 2D7 2Y 1Y S C B A VCC

equations

/1Y = /100 * /C * /B * /A * /S
+ /101 * /C * /B * /A * /S
+ /1D2 * /C * B * /A * /S
+ /1D3 * /C * B * /A * /S
+ /1D4 * C * /B * /A * /S
+ /1D5 * C * /B * /A * /S
+ /1D6 * C * B * /A * /S
+ /1D7 * C * B * /A * /S

/2Y = /2D0 * /C * /B * /A * /S
+ /2D1 * /C * /B * /A * /S
+ /2D2 * /C * B * /A * /S
+ /2D3 * /C * B * /A * /S
+ /2D4 * C * /B * /A * /S
+ /2D5 * C * /B * /A * /S
+ /2D6 * C * B * /A * /S
+ /2D7 * C * B * /A * /S

; end of mux8t1
7.5 Dual 8-to-1 Multiplexer (Continued)

PLANTM JEDEC FILE

PAL20L2

title DUAL 8 to 1 multiplexer
pattern mux8t1
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/15/1989

* QF0640*QP24*FO*
L0000
11101110111011011110111111111111111111
1011110111101110111111111111111111
1111101101111101111111111111111111
1111101101110111111111111111111111
11111111111111111111111111111111
1111101111011011111111111111111111
11111011110110111111111111111111111
111111111111111111111111111111111
111111111111111111111111111111111*
L0320
1111111011101111011111111111111111
111111011110111111111111111111111
111111011110111111111111111111111
111111011110111111111111111111111
111111101110110111111111111111111
111111101110110111111111111111111
111111101110110111111111111111111
111111101110110111111111111111111*
C408E*
0000

TL/L/9991--F1
### 7.5 Dual 8-to-1 Multiplexer (Continued)

Document file for 2MUX.INP
Device: 20L2

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1D0</td>
<td>com input</td>
</tr>
<tr>
<td>2</td>
<td>1D1</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>1D2</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>1D3</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>1D4</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>1D5</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>1D6</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>1D7</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>2D0</td>
<td>com input</td>
</tr>
<tr>
<td>10</td>
<td>2D1</td>
<td>com input</td>
</tr>
<tr>
<td>11</td>
<td>2D2</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>ground pin</td>
</tr>
<tr>
<td>13</td>
<td>2D3</td>
<td>com input</td>
</tr>
<tr>
<td>14</td>
<td>2D4</td>
<td>com input</td>
</tr>
<tr>
<td>15</td>
<td>2D5</td>
<td>com input</td>
</tr>
<tr>
<td>16</td>
<td>2D6</td>
<td>com input</td>
</tr>
<tr>
<td>17</td>
<td>2D7</td>
<td>com input</td>
</tr>
<tr>
<td>18</td>
<td>2Y</td>
<td>neg, com output</td>
</tr>
<tr>
<td>19</td>
<td>1Y</td>
<td>neg, com output</td>
</tr>
<tr>
<td>20</td>
<td>S</td>
<td>com input</td>
</tr>
<tr>
<td>21</td>
<td>C</td>
<td>com input</td>
</tr>
<tr>
<td>22</td>
<td>B</td>
<td>com input</td>
</tr>
<tr>
<td>23</td>
<td>A</td>
<td>com input</td>
</tr>
<tr>
<td>24</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>

#### Chip Diagram (DIP)

```
1D0  1  24  VCC
1D1  2  23  A
1D2  3  22  B
1D3  4  21  C
1D4  5  20  S
1D5  6  19  1Y
1D6  7  18  2Y
1D7  8  17  2D7
2D0  9  16  2D6
2D1 10  15  2D5
2D2 11  14  2D4
GND 12  13  2D3
```
7.6 16-to-1 Multiplexer
The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C and D. The true data is output on Y and the inverted data on W. The circuit is implemented using a PAL20C1.

**LOGIC SYMBOL**

**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>Input Select</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>D C B A</td>
<td>W Y</td>
</tr>
<tr>
<td>L L L L</td>
<td>E0 E0</td>
</tr>
<tr>
<td>L L L H</td>
<td>E1 E1</td>
</tr>
<tr>
<td>L L H L</td>
<td>E2 E2</td>
</tr>
<tr>
<td>L L H H</td>
<td>E3 E3</td>
</tr>
<tr>
<td>L H L L</td>
<td>E4 E4</td>
</tr>
<tr>
<td>L H L H</td>
<td>E5 E5</td>
</tr>
<tr>
<td>L H H L</td>
<td>E6 E6</td>
</tr>
<tr>
<td>L H H H</td>
<td>E7 E7</td>
</tr>
<tr>
<td>H L L L</td>
<td>E8 E8</td>
</tr>
<tr>
<td>H L L H</td>
<td>E9 E9</td>
</tr>
<tr>
<td>H L H L</td>
<td>E10 E10</td>
</tr>
<tr>
<td>H L H H</td>
<td>E11 E11</td>
</tr>
<tr>
<td>H H L L</td>
<td>E12 E12</td>
</tr>
<tr>
<td>H H L H</td>
<td>E13 E13</td>
</tr>
<tr>
<td>H H H L</td>
<td>E14 E14</td>
</tr>
<tr>
<td>H H H H</td>
<td>E15 E15</td>
</tr>
</tbody>
</table>
7.6 16-to-1 Multiplexer (Continued)

LOGIC DIAGRAM

16:1 Mux
7.6 16-to-1 Multiplexer (Continued)

PLANTM INPUT FILE

title 16 to 1 multiplexer
pattern mux16T1
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/15/1989

chip mux16T1 PAL20C1

; pin 1 2 3 4 5 6 7 8 9 10 11 12
  E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 GND
; pin 13 14 15 16 17 18 19 20 21 22 23 24
  E11 E12 E13 E14 E15 W Y D C B A VCC

equations

  Y  =  E0 * /D * /C * /B * /A
      +  E1 * /D * /C * /B * /A
      +  E2 * /D * /C * /B * /A
      +  E3 * /D * /C * /B * /A
      +  E4 * /D * C * /B * /A
      +  E5 * /D * C * /B * /A
      +  E6 * /D * C * /B * /A
      +  E7 * /D * C * /B * /A
      +  E8 * D * /C * /B * /A
      +  E9 * D * /C * /B * /A
      +  E10* D * /C * /B * /A
      +  E11* D * /C * /B * /A
      +  E12* D * C * /B * /A
      +  E13* D * C * /B * /A
      +  E14* D * C * /B * /A
      +  E15* D * C * /B * /A

; end of mux16T1
7.6  16-to-1 Multiplexer (Continued)

PLANT™ JEDEC FILE

PAL20C1
title  16 to 1 multiplexer
pattern mux16T1
revision A
author  Tarif Engineer
company National Semiconductor Corporation
Date  11/15/1989

*QF0660*QP24*F0*
L0000
11011110111101111111111111111111111111111111111
0111110111110111111111111111111111111111111111
1111101011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
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1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
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1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
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1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
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1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
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1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
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1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
1111111011111011111111111111111111111111111111
### 16-to-1 Multiplexer (Continued)

Document file for MUX16T1  
Device: 20C1

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>E0</td>
<td>com input</td>
</tr>
<tr>
<td>2</td>
<td>E1</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>E2</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>E3</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>E4</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>E5</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>E6</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>E7</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>E8</td>
<td>com input</td>
</tr>
<tr>
<td>10</td>
<td>E9</td>
<td>com input</td>
</tr>
<tr>
<td>11</td>
<td>E10</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>ground pin</td>
</tr>
<tr>
<td>13</td>
<td>E11</td>
<td>com input</td>
</tr>
<tr>
<td>14</td>
<td>E12</td>
<td>com input</td>
</tr>
<tr>
<td>15</td>
<td>E13</td>
<td>com input</td>
</tr>
<tr>
<td>16</td>
<td>E14</td>
<td>com input</td>
</tr>
<tr>
<td>17</td>
<td>E15</td>
<td>com input</td>
</tr>
<tr>
<td>18</td>
<td>W</td>
<td>unused</td>
</tr>
<tr>
<td>19</td>
<td>Y</td>
<td>pos, com output</td>
</tr>
<tr>
<td>20</td>
<td>D</td>
<td>com input</td>
</tr>
<tr>
<td>21</td>
<td>C</td>
<td>com input</td>
</tr>
<tr>
<td>22</td>
<td>B</td>
<td>com input</td>
</tr>
<tr>
<td>23</td>
<td>A</td>
<td>com input</td>
</tr>
<tr>
<td>24</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>

**Chip Diagram (DIP)**

```
EO     1  24  VCC
E1     2  23  A
E2     3  22  B
E3     4  21  C
E4     5  20  D
E5     6  19  Y
E6     7  18  W
E7     8  17  E15
E8     9  16  E14
E9    10  15  E13
E10   11  14  E12
GND  12  13  E11
```

TL/L/9991-F5

TL/L/9991-S4
7.7 7-Bit Counter with Parallel Load

DESCRIPTION
In this example, a GAL20V8 implements a seven-bit counter with asynchronous carry-out and load functions. As illustrated in the block diagram (Figure 7.7.1) and pinout diagram (Figure 7.7.2), the carry-in and carry-out pins make the counter fully cascaddable to form larger counters. The CUPL design input files are shown in Figure 7.7.3, and simulation files in Figure 7.7.4. Note that the counter requires seven registers and one asynchronous output, taking full advantage of the generic architecture of the GAL20V8.

FIGURE 7.7.1. Block Diagram

FIGURE 7.7.2. Pinout Diagram

TL/L/9991-37

CLK  1  24  VCC
D0  2  23  CARRY IN
D1  3  22  Q0
D2  4  21  Q1
D3  5  20  Q2
D4  6  19  Q3
D5  7  18  Q4
D6  8  17  Q5
LOAD  9  16  Q6
CLEAR  10  15  CARRY OUT
OE  11  14
GND  12  13  OE
7.7 7-Bit Counter with Parallel Load (Continued)

`/*----------------------------------------------------------------------*/
/*
/* CUPL INPUT FILE
/* DESIGN INPUT FOR 7-BIT COUNTER
/*
/*----------------------------------------------------------------------*/
/* ALLOWABLE TARGET DEVICE: GAL20V8
/*----------------------------------------------------------------------*/
PARTNO  7BITCNT ;
NAME  7-BIT COUNTER ;
REV  01 ;
DATE  10/08/85 ;
DESIGNER  Joe Engineer;
COMPANY  National Semiconductor;
ASSEMBLY  3A-27 ;
LOCATION  U06 ;

PIN 1 = CLK ; /* CLOCK INPUT */
PIN 2 = D0 ; /* DATA0 INPUT */
PIN 3 = D1 ; /* DATA1 INPUT */
PIN 4 = D2 ; /* DATA2 INPUT */
PIN 5 = D3 ; /* DATA3 INPUT */
PIN 6 = D4 ; /* DATA4 INPUT */
PIN 7 = D5 ; /* DATA5 INPUT */
PIN 8 = D6 ; /* DATA6 INPUT */
PIN 9 = LD ; /* LOAD CONTROL */
PIN 10 = CLEAR; /* ASYNCHRONOUS CARRY-IN */
PIN 13 = !OE ; /* OUTPUT ENABLE */
PIN 15 = CARRYOUT ;
PIN 16 = Q6 ; /* COUNTER MSB */
PIN 17 = Q5 ;
PIN 18 = Q4 ;
PIN 19 = Q3 ;
PIN 20 = Q2 ;
PIN 21 = Q1 ;
PIN 22 = Q0 ; /* COUNTER LSB */
PIN 23 = CARRYIN ; /* CARRY-IN FOR CASCADING */

FIGURE 7.7.3. CUPL Design Input File

TL/L/9991-39"
7.7 7-Bit Counter with Parallel Load (Continued)

Q0.D = (LD & D0)
# !LD & !Q0 & CARRYIN) & !CLEAR; /* LOAD D0 */
# !LD & !Q0 & CARRYIN) & !CLEAR; /* TOGGLE */

Q1.D = (LD & D1)
# !LD & !Q1 & Q0 & CARRYIN /* LOAD D1 */
# !LD & !Q1 & Q0 & CARRYIN /* TOGGLE */
# !LD & !Q1 & Q0 & CARRYIN /* HOLD */

Q2.D = (LD & D2)
# !LD & !Q2 & Q1 & Q0 & CARRYIN /* LOAD D2 */
# !LD & !Q2 & Q1 & Q0 & CARRYIN /* TOGGLE */
# !LD & !Q2 & Q1 & Q0 & CARRYIN /* HOLD */
# !LD & !Q2 & Q1 & Q0 & CARRYIN /* HOLD */

Q3.D = (LD & D3)
# !LD & !Q3 & Q2 & Q1 & Q0 & CARRYIN /* LOAD D3 */
# !LD & !Q3 & Q2 & Q1 & Q0 & CARRYIN /* TOGGLE */
# !LD & !Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */
# !LD & !Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */

Q4.D = (LD & D4)
# !LD & !Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* LOAD D4 */
# !LD & !Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* TOGGLE */
# !LD & !Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */
# !LD & !Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */

Q5.D = (LD & D5)
# !LD & !Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* LOAD D5 */
# !LD & !Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* TOGGLE */
# !LD & !Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */
# !LD & !Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */

Q6.D = (LD & D6)
# !LD & !Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* LOAD D6 */
# !LD & !Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* TOGGLE */
# !LD & !Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */
# !LD & !Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN /* HOLD */

CARRYOUT = !LD & Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0 & CARRYIN; /* CARRY-OUT */

FIGURE 7.7.3. CUPL Design Input File (Continued)
7.7 7-Bit Counter with Parallel Load (Continued)

//****************************************************************************
//CUPL INPUT FILE
//SIMULATION FOR 7-BIT COUNTER
//****************************************************************************
//ALLOWABLE TARGET DEVICE: GAL20V8
//****************************************************************************
PARTNO 7BITCNT
NAME 7-BIT COUNTER
REV 01
DATE 10/08/85
DESIGNER Joe Engineer
COMPANY National Semiconductor
ASSEMBLY 3A-27
LOCATION U06

ORDER:
CLK, IOE, CLEAR, LD, CARRYIN, D6, D5, D4, D3, D2, D1, D0, Q6, Q5, Q4, Q3, Q2, Q1, Q0, CARRYOUT

VECTORS:
$mg"  C ";
$mg"  C ! C C D ";
$mg"  L O L I DDDDDDD QQQQQQ U ";
$mg"  K E R D N 6543210 6543210 T ";
$mg"  ";
0 1 X X X XXXXXXX ZZZZZZZ X /* TEST HI-2 */
C 0 1 X X XXXXXXX LLLLLLL L /* TEST CLEAR */
C 0 0 1 X 1111111 HHHHHHH L /* LOAD ONES */
C 0 0 0 1 X 0000000 LLLLLLL L /* LOAD ZEROS */
C 0 0 0 0 1 XXXXXXX LLLLHHH L /* COUNT=1 */
C 0 0 0 0 1 XXXXXXX LLLLLLL L /* COUNT=2 */
C 0 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=3 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=4 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=5 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=6 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=7 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=8 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=9 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=10 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=11 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=12 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=13 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=14 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=15 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=16 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=17 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=18 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=19 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=20 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=21 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=22 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=23 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=24 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=25 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=26 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=27 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=28 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=29 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=30 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=31 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=32 */
C 0 0 0 1 XXXXXXX LLLLLLLL L /* COUNT=33 */
C 0 0 0 1 X 0111111 LHHHHHHH L /* LOAD=63 TO OBSERVE MSB TOGGLE */
C 0 0 0 1 X 0000000 HHHHHHHH L /* COUNT=64, OBSERVE MSB */
C 0 0 0 1 X 0000000 HHHHHHHH L /* COUNT=65, OBSERVE MSB */
C 0 0 0 1 X 1111111 HHHHHHHH L /* LOAD=126 TO OBSERVE CARRY */
C 0 0 0 1 XXXXXXX HHHHHHHH L /* COUNT=127, OBSERVE CARRY */
C 0 0 0 1 XXXXXXX HHHHHHHH L /* COUNT=0, OBSERVE CARRY */

FIGURE 7.7.4. CUPL Simulation File
7.8 10-Bit Up/Down Counter

The ten-bit up/down counter can count up, count down, set all output to high, disable the output (high impedance), and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the rising edge of the clock. SET overrides LOAD, CNT and HOLD. LOAD overrides CNT and HOLD. CIN enable counting operation or hold it. CNT Up or Down depend on UP signal.

All outputs are enabled when OE is low, otherwise HIGH-Z. This circuit is implemented using a PAL20X10, with the exclusive-or function the PAL20X10 facilitates design of counter and state sequences with minimum propagation delay. The PAL20X10 offers an efficient means of implementing counters. Normal PAL & PLA implementation would require addition terms for the XOR functions. Having 10 output the PAL20X10 supersedes 20 and 24 medium PAL’s in this specific application. On power up all registers are reset to simplify sequential circuit design.

LOGIC SYMBOL

FUNCTION TABLE

<table>
<thead>
<tr>
<th>OE</th>
<th>CK</th>
<th>SET</th>
<th>LD</th>
<th>CNT</th>
<th>CIN</th>
<th>UP</th>
<th>D9–D0</th>
<th>Q9–Q0</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td></td>
<td>Hi-Z</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td></td>
<td>Set all HIGH</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>D</td>
<td>D</td>
<td>LOAD D</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td></td>
<td>HOLD</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>Q</td>
<td></td>
<td>HOLD</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Q plus 1</td>
<td></td>
<td>Count UP</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Q minus 1</td>
<td></td>
<td>Count DN</td>
</tr>
</tbody>
</table>

Pinout

TL/L/9991–51
7.8 10-Bit Up/Down Counter (Continued)

LOGIC DIAGRAM
7.8 10-Bit Up/Down Counter (Continued)

PLANT™ INPUT FILE

title 10-BIT SYNCHRONOUS UP/DOWN COUNTER
pattern COUNTER
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/17/1989
chip COUNTER PAL20X10
; pin 1 2 3 4 5 6 7 8 9 10 11 12
  CLK D0 D1 D2 D7 /LD /CNT /UP SET D8 /CIN 09 GND
; pin 13 14 15 16 17 18 19 20 21 22 23 24
  /OE 09 08 07 06 05 04 03 02 01 00 VCC
equations
/00 := /00*LD */SET
  + /LD*/SET*/D0
  $ LD */CIN*/SET*/CNT*/UP
  + LD */CIN*/SET*/CNT*/UP

/01 := /01*LD */SET
  + /LD*/SET*/D1
  $ LD */CIN*/SET*/CNT*/UP */00
  + LD */CIN*/SET*/CNT*/UP* 00

/02 := /02*LD */SET
  + /LD*/SET*/D2 D7
  $ LD */CIN*/SET*/CNT*/UP */01*/00
  + LD */CIN*/SET*/CNT*/UP* 01* 00

/03 := /03*LD */SET
  + /LD*/SET*/D2 D7
  $ LD */CIN*/SET*/CNT*/UP */02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 02* 01* 00

/04 := /04*LD */SET
  + /LD*/SET*/D2 D7
  $ LD */CIN*/SET*/CNT*/UP */03*/02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 03* 02* 01* 00

/05 := /05*LD */SET
  + /LD*/SET*/D2 D7
  $ LD */CIN*/SET*/CNT*/UP */04*/03*/02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 04* 03* 02* 01* 00

/06 := /06*LD */SET
  + /LD*/SET*/D2 D7
  $ LD */CIN*/SET*/CNT*/UP */05*/04*/03*/02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 05* 04* 03* 02* 01* 00

/07 := /07*LD */SET
  + /LD*/SET*/D2 D7
  $ LD */CIN*/SET*/CNT*/UP */06*/05*/04*/03*/02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 06* 05* 04* 03* 02* 01* 00

/08 := /08*LD */SET
  + /LD*/SET*/D8
  $ LD */CIN*/SET*/CNT*/UP */07*/06*/05*/04*/03*/02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 07* 06* 05* 04* 03* 02* 01* 00

/09 := /09*LD */SET
  + /LD*/SET*/D9
  $ LD */CIN*/SET*/CNT*/UP */08*/07*/06*/05*/04*/03*/02*/01*/00
  + LD */CIN*/SET*/CNT*/UP* 08* 07* 06* 05* 04* 03* 02* 01* 00

TL/L/9991-F6
7.8 10-Bit Up/Down Counter

Title: 10-BIT SYNCHRONOUS UP/DOWN COUNTER
Pattern: COUNTER
Revision: A
Author: Tarif Engineer
Company: National Semiconductor Corporation
Date: 11/17/1989

PAL20X10

QF1600*QP24*F0*
L0000
11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
# 7.8 8-Bit Cascadable Shift Register

Document file for CNT10B.INP
Device: 20X10

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CLK</td>
<td>clock pin</td>
</tr>
<tr>
<td>2</td>
<td>DO</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>D1</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>D2D7</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>LD</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>CNT</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>UP</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>SET</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>D8</td>
<td>com input</td>
</tr>
<tr>
<td>10</td>
<td>CIN</td>
<td>com input</td>
</tr>
<tr>
<td>11</td>
<td>D9</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>ground pin</td>
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<tr>
<td>13</td>
<td>OE</td>
<td>enable pin</td>
</tr>
<tr>
<td>14</td>
<td>Q9</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>15</td>
<td>Q8</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>16</td>
<td>Q7</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>17</td>
<td>Q6</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>18</td>
<td>Q5</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>19</td>
<td>Q4</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>20</td>
<td>Q3</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>21</td>
<td>Q2</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>22</td>
<td>Q1</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>23</td>
<td>Q0</td>
<td>neg, reg, xor feedback</td>
</tr>
<tr>
<td>24</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>

**Chip Diagram (DIP)**

```
CLK   1  24 VCC
DO    2  23 Q0
D1    3  22 Q1
D2D7  4  21 Q2
LD    5  20 Q3
CNT   6  19 Q4
UP    7  18 Q5
SET   8  17 Q6
D8    9  16 Q7
CIN   10 15 Q8
D9    11 14 Q9
GND   12 13 OE
```
### 7.9 8-Bit Equality Comparator

The equality comparator takes two 8-bit data words as inputs and produces one combinatorial output (EQ) which becomes active when the two input words match. Due to the large number of product terms required to implement this function, a PAL16C1 is the appropriate device to use. The complement output (NE) is also provided.

**PINOUT**

<table>
<thead>
<tr>
<th>Pin</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A0</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>7</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A6</td>
<td>8</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A7</td>
<td>9</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LOGIC DIAGRAM**

Note: To express this function in the sum-of-products form required by the PAL16C1, it is necessary to apply the identity function
\[ X \oplus Y = XY + \overline{X}Y \]
as well as DeMorgan's Theorem
\[ \overline{X} + \overline{Y} = \overline{X + Y} \]
to the above logic definition.

**PLAN™ INPUT FILE**

```plaintext
title 8 bit comparator
pattern com8b
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/28/1989

chip com8b PAL16c1

; pin 1 2 3 4 5 6 7 8 9 10 11 12
B0 A0 A1 A2 A3 A4 A5 A6 A7 GND
; pin 11 12 13 14 15 16 17 18 19 20
B7 B6 B5 B4 EQ NEQ B3 B2 B1 VCC

equations

\[
\text{NEQ} = A0 \times /B0 + /A0 \times B0 \\
+ A1 \times /B1 + /A1 \times B1 \\
+ A2 \times /B2 + /A2 \times B2 \\
+ A3 \times /B3 + /A3 \times B3 \\
+ A4 \times /B4 + /A4 \times B4 \\
+ A5 \times /B5 + /A5 \times B5 \\
+ A6 \times /B6 + /A6 \times B6 \\
+ A7 \times /B7 + /A7 \times B7
\]

; end of com8b
```
7.9 8-Bit Equality Comparator (Continued)

PLANT™ JEDEC FILE

PAL16C1

title 8 bit comparator

pattern com8b

revision A

author Tarif Engineer

company National Semiconductor Corporation

Date 11/28/1989

* QFO512*QP20*FO* 

L0000

01101111111111111111111111111111
10011111111111111111111111111111
11110110111111111111111111111111
11111001111111111111111111111111
11111101101111111111111111111111
11111110011111111111111111111111
11111111001111111111111111111111
11111111101101111111111111111111
11111111110101111111111111111111
11111111111001111111111111111111
11111111111110011111111111111111
11111111111111011011111111111111
11111111111111100111111111111111
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11111111111111111111100111111111
11111111111111111111111001111111
11111111111111111111111101111111
11111111111111111111111110111111
11111111111111111111111111101111
11111111111111111111111111110111
11111111111111111111111111111011
11111111111111111111111111111101
11111111111111111111111111111110
C3BC4* 

0000
Chip Diagram (DIP)
Document file for CMRBB.INP
Device: 16C1

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>B0</td>
<td>com input</td>
</tr>
<tr>
<td>2</td>
<td>A0</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>A1</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>A2</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>A3</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>A4</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>A5</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>A6</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>A7</td>
<td>com input</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>ground pin</td>
</tr>
<tr>
<td>11</td>
<td>B7</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>B6</td>
<td>com input</td>
</tr>
<tr>
<td>13</td>
<td>B5</td>
<td>com input</td>
</tr>
<tr>
<td>14</td>
<td>B4</td>
<td>com input</td>
</tr>
<tr>
<td>15</td>
<td>EQ</td>
<td>unused</td>
</tr>
<tr>
<td>16</td>
<td>NEQ</td>
<td>pos, com output</td>
</tr>
<tr>
<td>17</td>
<td>B3</td>
<td>com input</td>
</tr>
<tr>
<td>18</td>
<td>B2</td>
<td>com input</td>
</tr>
<tr>
<td>19</td>
<td>B1</td>
<td>com input</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>
7.10 8-Bit Barrel Shifter

DESCRIPTION

The barrel shifter (Figure 7.10.1) is a specialized shift register that rotates data a selectable number of bit positions out of the most-significant bit and back into the least-significant bit—thus the name. Typical applications of a barrel shifter are floating-point arithmetic and display rotation on a graphics terminal.

Since our barrel shifter has 8 data inputs and 8 registered outputs, as well as control signals, the GAL20V8 is the PLD of choice. The shift-select inputs (S₀, S₁, S₂) determine the number of positions shifted, as described in the function table of Figure 7.10.2. The block diagram is shown in Figure 7.10.3, and the pinout in Figure 7.10.4. The clock (CLK) input gates input data synchronously to the output registers, and the output enable (OE) allows TRI-STATE® buffering of the Q outputs. The one remaining input is used for a reset (RS) function.

The ABEL design input files shown in Figure 7.10.5 may appear tedious, but simply enumerate the eight different bit-shift possibilities for each output.

FIGURE 7.10.1. Barrel Shift Rotation

<table>
<thead>
<tr>
<th>S₂</th>
<th>S₁</th>
<th>S₀</th>
<th>Q₇</th>
<th>Q₆</th>
<th>Q₅</th>
<th>Q₄</th>
<th>Q₃</th>
<th>Q₂</th>
<th>Q₁</th>
<th>Q₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
</tr>
<tr>
<td>0 0 1</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
</tr>
<tr>
<td>0 1 0</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
</tr>
<tr>
<td>0 1 1</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
</tr>
<tr>
<td>1 0 0</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
</tr>
<tr>
<td>1 0 1</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
</tr>
<tr>
<td>1 1 0</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
</tr>
<tr>
<td>1 1 1</td>
<td>D₀</td>
<td>D₇</td>
<td>D₆</td>
<td>D₅</td>
<td>D₄</td>
<td>D₃</td>
<td>D₂</td>
<td>D₁</td>
<td>D₀</td>
<td>D₇</td>
</tr>
</tbody>
</table>

FIGURE 7.10.2. Function Table

FIGURE 7.10.3. Block Diagram

FIGURE 7.10.4. Pinout Diagram
module barrel_shifter_8;

title 'ABEL INPUT FILE
8-bit Barrel Shifter in a GAL20V8
National Semiconductor

April 16, 1986
Joe Eng'

"device declaration

"location keyword device code
U9 device 'P20V8R' ;

"pin declaration

"inputs
D7,D6,D5,D4,D3,D2,D1,D0 pin 4,5,6,7,8,9,10,11;
CLK pin 1;

"outputs
Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0 pin 22,21,20,19,18,17,16,15;

"control
S2,S1,S0 pin 23,2,3; " selects 0-7 bit shift
RS pin 14;  " resets all outputs to 0
OE pin 13; " output enable

"constant declaration

X = .X.; " simplify 'don't care' constant
C = .C.; " simplify 'clock' constant

FIGURE 7.10.5. ABEL Input File
7.10 8-Bit Barrel Shifter (Continued)

equations

\[ Q_0 := \neg RS \land ((\neg S_2 \land \neg S_1 \land \neg S_0 \land D_0) \land (\neg S_2 \land \neg S_1 \land S_0 \land D_7) \land (\neg S_2 \land S_1 \land \neg S_0 \land D_6) \land (S_2 \land \neg S_1 \land \neg S_0 \land D_4) \land (S_2 \land \neg S_1 \land S_0 \land D_3) \land (S_2 \land S_1 \land \neg S_0 \land D_2) \land (S_2 \land S_1 \land S_0 \land D_1)) ; \]

\[ Q_1 := \neg RS \land ((\neg S_2 \land \neg S_1 \land \neg S_0 \land D_1) \land (\neg S_2 \land \neg S_1 \land S_0 \land D_0) \land (\neg S_2 \land S_1 \land \neg S_0 \land D_7) \land (S_2 \land \neg S_1 \land \neg S_0 \land D_6) \land (S_2 \land \neg S_1 \land S_0 \land D_4) \land (S_2 \land S_1 \land \neg S_0 \land D_3) \land (S_2 \land S_1 \land S_0 \land D_2)) ; \]

\[ Q_2 := \neg RS \land ((\neg S_2 \land \neg S_1 \land \neg S_0 \land D_2) \land (\neg S_2 \land \neg S_1 \land S_0 \land D_1) \land (\neg S_2 \land S_1 \land \neg S_0 \land D_0) \land (S_2 \land \neg S_1 \land \neg S_0 \land D_7) \land (S_2 \land \neg S_1 \land S_0 \land D_6) \land (S_2 \land S_1 \land \neg S_0 \land D_3) \land (S_2 \land S_1 \land S_0 \land D_2)) ; \]

\[ Q_3 := \neg RS \land ((\neg S_2 \land \neg S_1 \land \neg S_0 \land D_3) \land (\neg S_2 \land \neg S_1 \land S_0 \land D_2) \land (\neg S_2 \land S_1 \land \neg S_0 \land D_1) \land (\neg S_2 \land S_1 \land S_0 \land D_0) \land (S_2 \land \neg S_1 \land \neg S_0 \land D_7) \land (S_2 \land \neg S_1 \land S_0 \land D_6) \land (S_2 \land S_1 \land \neg S_0 \land D_3) \land (S_2 \land S_1 \land S_0 \land D_2)) ; \]

\[ Q_4 := \neg RS \land ((\neg S_2 \land \neg S_1 \land \neg S_0 \land D_4) \land (\neg S_2 \land \neg S_1 \land S_0 \land D_3) \land (\neg S_2 \land S_1 \land \neg S_0 \land D_2) \land (\neg S_2 \land S_1 \land S_0 \land D_1) \land (S_2 \land \neg S_1 \land \neg S_0 \land D_0) \land (S_2 \land \neg S_1 \land S_0 \land D_7) \land (S_2 \land S_1 \land \neg S_0 \land D_6) \land (S_2 \land S_1 \land S_0 \land D_5)) ; \]

FIGURE 7.10.5. ABEL Input File (Continued)
7.10 8-Bit Barrel Shifter (Continued)

\[
Q5 := \text{IR5 & } ((\text{IS2 & IS1 & IS0 & D5}) \# \\
(\text{IS2 & IS1 & IS0 & D4}) \# \\
(\text{IS2 & S1 & IS0 & D3}) \# \\
(\text{IS2 & S1 & IS0 & D2}) \# \\
(\text{S2 & IS1 & IS0 & D1}) \# \\
(\text{S2 & S1 & IS0 & D0}) \# \\
(\text{S2 & S1 & IS0 & D6}));
\]

\[
Q6 := \text{IR5 & } ((\text{IS2 & IS1 & IS0 & D6}) \# \\
(\text{IS2 & IS1 & IS0 & D5}) \# \\
(\text{IS2 & S1 & IS0 & D4}) \# \\
(\text{IS2 & S1 & IS0 & D3}) \# \\
(\text{S2 & IS1 & IS0 & D2}) \# \\
(\text{S2 & S1 & IS0 & D1}) \# \\
(\text{S2 & S1 & IS0 & D0}));
\]

\[
Q7 := \text{IR5 & } ((\text{IS2 & IS1 & IS0 & D7}) \# \\
(\text{IS2 & IS1 & IS0 & D6}) \# \\
(\text{IS2 & S1 & IS0 & D5}) \# \\
(\text{IS2 & S1 & IS0 & D4}) \# \\
(\text{S2 & IS1 & IS0 & D3}) \# \\
(\text{S2 & S1 & IS0 & D2}) \# \\
(\text{S2 & S1 & IS0 & D0}));
\]

test_vectors ( [CLK, OE, RS, S2, S1, S0, D7..D0] \rightarrow [Q7..Q0])

end barrel_shifter_8

FIGURE 7.10.5. ABEL Input File (Continued)
7.11 Hexadecimal 7-Segment Display Encoder

The increasing use of microcomputers has led to an increased need to display numbers in hexadecimal format (0–9, A–F). Standard drivers for this function are not available, so most applications are forced to use several packages to decode each digit of the display. Since 6 to 12 digits are often being displayed, this approach can become very expensive. This example demonstrates how the hexadecimal display format can be both decoded and the LED indicators driven using a single PAL for each digit of the display.

FUNCTIONAL DESCRIPTION

A hex decoder/lamp driver accepts a four-bit hex digit, converts it to its corresponding seven-segment display code, and activates the appropriate segments on the display. These drivers can be used in both direct-drive and multiplexed display applications. A single PAL can provide both the basic decode/drive functions, and additional useful features as well.

GENERAL DESCRIPTION

Figure 7.11.1 shows three digits of a display system that uses three PALs to implement the complete decoding and display-driving functions. The inputs to each section are a hex code on pins D0–D3, a ripple blanking signal, an intensity control signal, and a lamp test signal.

The hex codes are decoded to form the seven-segment patterns shown in Table 7.11.1. The input codes, digit represented, and segments driven are as follows:

<table>
<thead>
<tr>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Digit</th>
<th>Segments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>0</td>
<td>ABCDEF</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>1</td>
<td>BC</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>2</td>
<td>ABDEG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>3</td>
<td>ABCDG</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>4</td>
<td>BCFG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>5</td>
<td>ACDFG</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>6</td>
<td>ACDEFG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>7</td>
<td>ABC</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>8</td>
<td>ABCDEFG</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>9</td>
<td>ABCDFG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>A</td>
<td>ABCEFG</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>B</td>
<td>COEFG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>C</td>
<td>ADEF</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>D</td>
<td>BCDEFG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>E</td>
<td>ADEFG</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>F</td>
<td>AEFG</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Ripple-blanking input RBI is used to suppress leading zeroes in the display. The signal is propagated from the most significant digit to the least significant digit. If the digit input is zero and RBI is low (indicating that the previous digit is also zero), all segments are left blank and this digit position's ripple-blanking output RBO is set low.

Intensity control signal IC controls the duty cycle of the display driver. When IC is high, all segment drivers are turned off. Pulsing this pin with a duty-cycled signal allows the adjustment of the display's apparent brightness.

Lamp test signal LT lets you check to see if all LED segments are energized.

PAL Device Implementation

the PAL16L8 has both the required I/O pins and the drive current capability to perform as the complete display decoder-driver circuit with seven inputs and eight outputs. The logic equations for this circuit are shown in the listing. One PAL device drives each digit; they may be cascaded without limit. With minor changes, the same logical structure could be used with multiplexer logic to allow a single PAL device to decode and drive multiple digits.
7.11 Hexadecimal 7-Segment Display Encoder (Continued)

THREE STAGE HEXADECIMAL DECODER /DRIVER

PALS8
BCD TO HEXADECIMAL
DECODER/SEGMENT
DRIVER WITH RIPPLE BLANKING

DISPLAY
LEADING
ZEROS

BLANK
LEADING
ZEROS

HEXADECIMAL
INPUTS

INTENSITY
OFF
ON
ON
OFF

LAMP TEST

TO NEXT STAGE

FIGURE 7.11.1. Hex Display Decoder-Driver Combinational Logic Diagram
7.11 Hexadecimal 7-Segment Display Encoder (Continued)

title 7-segment display encoder
pattern ENC
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/28/1989

chip ENC PAL16L8

; pin 1  2  3  4  5  6  7  8  9  10
/R0 0  D0  D1  D2  D3  IC  LT  NC  NC  NC
; pin 11 12 13 14 15 16 17 18 19 20
NC G /R0 F E D C B A VCC

equations
/A  =  /R0  *  /D0  *  /D2  
    +  /R0  *  /D3  
    +  /R0  *  D1  *  D2  
    +  /R0  *  D1  *  D2  *  /D3  
    +  /R0  *  D0  *  D2  *  /D3  
    +  /R0  *  D0  *  D2  *  D3  +  LT  
A.TRST  =  /IC

/B  =  /R0  *  /D2  *  /D3  
    +  /R0  *  /D0  *  /D2  
    +  /R0  *  /D0  *  /D2  *  /D3  
    +  /R0  *  D0  *  D1  *  /D3  
    +  /R0  *  D0  *  D1  *  D3  +  LT  
B.TRST  =  /IC

/C  =  /R0  *  D0  *  /D1  
    +  /R0  *  D0  *  /D2  
    +  /R0  *  /D1  *  /D2  
    +  /R0  *  /D2  *  /D3  
    +  /R0  *  /D2  *  D3  +  LT  
C.TRST  =  /IC

/D  =  /R0  *  /D1  *  D3  
    +  /R0  *  /D0  *  /D2  *  /D3  
    +  /R0  *  D0  *  D1  *  /D2  
    +  /R0  *  /D0  *  D1  *  D2  
    +  /R0  *  D0  *  D2  *  D3  +  LT  
D.TRST  =  /IC

/E  =  /R0  *  /D0  *  /D2  
    +  /R0  *  /D2  *  D3  
    +  /R0  *  /D0  *  D1  
    +  /R0  *  D1  *  D3  
E.TRST  =  /IC

/F  =  /R0  *  /D0  *  /D1  
    +  /R0  *  /D2  *  D3  
    +  /R0  *  D1  *  D3  
    +  /R0  *  /D0  *  D2  
    +  /R0  *  /D1  *  D2  *  /D3  +  LT  
F.TRST  =  /IC

/G  =  /R0  *  D1  *  /D2  
    +  /R0  *  D0  *  D3  
    +  /R0  *  /D2  *  D3  
    +  /R0  *  D0  *  D1  
    +  /R0  *  /D1  *  D2  *  /D3  +  LT  
G.TRST  =  /IC

/R0  =  /D0  *  /D1  *  /D2  *  /D3  *  /R0  
/R0.TRST  =  VCC

; end of ENC

TL/L/9991-G4
7.11 Hexadecimal 7-Segment Display Encoder (Continued)

PAL 16L8

Title: 7-segment display encoder
Pattern: ENC

Author: Tarif Engineer
Company: National Semiconductor Corporation
Date: 11/28/1989

L0000

11111111111111111011111111111111
101111110111111111111111011111
10111111111111111111111111011111
11110111111111111111111111111111
11110111111111111111111111111111
01111111011111111111111111111111
11111011101111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
00000000000000000000000000000000*

L0256

11111111111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
00000000000000000000000000000000*

L0512

11111111111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
00000000000000000000000000000000*

L0768

11111111111111111111111111111111
11111011111111111111111111111111
11111111111111111111111111111111
11111111111111111111111111111111
10111111111111111111111111111111
00000000000000000000000000000000*
### 7.11 Hexadecimal 7-Segment Display Encoder (Continued)

Device: 16L8

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RBI</td>
<td>com input</td>
</tr>
<tr>
<td>2</td>
<td>D0</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>D1</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>D2</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>D3</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>IC</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>LT</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>unused</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>unused</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>ground pin</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td>unused</td>
</tr>
<tr>
<td>12</td>
<td>G</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>13</td>
<td>RB0</td>
<td>neg, trst, com feedback</td>
</tr>
<tr>
<td>14</td>
<td>F</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>15</td>
<td>E</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>16</td>
<td>D</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>17</td>
<td>C</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>18</td>
<td>B</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>19</td>
<td>A</td>
<td>neg, trst, com output</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>

**Chip Diagram (DIP)**

```
RBI  1  19  A
D0   2  18  B
D1   3  17  C
D2   4  16  D
D3   5  15  E
IC   6  14  F
LT   7  13  RB0
NC   8  12  G
NC   9  11  NC
GND  10  VCC
```
7.11 Hexadecimal 7-Segment Display Encoder (Continued)

FIGURE 7.11.2. PAL16L8 Logic Diagram Showing Lamp Driver Pattern
7.12 Dual-Port RAM Controller

DESCRIPTION
As an example of the speed and architectural flexibility of the GAL16V8, a dual-port, dynamic-RAM controller capable of controlling four banks of DRAMs is implemented. The design, whose block diagram is shown in Figure 7.12.1 and state diagrams in Figures 7.12.2 and 7.12.3, requires two GAL16V8 devices. The CUPL input listings for each device are shown in Figures 7.12.4 and 7.12.6, with respective simulation files shown in Figures 7.12.5 and 7.12.7.

The first device, the Controller, is primarily responsible for maintaining the state of the entire circuit. As shown by its state diagram in Figure 7.12.2, the Controller normally resides in the IDLE state. It can cycle to any of the states: RFGT (Refresh Grant), RQGTA (Request Grant A), or RQGTB (Request Grant B), depending on the inputs: REFRQ (Refresh Request), MRQA (Memory Request A), or MRQB (Memory Request B).

REFRQ has top priority, since the refresh cycle is of vital importance for DRAM memory retention. MRQA is arbitrarily chosen to have priority over MRQB to avoid bus contention with contiguous requests. Every REQUEST, whether a refresh request or a memory request, must receive an ACK (acknowledge) signal before the Controller will continue to cycle. Once an ACK is received, the Controller will either return to the IDLE state or perform a refresh (if REFRQ is present), and then return to the IDLE state. Cycling between RQGTA and RQGTB is also possible.

The CUPL input file for the Controller, shown in Figure 7.12.4, distinguishes output declarations from intermediate variable definitions, which greatly reduce the complexity of declarations. BK3–BK0 are intermediate definitions decoded from address lines A17 and A16 to determine which bank will be selected. RQGTAS, RQGTBS, and RFGTS are also intermediate definitions of Controller state paths. These are used to simplify the final output declarations.

Output declarations for RQGTA, RQGTB, and RFTG are formulated by simply documenting each set of input conditions that causes the Controller to enter each state. ACK is a signal asserted by inputs the Controller receives that acknowledge the end of a memory access.

The second GAL16V8 device, called the Sequencer, is a state counter that asserts the control signals communicating with the DRAM section. Among these signals are: RAD (Row-Address-Data enable), CAD (Column-Address-Data enable), RAS (Row-Address Strobe), CAS (Column-Address Strobe), and ACK (Acknowledge). These signals are asserted when the Sequencer enters the proper state, as shown in the state diagram of Figure 7.12.3.

The CUPL input listing for the Sequencer is shown in Figure 7.12.6. Again, intermediate variable definitions are used to simplify output declarations. DST8–DST1 are intermediate definitions that name the states as decoded by the variables ST2, ST1, ST0. Notice that a grey-code scheme, which minimizes the number of product terms, was used for the counting operation.

Next, ST2, ST1 and ST0 are declared by identifying which previous states will cause each next state. For example, to cycle from state 2 (DST2) to state 3 (DST3), variables ST2 and ST1 will be logic ones and variable ST0 will be a logic zero upon reaching the new state. This can easily be extracted from the CUPL listing. Outputs RAD and CAD are also declared using the intermediate definitions DST8–DST1.
7.12 Dual-Port RAM Controller (Continued)

FIGURE 7.12.1. Block Diagram
7.12 Dual-Port RAM Controller (Continued)

FIGURE 7.12.2. State Diagram for Controller Section

FIGURE 7.12.3. State Diagram for Sequencer Section
7.12 Dual-Port RAM Controller (Continued)

The two GAL16V8-25 devices can be clocked at cycle times as fast as 35 ns (28.5 MHz), ample enough for the tight timings required to run a DRAM at its specified access times. The GAL16V8's power-up reset feature comes in handy in this circuit, since no inputs were available for a reset term. To test the functionality of this circuit, the simulation facilities of CUPL were used.

It should be noted that although the Controller uses all eight registers in the device, the Sequencer requires seven registers and one combinational output. While the Controller could be implemented in a traditional PAL configuration (16R8), the Sequencer requires a nonstandard architecture which can only be implemented in a GAL16V8 device. This is one of the biggest advantages of GAL devices—the flexibility of the architecture.

/* ********************************************************/
/* */
/* */
/* CUPL INPUT FILE */
/* */
/* Design input for the controller section of the */
/* Dual Port DRAM Controller */
/* */
/* ********************************************************/
/* */
/* Allowable Target Device Types: GAL16V8 */
/* ********************************************************/
/* */
PARTNO CONTROLLER SECTION;
NAME DRAM CONTROLLER;
DATE 03/28/86 ;
REV 01 ;
DESIGNER Joe Engineer;
COMPANY National Semiconductor;
ASSEMBLY ONE;
LOCATION U10;

/** Inputs **/

PIN 1 = SYSCLK;
PIN [2,3] = [A16,A17] ;
PIN [4..6] = [ST2,ST1,ST0] ;
PIN 7 = MRQA ;
PIN 8 = MRQB ;
PIN 9 = REFREQ ;
PIN 11 = !OE ;

/** Outputs **/

PIN 19 = !RAS0 ;
PIN 18 = !RAS1 ;
PIN 17 = !RAS2 ;
PIN 16 = !RAS3 ;
PIN 15 = !RQGTA ;
PIN 14 = !RQGTB ;
PIN 13 = !RFGT ;
PIN 12 = ACK ;

FIGURE 7.12.4. Design Input File for Controller Section
7.12 Dual-Port RAM Controller (Continued)

/** Declarations and Intermediate Variable Definitions **/

BK0 = (A17 & A16) # RFGT ;
BK1 = (A17 & A16) # RFGT ;
BK2 = (A17 & A16) # RFGT ;
BK3 = (A17 & A16) # RFGT ;

RASEN = !(ST2 & ST1 & !ST0 & ST2 & ST1 & !ST0 & !ST2 & ST1 & !ST0 ;

RAS0.D = BK0 & RASEN ;
RAS1.D = BK1 & RASEN ;
RAS2.D = BK2 & RASEN ;
RAS3.D = BK3 & RASEN ;

RQGTAS = RQGTA & !RQGTB & !RFGT ;
RQGTBS = !RQGTA & RQGTB & !RFGT ;
RFGTS = !RQGTA & !RQGTB & RFGT ;
IDLE = !RQGTA & !RQGTB & !RFGT ;


RFGT.D = (IDLE & REFRQ & RFGTS & !ACK & RQGTAS & ACK & REFRQ & RQGTBS & ACK & REFRQ) & !(ACK & !MRQA & !MRQB & !REFRQ) ;

ACK.D = ST2 & ST1 & ST0 & ST2 & ST1 & ST0 & RFGT ;

FIGURE 7.12.4. Design Input File for Controller Section (Continued)
7.12 Dual-Port RAM Controller (Continued)

/***************************************************************/
/* Allowable Target Device Types: GAL16V8 */
/***************************************************************/

PARTNO  CONTROLLER SECTION;
NAME     DRAM CONTROLLER;
DATE     03/28/86 ;
REV      01 ;
DESIGNER Joe Engineer;
COMPANY  National Semiconductor;
ASSEMBLY ONE;
LOCATION U10;

ORDER:
SYSCLK,%2,A17,A16,%2,ST2,ST1,ST0,%2,MRQA,MRQB,REFRQ,%2,!OE,%4,
!RAS0,!RAS1,!RAS2,!RAS3,%2,!RQGTA,!RQGTB,!RFGT,%2,ACK;

VECTORS:
$msg" S 11 ";
$msg" Y R 1111 RR1 ";
$msg" S MME RRRQ QQR ";
$msg" C AA SSS RRF ! AAAA GGF A ";
$msg" L 11 TTT QRR O SSSS TTG C ";
$msg" K 76 210 ABQ E 0123 ABT K ";
$msg" "---------------------------------- ";

0 00 101 000 0 XXXX XXX X
C 00 101 000 0 HHHH XXX H
C 00 111 000 0 HHHH HHH L
C 00 111 100 0 HHHH HHH L
C 00 010 100 0 LHHH LHH L
C 00 110 100 0 LHHH LHH L
C 00 011 100 0 LHHH LHH L
C 00 001 100 0 LHHH LHH L
C 00 000 100 0 LHHH LHH L
C 00 100 100 0 HHHH LHH L
C 00 101 110 0 HHHH LHH H
C 00 111 110 0 HHHH HLH L
C 11 111 010 0 HHHH HLH L
C 11 111 010 0 HHHH HLH L
C 11 010 010 0 HHHL HLH L
C 11 110 010 0 HHHL HLH L
C 11 011 010 0 HHHL HLH L
C 11 001 010 0 HHHL HLH L
C 11 000 010 0 HHHL HLH L
C 11 100 101 0 HHHH HLH L
C 11 101 101 0 HHHH HLH L
C 00 111 101 0 HHHH HLH L
C 00 111 101 0 HHHH HLH L
C 11 010 000 0 LLLL HLH L
C 11 110 000 0 LLLL HLH L
C 11 011 000 0 LLLL HLH L
C 11 001 000 0 LLLL HLH L
C 11 100 101 0 HHHH HLH L
C 11 101 101 0 HHHH HLH L
C 00 111 101 0 HHHH HLH L
C 00 111 101 0 HHHH HLH L

FIGURE 7.12.5. Simulation File for Controller Section
** 7.12 Dual-Port RAM Controller (Continued) **

```c
/* ***********************************************************************/
/*                        CUPL INPUT FILE                                */
/* Design input for the sequencer section for the                     */
/* Dual Port DRAM Controller                                          */
/* ***********************************************************************/
/* Allowable Target Device Types: GAL16V8                             */
/* ***********************************************************************/
PARTNO  SEQUENCER SECTION;
NAME    DRAM CONTROLLER;
DATE    03/28/86;
REV     01;
DESIGNER Joe Engineer;
COMPANY National Semiconductor;
ASSEMBLY TWO;
LOCATION U11;

/** Inputs **/
PIN 1   = SYSCLK;
PIN [2,3] = ![RQGTA, !RQGTB];
PIN 4   = RDY;
PIN 5   = !RFGT;
PIN 6   = !WR;
PIN 7   = ACK;
PIN 8   = !RES;
PIN 11  = !OE;

/** Outputs **/
PIN 19  = ST2;
PIN 18  = ST1;
PIN 17  = ST0;
PIN 16  = DIR;
PIN 15  = !CAD;
PIN 14  = !RAD;
PIN 13  = !ACKREF;
PIN 12  = !WE;
```

**FIGURE 7.12.6. Input File for Sequencer Section**
7.12 Dual-Port RAM Controller (Continued)

/** Declarations and Intermediate Variable Definitions **/

DST1 = ST2 & ST1 & ST0;
DST2 = !ST2 & ST1 & !ST0;
DST3 = ST2 & ST1 & !ST0;
DST4 = !ST2 & ST1 & ST0;
DST5 = !ST2 & !ST1 & ST0;
DST6 = !ST2 & !ST1 & !ST0;
DST7 = ST2 & !ST1 & !ST0;
DST8 = ST2 & !ST1 & ST0;

STCYC = (((RQGTA # RQGTB) & RDY # RFGT));

ST2.D = (DST2 # DST6 # DST8 # DST7 # DST4 & RFGT) # RES #
        DST1 & !STCYC;

ST1.D = DST2 # DST3 # DST8 # DST4 & RFGT # DST1 # RES;

ST0.D = (DST3 # DST4 # DST7 # DST8) # RES # DST1 & !STCYC;

DIR.D = WR & !DST1;

CAD.D = DST3 & !RFGT # DST4 & !RFGT # DST5;

RAD.D = (RQGTA # RQGTB) & RDY & (DST1 # DST2);

ACKREF = RFGT & ACK;

WE.D = WR & (DST5 # DST6);

FIGURE 7.12.6. Input File for Sequencer Section (Continued)
7.12 Dual-Port RAM Controller (Continued)

/* **********************************************************************************************/
/* *  */
/*  */
/*  */
/* - CUPL SIMULATION FILE */
/*  */
/* - Simulation File for the sequencer section of the Dual Port DRAM Controller */
/*  */
/*  */
/* **********************************************************************************************/
/* Allowable Target Device Types: GAL16V8 */
/* **********************************************************************************************/

PARTNO SEQUENCER SECTION;
NAME DRAM CONTROLLER;
DATE 03/28/86 ;
REV 01 ;
DESIGNER Joe Engineer;
COMPANY National Semiconductor;
ASSEMBLY TWO;
LOCATION U11;

ORDER:
SYSCLK,%2, !RES,%2, !RQGTA, !RQGTB, !RFGT,%2, RDY, !WR, ACK,%2, !OE,%4,
ST2,ST1,ST0,%2, DIR,%2, !CAD, !RAD,%2, !WE ;

VECTORS:
$num" S   ! !       ";
$num" Y   RR!       ";
$num" S   QQR ! !    ";
$num" C R GGF R!A !   SSS D CR ! ";
$num" L E TTG DWC O   TTT I AA W ";
$num" K S ABT YRK E   210 R DD E ";
$num" ------------------- ";
0 0 111 010 0  XXX X XX X
0 0 111 010 0  XXX X XX X
C 0 111 010 0  HHH L XH H
C 1 011 010 0  HHH L HH H
C 1 011 110 0  LHL L HL H
C 1 011 110 0  HHL L HL H
C 1 011 010 0  LHH L LH H
C 1 011 010 0  LLH L LH H
C 1 011 010 0  LLL L LH H
C 1 011 010 0  HLL L HH H
C 1 011 010 0  HLH L HH H
C 1 011 010 0  HHH L HH H
C 1 011 010 0  HHH L HH H
C 1 011 010 0  HHH L HH H

FIGURE 7.12.7. Simulation File for Sequencer Section

TL/L/8991-83
FIGURE 7.13. Control Logic for 8086 CPU Board
7.13 8086 CPU Board Random Control Logic (Continued)

PLANTM INPUT FILE

title 8086 CPU CONTROL LOGIC
pattern CPU8086
revision A
author Tarif Engineer
company National Semiconductor Corporation
Date 11/28/1989

chip CPU8086 PAL12H6

; pin 1 2 3 4 5 6 7 8 9 10
PD  EN  E0  EA  S1  SA  E1  DO  DE  GND

; pin 11 12 13 14 15 16 17 18 19 20
S0  NC  N0  C3  HA  SS  LA  MW  PW  VCC

equations

MW = /S0 + PW * DE
LA = /SA * /DO
SS = S1 * PD * /SA
HA = S1 * PD * /SA * EA * E1
C3 = PD * E0 * EA
N0 = PD * /EN

; end of CPU8086

Chip Diagram (DIP)
Document file for CPU8086.inp
Device: 12H6

<table>
<thead>
<tr>
<th>Pin</th>
<th>Label</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PD</td>
<td>com input</td>
</tr>
<tr>
<td>2</td>
<td>EN</td>
<td>com input</td>
</tr>
<tr>
<td>3</td>
<td>E0</td>
<td>com input</td>
</tr>
<tr>
<td>4</td>
<td>EA</td>
<td>com input</td>
</tr>
<tr>
<td>5</td>
<td>S1</td>
<td>com input</td>
</tr>
<tr>
<td>6</td>
<td>SA</td>
<td>com input</td>
</tr>
<tr>
<td>7</td>
<td>E1</td>
<td>com input</td>
</tr>
<tr>
<td>8</td>
<td>D0</td>
<td>com input</td>
</tr>
<tr>
<td>9</td>
<td>DE</td>
<td>com input</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>ground pin</td>
</tr>
<tr>
<td>11</td>
<td>S0</td>
<td>com input</td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td>unused</td>
</tr>
<tr>
<td>13</td>
<td>N0</td>
<td>pos, com output</td>
</tr>
<tr>
<td>14</td>
<td>C3</td>
<td>pos, com output</td>
</tr>
<tr>
<td>15</td>
<td>HA</td>
<td>pos, com output</td>
</tr>
<tr>
<td>16</td>
<td>SS</td>
<td>pos, com output</td>
</tr>
<tr>
<td>17</td>
<td>LA</td>
<td>pos, com output</td>
</tr>
<tr>
<td>18</td>
<td>MW</td>
<td>pos, com output</td>
</tr>
<tr>
<td>19</td>
<td>PW</td>
<td>com input</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>power pin</td>
</tr>
</tbody>
</table>
A GAL6001-30L Zero Wait State Page Mode Memory System Interface Between The DP8422A and The 68020

1.0 INTRODUCTION
This application note describes how the National Semiconductor GAL6001-30L can create a zero wait state page mode memory system interface between the DP8422A DRAM controller and the 68020 microprocessor operating at 16 MHz. It is assumed that the reader is already familiar with 68020 CPU, the DP8422A and GAL design using the GAL6001-30L.

2.0 DESCRIPTION OF DESIGN
This design illustrates the use of the GAL6001 in conjunction with the DP8422A DRAM controller to provide a no-wait state page mode memory system for a 68020 CPU running at 16 MHz. This application note assumes two 32-bit memory banks using 4 M-bit DRAMs. This gives a 32 Mega-byte memory.

This memory design forces three wait states during out-of-page accesses and zero wait states during in-page accesses using inexpensive 100 ns DRAMs. The theory behind this design is that the CPU will tend to have multiple accesses within some local area of memory (a page) before accessing some other area of memory (different page). The more accesses within a page of memory, the more efficient this memory design allows the CPU to become. The page size of a 4 M-bit DRAM is 2048 bits. The page size of one bank of memory (32 bits per bank) is 8192 bytes or 8 Kbytes.

It should be noticed that if the user wanted to use fast DRAMs (80 ns or less access times) he could get rid of one wait state during out-of-page accesses. This can be seen by subtracting one clock period (62.5 ns) from the calculated RAS access time (tRAC) and the CAS access time (tCAC), section IV numbers 5 and 6. This would result in the design forcing two wait states during out-of-page accesses, in-page accesses would still remain with zero wait states.

Figure 1 shows a block diagram of this design driving two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of up to 32 Mbytes (using 4 M-bit by 1 DRAMs). This memory design could easily be changed to four banks of 1 M-bit DRAMs since there are 12 bits that are compared internally, 10 bits of row address for 1 M-bit DRAMs and 2 bank bits.

The memory banks are interleaved on page boundaries (2K double word boundaries). This means that the address bit (A13) is tied to the bank select input of the DP8422A (B1). The bottom 11 bits (A2–12) constitute the column address es (intra-page address) and the top 11 bits constitute the row addresses (page address) of the DRAMs. Address bits A0 and A1 are used, along with the transfer size outputs (SIZ0, 1), to produce the four byte select strobe inputs to the DP8422A, ECAS~ (3:0). These byte select strobes, ECAS~ (3:0), enable the CAS~ outputs which are used in byte reads and writes. The ECAS~ output of the GAL6001 further shapes the CAS~ pulse to the DRAMs, CS~ (3:0).

The GAL6001-30 along with the DP8422A DRAM controller implement a page mode DRAM system. The GAL6001-30 latches the DRAM row and bank inputs (ROW0-10, B1) during each Chip Selected access. This page address is compared with each new Chip Selected address to determine whether the current access is within the same page of DRAM as the previous access. If the current access is within the same page a zero wait state access can be completed. If the current access is to another page of the DRAM the GAL6001-30 will end the current access by pulling AREQ~ high; latch the new current page address in its internal registers; start the new access by pulling AREQ~ back low again; and then pull DSACK~ low once the current access has completed.

If AS~ from the 68020 is high and a refresh is requested (RFRQ~ low) the GAL6001-30 will end the current page mode access by pulling AREQ~ high. Then the GAL will allow the refresh to take place and start the next CPU DRAM access if one has been requested.

The logic shown in this application note forms a complete 68020 memory sub-system, no other logic is needed. This sub-system automatically takes care of:
A. arbitration between Port A and refreshing the DRAM;
B. the insertion of wait states to the processor (Port A and Port B) when needed (i.e., if RAS~ precharge is needed, refresh is happening during a memory access . . . etc.);
C. performing byte writes and reads to the 32-bit double words in memory.

Memory system timing diagrams appear in Figures 2, 3, and 4. These figures are the result of simulating this design on an engineering workstation.

Also, throughout this application note the symbol "~" has been used to denote an active low signal. For example RAS~0 refers to the active low RAS0 output of the DP8421A.
3.0 DP8422A PROGRAMMING MODE BITS

<table>
<thead>
<tr>
<th>Programming Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0 = 0</td>
<td>RAS~ low two clocks, RAS~ precharge of two clocks. If more RAS~ precharge is desired by the user, programming three periods of RAS~ precharge</td>
</tr>
<tr>
<td>R1 = 1</td>
<td>DTACK~ 1 is chosen, DTACK~ follows the access RAS~ low on the following rising clock edge</td>
</tr>
<tr>
<td>R2 = 1</td>
<td>No WAIT states during burst accesses</td>
</tr>
<tr>
<td>R3 = 0</td>
<td>R3 = 0</td>
</tr>
<tr>
<td>R4 = 0</td>
<td>R4 = 0</td>
</tr>
<tr>
<td>R5 = 0</td>
<td>R5 = 0</td>
</tr>
<tr>
<td>R6 = 0</td>
<td>R6 = 0</td>
</tr>
<tr>
<td>R7 = 1</td>
<td>R7 = 1</td>
</tr>
<tr>
<td>R8 = 1</td>
<td>R8 = 1</td>
</tr>
<tr>
<td>R9 = X</td>
<td>R9 = X</td>
</tr>
<tr>
<td>C0 = 0</td>
<td>Select based upon the input</td>
</tr>
<tr>
<td>C1 = 1</td>
<td>&quot;DECLK&quot; frequency. Example: if the input clock frequency is 16 MHz then choose C0, 1, 2 = 0, 1, 0 (divide by eight, this will give a frequency of 2 MHz).</td>
</tr>
<tr>
<td>C2 = 0</td>
<td>RAS~ banks selected by &quot;B1&quot;. Mode allows two RAS~ outputs to go low during an access, and allows byte writing in 16-bit words.</td>
</tr>
<tr>
<td>C3 = X</td>
<td>Column address setup time of 0 ns.</td>
</tr>
<tr>
<td>C4 = 0</td>
<td>Row address hold time of 15 ns</td>
</tr>
<tr>
<td>C5 = 0</td>
<td>Delay CAS~ during write accesses to one clock after RAS~ transitions low</td>
</tr>
<tr>
<td>C6 = 1</td>
<td>Fall through latches.</td>
</tr>
<tr>
<td>C7 = 1</td>
<td>Access mode 1</td>
</tr>
<tr>
<td>C8 = 1</td>
<td>Allow CAS~ to be extended after RAS~ transitions high. Also, allow the WE~ output to be used as a refresh request (RFRQ~) output indicator.</td>
</tr>
<tr>
<td>C9 = 1</td>
<td>0 = Program with low voltage level</td>
</tr>
<tr>
<td>B0 = 1</td>
<td>1 = Program with high voltage level</td>
</tr>
<tr>
<td>B1 = 1</td>
<td>X = Program with either high or low voltage level (don't care condition)</td>
</tr>
</tbody>
</table>

2. Minimum time to ADS~ valid: 62.5 ns (one clock period at 16 MHz) + 4 ns (GAL6001-30 max time output clock to AREQ~ valid) = 66.5 ns

3. Minimum CS~ setup time to ADS~ valid (DP8422A-25 needs a minimum of 5 ns): 66.5 ns (see #2 above) - 30 ns (see #1 above) = 36.5 ns

4. Minimum CS~ setup time to CLOCK high (GAL6001-30 needs 25 ns input setup time to the output CLOCK for the AREQ~ output): 62.5 ns (one clock) - 30 ns (max time to address bit 31 valid, see #1 above) = 32.5 ns

5. Determining tRAC during a normal access (RAS~ access time needed by the DRAM): 217.5 ns (three and one half clocks, \((3 \times 62.5) + 30 = 217.5 \text{ ns}\)) - 15 ns (GAL6001-30 max CLK to AREQ~ valid) - 7 ns (74F245 max delay) - 5 ns (68020 data setup time) = 161.5 ns Therefore the tRAC of the DRAM must be 161.5 ns or less.

6. Determining tCAC during a normal access (CAS~ access time): 217.5 ns (three and one half clocks, \((3 \times 62.5) + 30 = 217.5 \text{ ns}\)) - 15 ns (GAL6001-30 max CLK to AREQ~ valid) - 7 ns (74F245 max delay) - 14 ns (74F32 CS~(3:0) drivers max delay driving 125 pF) - 5 ns (68020 data setup time) = 102.5 ns Therefore the tCAC and the column address access time of the DRAM must be 102.5 ns or less.

7. Maximum time to CS~(3:0) low during a page mode access: 62.5 ns (one clock at 16 MHz) + 30 ns (GAL6001-30 max time from clock to output, ECAS~) + 14 ns (74F32 max time to CS~(3:0) valid) = 106.5 ns

8. Minimum time to DRAM column address strobes low [CS~(3:0)] during a page mode access: 62.5 ns (one clock at 16 MHz) + 8 ns (assumed GAL6001-30 max time from input to output, ECAS~) + 4 ns (assumed 74F32 min time to CS~(3:0) valid) = 74.5 ns
9. Determining the minimum column address setup time to CS~ (3:0) low (0 ns needed by the DRAMs) during burst mode accesses for zero wait states:
   74.5 ns (see #8 above, min time to CS~ (3:0) valid)
   −30 ns (max time to 68020 address valid)
   −35 ns (DP8422A-25 max time address in to out, #27)
   = 9.5 ns minimum
10. Determining the tCAC (CAS~ access time) needed during burst mode accesses for zero wait states:
   155 ns (two and one half clocks, (2 × 62.5) + 30 = 155 ns)
   −106.5 ns (max time to CS~ (3:0), see #7 above)
   −7 ns (74F245 max delay)
   −5 ns (68020 data setup time)
   = 36.5 ns
11. Determining the column address access time needed during burst mode accesses for zero wait states:
   155 ns (two and one half clocks, (2 × 62.5) + 30 = 155 ns)
   −30 ns (max time to 68020 address valid)
   −35 ns (DP8422A-25 max time address in to out, #27)
   −7 ns (74F245 max delay)
   −5 ns (68020 data setup time)
   = 78 ns
12. Minimum DSACK~ (Data transfer and Size ACKnowledge) setup time to clock low (68020 DSACK~ input needs 5 ns, #47a) during page mode zero wait state accesses:
   30 ns (one half clock period, S2 clock of 68020 clock cycle)
   −25 ns (GAL6001-30 input to outputs enabled, DSACK~ output)
   = 5 ns

Note: Calculations can be performed for different frequencies, different logic (ALS or CMOS etc.), and/or different combinations of wait states by substituting the appropriate values into the above equations.

5.0 68020 GAL6001-30 INPUT AND OUTPUT DESCRIPTIONS

Inputs:
ROW0-10 These are the row address inputs of the DRAMs and are also connected to the R0-10 inputs of the DP8422A-25. The GAL6001-30 latches these inputs along with the B1 input and compares this address with each new address during a Chip Selected DRAM access to determine whether the current address is within the same page of DRAM as the previous access.

B1 The bank input to the DP8422A-25, B1 input. This input determines which of the two DRAM banks the CPU is currently accessing in. The GAL6001-30 latches this input along with the ROW0-10 inputs and compares this address with each new address during a Chip Selected DRAM access to determine whether the current access is within the same page of DRAM as the previous access.

RFRQ~ The ReFresh ReQuest input from the DP8422A DRAM controller.

READ The 68020 READ and write access indicator.

DTACK~ The DP8422A Data Transfer ACKnowledge indicator.

AS~ The 68020 address strobe, indicating that the CPU address is valid and a CPU access is in progress.

CS~ Chip Select for the memory system. It was assumed that the 68020 address bit 31 would be used for this indicator. When low it indicates that the 68020 is accessing the DRAM.

CLK, ICLK The 68020 system clock, 16 MHz in this application.

Outputs:
AREQ~ The DRAM Access REQuest. This signal is input to the DP8422A DRAM controller. It will remain low as long as all 68020 chip selected accesses remain within the current page. As soon as an access occurs that is not within the currently latched page address or a refresh request occurs AREQ~ will be pulled high.

ECAS~ Enable CAS~ is toggled during every access and is used to drive the CAS~ inputs to the DRAMs, CS~ (3:0). This input is delayed during write accesses to allow time for the data to become valid at the DRAM inputs before CAS~ transitions low. The READ input to the DRAMs is guaranteed to transition while ECAS~ is high.

Internal Nodes:
LR0-10 These are the latched ROW0-10 addresses of the current page of DRAM. These addresses are clocked by the falling edge of CS__AS_L~.

LB1 This is the latched B1 address of the current page of DRAM.

CS__AS_L~ This is a latched version of Chip Select and Address Strobe of the 68020. This signal toggles during each access and transitions low from the rising edge of S2 clock and high from the rising edge of S5 clock.
AS_D2~ This is a delayed version of CS_AS_L~.
FREQD~ This is the DP8422A ReFresh ReQuest
Delayed and Synchronized to the 68020 system clock.

6.0 68020 GAL6001-30 EQUATIONS WRITTEN IN NATIONAL SEMICONDUCTOR PLAN FORMAT

| TITLE | 68020/DP8422A DRAM PAGE DETECTOR FOR USE WITH NATIONAL GAL6001 |
| PATTERN | PG_DETECT |
| REV | A |
| AUTHOR | RUSTY MEIER |
| COMPANY | NATIONAL SEMICONDUCTOR |
| DATE | DEC. 11, 1989 |
| CHIP | PG_DETECT GAL6001 |

;PIN LIST
R0 R1 R2 R3 R4 R5 R6 R7 RFRQ~ DTACK~ AS~ GND
CLK R8 R9 R10 B1 CS~ ICLK DSACK~ AREQ~ ECAS~ READ VCC
;BURIED NODE OUTPUTS
LR0 LR1 LR2 LR3 LR4 LR5 LR6 LR7
;DUAL FEEDBACK NODE OUTPUTS
LR8 LR9 LR10 LB1 CS_AS_L~ AS_D2~ NC NC NC RFRQD~

;GAL DUAL FEEDBACK NODES ********************************************
;NOTICE THAT THE CLOCKS (XXX.CLKF TERMS)
;ARE THE SAME AS *CS_AS_L~* INVERTED
LR8 := R8
LR8.CLFK = !CS~ & !AS~ & ICLK
# CS_AS_L~ & !AS~
# CS_AS_L~ & !ICLK
LR9 := R9
LR9.CLFK = !CS~ & !AS~ & ICLK
# CS_AS_L~ & !AS~
# CS_AS_L~ & !ICLK
LR10 := R10
LR10.CLFK = !CS~ & !AS~ & ICLK
# CS_AS_L~ & !AS~
# CS_AS_L~ & !ICLK
LB1 := B1
LB1.CLFK = !CS~ & !AS~ & ICLK
# CS_AS_L~ & !AS~
# CS_AS_L~ & !ICLK
CS_AS_L~ = !CS~ & !AS~ & !CS_AS_L~ & !ICLK
# CS~ & !AS~ & !AS_D2~
# CS~ & !AS_D2~ & !ICLK
!RFRQD~ := !RFRQ~
;GAL OUTPUTS *****************************************
DSACK~ = CS~
# CS~ & R0 & !LR0
# CS~ & !R0 & LR0
# CS~ & R1 & LR1
# CS~ & !R1 & LR1
# CS~ & R2 & LR2
# CS~ & !R2 & LR2
# CS~ & R3 & LR3
# !CS~ & IR3 & LR3  
# !CS~ & R4 & !LR4  
# !CS~ & IR4 & LR4  
# !CS~ & R5 & !LR5  
# !CS~ & IR5 & LR5  
# !CS~ & R6 & !LR6  
# !CS~ & IR6 & LR6  
# !CS~ & R7 & !LR7  
# !CS~ & IR7 & LR7  
# !CS~ & R8 & !LR8  
# !CS~ & IR8 & LR8  
# !CS~ & R9 & !LR9  
# !CS~ & IR9 & LR9  
# !CS~ & R10 & !LR10 
# !CS~ & IR10 & LR10 
# !CS~ & B1 & !LB1  
# !CS~ & !B1 & LB1 
# DTACK~  
# DSACK~ & ICLK & !AS_D2~  
# AS~ & !AS_D2~  
# AREQ~  

DSACK~ .TRST = !CS~ & !AS~  

ECAS~ = CS~  

# !CS~ & RO & !LR0  
# !CS~ & IR0 & LR0  
# !CS~ & RI & !LR1  
# !CS~ & IR1 & LR1  
# !CS~ & R2 & !LR2  
# !CS~ & IR2 & LR2  
# !CS~ & R3 & !LR3  
# !CS~ & IR3 & LR3  
# !CS~ & R4 & !LR4  
# !CS~ & IR4 & LR4  
# !CS~ & R5 & !LR5  
# !CS~ & IR5 & LR5  
# !CS~ & R6 & !LR6  
# !CS~ & IR6 & LR6  
# !CS~ & R7 & !LR7  
# !CS~ & IR7 & LR7  
# !CS~ & R8 & !LR8  
# !CS~ & IR8 & LR8  
# !CS~ & R9 & !LR9  
# !CS~ & IR9 & LR9  
# !CS~ & R10 & !LR10 
# !CS~ & IR10 & LR10 
# !CS~ & B1 & !LB1 
# !CS~ & !B1 & LB1  

# AS~  

# CS~  
# ECAS~ & !ICLK & CS_AS_L~  

AREQ~  

# !READ & ECAS~ & AS_D2~ & ICLK  
# !RFRD~ & CS_AS_L~  

AREQ~ :=  

!CS~ & RO & !LR0  
# !CS~ & IR0 & LR0  
# !CS~ & R1 & !LR1  
# !CS~ & IR1 & LR1  
# !CS~ & R2 & !LR2
BURIED NODES
**************************************
; NOTICE THAT THE CLOCKS (xxx.CLKF TERMS) ARE THE
; SAME AS 'CS_AS_L~' INVERTED
LR0 := R0
LR0.CLKF = !CS- & !AS- & ICLK
= !CS_AS_L~ & !AS~
= !CS_AS_L~ & !ICLK

LR1 := R1
LR1.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK

LR2 := R2
LR2.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK

LR3 := R3
LR3.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK

LR4 := R4
LR4.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK

LR5 := R5
LR5.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK

LR6 := R6
LR6.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK

LR7 := R7
LR7.CLKF = !CS- & !AS- & ICLK
# !CS_AS_L~ & !AS~
# !CS_AS_L~ & !ICLK
FIGURE 1. A GAL6001 Interface to the 68020/DP8422A-25/DRAM Using Page Mode Accessing
FIGURE 2. System Timing
FIGURE 3. System Timing
FIGURE 4. System Timing
A PAL Interface between Static Random Access Memory (SRAM) and the NSC Raster Graphics Processor (RGP, DP8500)

INTRODUCTION
This application note describes a PAL design that interfaces the National Semiconductor RGP to Static RAM. This allows the RGP to be operated at up to 20 MHz with one wait state inserted during normal accesses. It is assumed that the reader is familiar with the National Semiconductor RGP, SRAM, and the basics of PAL design.

DESIGN DESCRIPTION
A block diagram of the RGP to SRAM interlace is seen in Figure 1. The State Machine block (PAL interface) receives the control signals from the RGP (BS1, RD−, WR−, ALE), the SRAM chip select from the address decoding circuitry (CS−), and the Phase 2 clock (PHI2) to the RGP. The State Machine block outputs a READY signal back to the RGP to allow the insertion of wait states into RGP access cycles, drives the System Read (SYS_RD−) and System Write (SYS_WR−) outputs to control the SRAM, drives the DDIN− and DBE− signals to control the data transceivers, and drives the State Variables (A, B, C) that control the interface (see Figure 2).

Figure 3 shows a State Transition Diagram for the design. A State Table Diagram for the Design (Figure 4) was then drawn up from Figure 3. The State Table Diagram was used to draw up Karnaugh Maps for each State Variable and output of the design, these can be seen in Figures 5, 6 and 7. These equations were then put in ABEL format in Figure 8.

DESIGN TIMING ANALYSIS AT 20 MHz
1. Maximum time to valid address at SRAM inputs from PHI2 rising edge:
   11 ns (ALE valid from PHI2 rising edge) + 23 ns (74ALS373 maximum propagation delay of enable to output valid) = 34 ns.

2. Maximum time to chip select valid at SRAM input from PHI2 rising edge:
   34 ns (see #1 above) + 22 ns (maximum propagation delay of 74ALS138) = 56 ns.

3. Minimum available time to perform an access of SRAM from rising edge PHI2 (during T1) to falling edge PHI2 (during T3):
   150 ns (3 clocks) + 19 ns (minimum PHI2 high time) = 169 ns.

4. Determining the SRAM address access time needed in this design:
   169 ns (available time, #3 above)
   -34 ns (max time to valid address, see #1 above)
   -10 ns (74ALS245 maximum delay time)
   -= 98 ns access time,
   therefore the SRAM must have a Chip Select access time of 98 ns or less.

5. Determining the SRAM Output Enable (GAL SYS_RD− output) access time needed in this design:
   169 ns (available time, #3 above)
   -100 ns (two clocks, rising edge of PHI2 during T1 until rising edge PHI2 during T2)
   -10 ns (GAL16V8A-10 maximum time from PHI2 rising clock edge until clocked output is valid)
   -= 8 ns (GAL16V8A-15 maximum time to SYS_RD− output valid)
   -10 ns (74ALS245 maximum delay time)
   -= 5 ns (RGP Data setup time) = 36 ns access time,
   therefore the SRAM must have an Output Enable access time of 36 ns or less.
FIGURE 1. Block Diagram of Raster Graphics Processor (RGP) to Static Random Access Memory (SRAM) Interface

FIGURE 2. Synchronized State Machine Model

FIGURE 3. State Transition Diagram for RGP/SRAM Interface Design
<table>
<thead>
<tr>
<th>Present State</th>
<th>Inputs</th>
<th>Next State</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A</strong></td>
<td><strong>B</strong></td>
<td><strong>C</strong></td>
<td><strong>ALEL~</strong></td>
</tr>
<tr>
<td>0 0 0</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0 0 0</td>
<td>X</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0 0 0</td>
<td>X</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0 0 0</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0 1 0</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0 1 1</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1 0 0</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1 0 1</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1 1 0</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1 1 1</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**FIGURE 4. State Table Diagram**

*ASSUME:  
F = ALEL~ & BS1~ & CS~ & (IALEL~ & IBS1~ & ICS~ & IRD~)  
G = ALEL~ & BS1~ & CS~ & (IALEL~ & IBS1~ & ICS~ & RD~)  

* Assume using active low outputs, circle "0"'s.

**FIGURE 5. Using Karnaugh Maps To Generate PAL Equations**
Since PAL16V8 has active low outputs, circle "0"s.

![Karnaugh Map](image1)

This term is not needed in this example because there never is a transition between states '011' and '111'.

![Karnaugh Map](image2)

![Karnaugh Map](image3)

**FIGURE 6. Using Karnaugh Maps To Generate PAL Equations**

Since PAL16V8 has active low outputs, circle "0"s.

![Karnaugh Map](image4)

![Karnaugh Map](image5)

**FIGURE 7. Using Karnaugh Maps To Generate PAL Equations**
MODULE SRAM_INTERFACE

TITLE 'SRAM_PAL, THIS PAL INTERFACES THE NATIONAL SEMICONDUCTOR RASTER GRAPHICS PROCESSOR TO A STATIC RANDOM ACCESS MEMORY'.

SRAM_PAL device 16V8

|    | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 | Pin 10 | Pin 11 | Pin 12 | Pin 13 | Pin 14 | Pin 15 | Pin 16 | Pin 17 | Pin 18 | Pin 19 | Pin 20 |
|----|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| PHI_2 | ALEL_ | BS1   | CS~   | RD~   | NC1   | NC2   | NC3   | READY | NC4   | SYS_RD~ | A      | B      | SYS_WR~ | A      | B      | VCC   |
| NC4   | Pin 9 | Pin 10 | Pin 11 | Pin 12 | Pin 13 | Pin 14 | Pin 15 | Pin 16 | Pin 17 | Pin 18 | Pin 19 | Pin 20 |
| C     | Pin 17 | Pin 18 | Pin 19 | Pin 20 | Pin 2 | Pin 6 | Pin 10 | Pin 14 | Pin 13 | Pin 8 | Pin 7 | Pin 6 |

EQUATIONS

IA:

\[
\text{IA} = \text{ALEL} \land \text{IA} \\
\text{# BS1} \land \text{IA} \\
\text{# CS} \land \text{IA} \\
\text{# IALEL} \land \text{IBS1} \land \text{ICS} \land \text{IRD} \land \text{IA} \\
\text{# IA} \land \text{IC} \\
\text{# B}
\]

IB:

\[
\text{IB} = \text{IC} \\
\text{# A} \land \text{B} \\
\text{= ALEL} \land \text{IA} \land \text{IC}
\]

IC:

\[
\text{IC} = \text{BS} \land \text{IA} \land \text{IC} \\
\text{# CS} \land \text{IA} \land \text{IC} \\
\text{# IALEL} \land \text{IBS1} \land \text{ICS} \land \text{RD} \land \text{IA} \land \text{IC} \\
\text{# B}
\]

IDBE~

\[
\text{IDBE} = \text{A} \land \text{IB} \\
\text{# B} \land \text{C} \\
\text{# IA} \land \text{B} \\
\text{# A} \land \text{C}
\]

IDDIN~

\[
\text{IDDIN} = \text{IA} \land \text{C} \\
\text{# IA} \land \text{B}
\]

SYS_RD~

\[
\text{SYS_RD} = \text{IA} \land \text{B}
\]

SYS_WR~

\[
\text{SYS_WR} = \text{A} \land \text{IB}
\]

READY

\[
\text{READY} = \text{IA} \land \text{IB} \\
\text{# A} \land \text{B} \\
\text{# IC}
\]

FIGURE 8. Able PAL Equations
Notes: 20 MHz Operation: State machine changes state on rising edge of PHI_2.
WAIT_DISABLE sampled by RGP on every falling edge of PHI_2 during T2.
Data sampled by RGP on falling edge of PHI_2 during T3.

FIGURE 9. Non Draw SRAM Read Operation
Notes: 20 MHz Operation: State machine changes on rising edge of PHIL_2.
Wait sampled on every falling edge of PHIL_2 during T2.

FIGURE 10. Non Draw SRAM Write Operation
A PAL Interface for a 25 MHz and above No-Wait State DP8422A/80286 Burst Mode DRAM Memory System

I. INTRODUCTION
This application note describes a two PAL designs that interface the DP8422A to the 80286 CPU. The first design allows the 80286 to be operated at up to 40 MHz (80286-20) with one wait state inserted during normal accesses. The second design allows the 80286 to operate at up to 40 MHz (80286-20) with zero wait states inserted when operating the DRAMs in page mode. Design number two also makes use of the 74ALS311 page detector to determine whether the 80286 current access is within the same page as the previous access. It is assumed that the reader is familiar with the 80286, the DP8422A DRAM controller, the 74ALSO311 and the basics of PAL design.

II. DESCRIPTION OF DESIGN #1, 80286 OPERATING AT UP TO 40 MHz WITH ONE WAIT STATED (80286-20)
The block diagram of this design is shown driving two banks of DRAM, each bank being 16 bits in width, giving a maximum memory capacity of up to 4 Mbytes (using 1 Mbit x 1 DRAMs). This memory could easily be expanded up to 32 Mbytes using four banks of 4 Mbit DRAMs.
The memory banks are interleaved on word (16-bit word) boundaries. This means that the address bit (A11) is tied to the bank select input of the DP8422A (B1).
Address bit A0 is used, along with Bus High Enable (BHE), to produce the two byte select ECAS~0,1 strobes. These byte select strobes (ECAS~0,1) enable the CAS~ outputs which are used in byte reads and writes.
If the majority of accesses made by the 80286 are sequential, the 80286 can alternate memory banks, allowing one memory bank to be precharging (RAS~ precharge) while the other banks are being accessed. Each separate memory access to the same memory bank will require extra wait states to be inserted into the CPU access cycles to allow for the RAS~ precharge time.
This application inserts 1 wait state in normal accesses of the 80286. The number of wait states can be adjusted through the WAITIN input of the DP8422A.
The logic shown in this application note forms a complete 80286 memory sub-system, no other logic is needed. This sub-system automatically takes care of:
A. Arbitration between Port A, Port B, and refreshing the DRAM;
B. The insertion of wait states to the processor (Port A and Port B) when needed (i.e., if RAS~ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . . etc);
C. Performing byte writes and reads to the 16-bit words in memory.
It is important that the 74AS00 NAND gates (U1) be in the same package so these delays (CLK~, S01) track each other.

By using the "output control" pins of some external latches (74AS73's), this application can easily be used in a dual access application. The addresses could be tri-stated through these latches, the write input (WIN~), lock input (LOCK~), and ECAS~0-3 inputs must also be able to be tri-stated (a 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A can be used in a dual access application. If this design is used in a dual access application the iRAC and iCAC (required RAS and CAS access time required by the DRAM) will have to be recalculated since the time to RAS and CAS is longer for the dual access application (see TIMING section of this application note).
Also, throughout this application note the symbol '~' has been used to denote and active low signal. For example RAS~0 refers to the active low RAS0 output of the DP8421A. For even higher system performance an 'E' speed PAL can be used.

III. DESCRIPTION OF DESIGN #2, 80286 OPERATING AT UP TO 40 MHz (80286-20) WITH ZERO WAIT STATES USING PAGE MODE DRAMs
This design is very similar with respect to design #1 except for the following differences.
The memory banks are interleaved on page (1024 word) boundaries. This means that the address bit (A11) is tied to the bank select input of the DP8421A (B1).
Address bit A0 is used, along with Bus High Enable (BHE), to produce the two byte select ECAS~0,1 strobes. These byte select strobes (ECAS~0,1) are logically "ORed" with the DP8421A CAS~ outputs to produce the byte selecting CAS~ inputs to the DRAMs.
If the majority of accesses made by the 80286 are sequential and within a page, the 80286 in conjunction with the page detector (74ALS311) allow zero wait state accessing. Each in-page memory access is completed using page mode (toggling the CAS~ inputs).
As in design #1 it is important that the 74AS00 NAND gates (U1) be in the same package so the delays (CLK~, S01) track each other. For even higher system performance an 'E' speed PAL could be used.
IV. 80286 DESIGNS #1 AND #2 PROGRAMMING MODE BITS

<table>
<thead>
<tr>
<th>Programming Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0 = 0</td>
<td>RAS~ low two clocks, RAS~ precharge of two clocks. If more RAS~ precharge is desired the user should program three periods of RAS~ precharge.</td>
</tr>
<tr>
<td>R1 = 1</td>
<td>DTACK~ 1/2 is chosen.</td>
</tr>
<tr>
<td>R2 = 0</td>
<td>DTACK~ follows the access RAS~ low.</td>
</tr>
<tr>
<td>R3 = 1</td>
<td>No WAIT states during burst accesses.</td>
</tr>
<tr>
<td>R4 = 0</td>
<td>If WAITIN~ = 0, add one clock to DTACK~. WAITIN~ may be tied high or low in this application depending upon the number of wait states the user desires to insert into the access.</td>
</tr>
<tr>
<td>R5 = 0</td>
<td>Select DTACK~.</td>
</tr>
<tr>
<td>R6 = 0</td>
<td>Select based upon the input</td>
</tr>
<tr>
<td>R7 = 1</td>
<td>Non-interleaved Mode.</td>
</tr>
<tr>
<td>R8 = 1</td>
<td>RAS~ low two clocks, RAS~ precharge of two clocks.</td>
</tr>
<tr>
<td>R9 = X</td>
<td>&quot;DECLK&quot; frequency. Example: 16 MHz then choose C0, 1, 2 = 0, 1, 0 (divide by eight, this will give a frequency of 2 MHz).</td>
</tr>
<tr>
<td>C0 = X</td>
<td>RAS banks selected by &quot;B1&quot;.</td>
</tr>
<tr>
<td>C1 = X</td>
<td>This mode allows two RAS~ outputs to go low during an access, and allows byte writing in 16 bit words.</td>
</tr>
<tr>
<td>C2 = X</td>
<td>Column address setup time of 0 ns.</td>
</tr>
<tr>
<td>C3 = X</td>
<td>Row address hold time of 15 ns.</td>
</tr>
<tr>
<td>C4 = 1</td>
<td>Delay CAS~ during write accesses to one clock after RAS~ transitions low.</td>
</tr>
<tr>
<td>C5 = 0</td>
<td>Fall through latches.</td>
</tr>
<tr>
<td>C6 = 1</td>
<td>Access mode 1.</td>
</tr>
<tr>
<td>C7 = 1</td>
<td>Access mode 1.</td>
</tr>
<tr>
<td>C8 = 1</td>
<td>Allow CAS~ to be extended after RAS~ transitions high. Also, allow the WE~ to output to be used as a refresh request (RFRQ~) output indicator.</td>
</tr>
</tbody>
</table>

0 = Program with low voltage level  
1 = Program with high voltage level  
X = Program with either high or low voltage level (don't care condition)

V. 80286 TIMING CALCULATIONS FOR DESIGNS #1 AND #2 AT 32 MHz (80286-16) WITH ONE WAIT STATE DURING NORMAL ACCESSES AND ZERO WAIT STATES IN PAGE MODE ACCESSES (DESIGN #2 ONLY). THE WAITIN~ INPUT OF THE DP8422A SHOULD BE TIED LOW.

1. Minimum S01 high setup time to CLK~ high (D' speed PAL needs 8 ns):
   31.25 ns (one clock period, 32 MHz) - 20 ns (maximum 80286 S0~ delay, #12a) = 11 ns (maximum skew between CLK~ and S0~, S1~ since both gates are in the same package) = 10.25 ns.

2. Maximum address valid time (with respect to CLK~ high during phase 1 in Ts):
   62.5 ns (two clocks 32 MHz) - 31 (80286 address valid delay from previous clock period, #15) + 1 ns (minimum CLK~ valid delay, 74AS00) = 1.25 ns (before CLK~ high phase 1 Ts).

3. Minimum address setup time to ADS~ low (DP8421A-25 needs 14 ns, #404):
   31.25 ns (one clock period) + 1.25 ns (from #2 calculation above) + 2 ns (minimum ADS~ valid delay from CLK~ high, beginning of phase 2 in Ts) = 34.5 ns address setup.

4. Minimum CS setup time to ADS~ low (DP8421A-25 needs 5 ns, #401): 34.5 ns (#3 above) - 10 ns (max 74ALS138 decoder) = 24.5 ns.

5. Determining tRAC during a normal access (RAS~ access time needed by the DRAM):
   156.25 ns (five clock (CLK) periods to do the access) - 4.5 ns (max delay 74AS00 for CLK~) = 151.75 ns (max 'D' speed PAL clocked output delay for ADS~ from CLK~) - 29 ns (ADS~ to RAS~ low max, DP8421A-25 #402) - 7 ns (80286 data setup time #8) - 7 ns (74F245 max delay) = 100.75 ns.
   Therefore the tRAC of the DRAM must be 100.75 ns or less.

6. Determining tCAC during a normal access (CAS~ access time) and column address access time needed by the DRAM:
   156.25 ns (five clock (CLK) periods to do the access) - 4.5 ns (max delay 74AS00 for CLK~) = 151.75 ns (max 'D' speed PAL clocked output delay for ADS~ from CLK~) - 82 ns (ADS~ to RAS~ low max, DP8421A-25 #402) - 7 ns (80286 data setup time #8) - 7 ns (74F245 max delay) = 47.75 ns.
   Therefore the tCAC and the column address access time of the DRAM must be 47.75 ns or less.

7. Determining the column address setup time to CAS~ 0~ low (0 ns needed by the DRAMs) during burst mode accesses for zero wait states (DESIGN #2 ONLY):
   31.25 ns (phase 1 in Ts) + 1.25 ns (#2 above, address valid with respect to CLK~ beginning of phase 1 in Ts) + 2 ns (minimum D' speed PAL clocked output delay from CLK~, ECAS~0,1) + 2 ns (74AS32 min delay to CAS~0~ low) = 36.5 ns.
   This gives 1.5 ns column address setup time to CAS~0~ low (36.5 ns - 35 ns 8421A-25 column address input to output valid, #26).
Interfacing the 80286 to the 8421A

80286

CLK
SO~
S1~
SRDY~

CHIP SELECT
DECODER
74ALS138

A22 A23 MI/O~

CS~
AD, BHE~

ADDRESS

DATA

PAL 16R6D

PCLK
CLK~
SO~
SRDY~

8420CLK~
WIN~
ADS~ (AREQ~)
DTACK~ (DACK2~)
RFQ~
ECAS~0, 1
A12-A21
A11
A2-A11

CO-C9
B0
ECAS~0
ECAS~1

DP8421A

CLK
DECLK
WIN~
ADS~
AREQ~
DTACK~
Q
RFQ~
RAS~0,1
RAS~2,3
R0-R9
CAS~0,1
B1
CAS~2,3

2 BANKS
(UP TO
4 BANKS)
OF 1M-BIT
DRAMS
(16 BITS
PER BANK)

2 BANKS
(UP TO
4 BANKS)
OF 1M-BIT
DRAMS
(16 BITS
PER BANK)

PAL WIN~

PAL ENX~

DIR

TRANSCEIVER

TL/F/10442-1
8. Determining the tCAC (CAS~ access time) needed during burst mode accesses for zero wait states (DESIGN #2 ONLY): 
93.75 ns (three clocks of CLK) − 4.5 ns (74AS00 max delay, CLK~) − 8 ns (D' speed PAL clocked output delay from CLK~, ECAS~0.1) − 10 ns (74AS32 max delay to CAS~0~3 low) − 7 ns (80286 data setup time #8) − 7 ns (74F245 max delay) = 57.25 ns tCAC needed.

9. Determining the column address access time needed during burst mode accesses for zero wait states (DESIGN #2 ONLY):
57.25 ns (*#8 above, tCAC needed by the DRAM) + 1.5 ns (#7 above, column address setup time to CAS~0~3 low) = 58.75 ns.

10. Minimum SRDY~ (Synchronous ReaDY) setup time to CLK low (80286 SRDY input needs 15 ns, #11): 
62.5 ns (two clock periods) − 4.5 ns (74AS00 max delay, CLK~) − 10 ns (D' speed PAL combinational output max delay to SRDY~ low) = 48 ns.

Note: Calculations can be performed for different frequencies, different logic (ALS or CMOS ... etc), and/or different combinations of wait states by substituting the appropriate values into the above equations.

VI. 80286 PAL INPUT AND OUTPUT DESCRIPTIONS FOR DESIGNS #1 AND #2

Inputs:
- CLK~: The inverted clock (CLK) of the 80286.
- PCLK: The half speed clock of the 80286, produced by the 82284.
- S01: The 80286 S0~ 'NANDed' with S1~.
- S0: The S0~ output of the 80286.
- WIN: The 80286 S0~ input low latched throughout the access cycle.
- CS: The DRAM chip select generated from the 80286 addresses.
- DT12: The DTACK~ output of the 8421A.
- A0: The least significant address bit (low byte enable) from the 80286.
- BHE: The high byte enable from the 80286.
- RFQ~: The refresh request output from the 8421A.
- HSA: The High Speed Access output (comparison equal) from the 74ALS6311.
- OE: Output enable of the PAL®.

Outputs:
- ECAS~0: The low byte CAS~ enable, this output also toggles during page mode accesses in design #2.
- ECAS~1: The high byte CAS~ enable, this output also toggles during page mode accesses in design #2.
- SRDY~: This is the ready input to the 80286, it is used to insert wait states into 80286 accesses.
- 8420CLK~: This is the CLOCK and DECLK input to the 8421A. This clock runs at half of the 80286 CLK frequency.
- ADS~: This is the ADS~ and AREQ~ inputs to the 8421A. In design #2 this input stays low thru multiple accesses as long as the accesses are within a page.

NOACC~: This PAL output is low at the end of an 80286 access and stays low until the next access starts.
LREQ~: In Design #2 this output latches that an access request occurred (from the 80286) during an out-of-page access or refresh request during page mode accessing.
WIN~: The latched S0~ output from the 80286.
ENX~: The PAL output used to enable the data transceivers.

80286 PAL EQUATIONS (DESIGN #1)
1. Up to 40 MHz (80286-20)
PAL16R6D
CLK~ PCLK S01 S0~ CS~ DT12~ A0 BHE~ NC3 GND
OE~ ECAS~1 WIN~ ENX~ SRDY~ ADS~ NOACC~ 8420CLK~ ECAS~0 VCC
If (Vcc) /ECAS~0 = /CS~ * S01 * S0~ * /A0 * 8420CLK~ ;READ
+/CS~ */ADS~ */DT12~ */A0 * 8420CLK~ ;WRITE
+/ECAS~ * */ADS~
+/ECAS~ * */SRDY~
If (Vcc) /ECAS~1 = /CS~ * S01 * S0~ * /BHE ~ 8420CLK~ ;READ
+/CS~ */ADS~ */DT12~ */BHE ~ 8420CLK~ ;WRITE
+/ECAS~ * */ADS~
+/ECAS~ * */SRDY~

8/420CLK~ := /PCLK
(NOACC~ := /SRDY~ */ADS~
+/NOACC~ */PCLK
+/NOACC~ */CS~ */ADS~
+/NOACC~ */S01
/ADS~ := /CS~ * S01 * PCLK
+/ADS~ */SRDY~
/SDRY~ := /CS~ */ADS~ */DT12~ */NOACC~ *
/8420CLK~ ;READ
+/SRDY~ */ADS~ */NOACC~
/ENX~ := /CS~ */ADS~
/WIN~ := /S0~ * S01
+/WIN~ */NOACC~
+/WIN~ */PCLK

80286 PAGE MODE PAL EQUATIONS
(DESIGN #2)
2. Up to 40 MHz (80286-20)
PAL16R6D
CLK~ PCLK S01 WIN~ CS~ DT12~ RFQ~ HSA~ A0 GND
OE~ BHE~ ADS~ LREQ~ NOACC~ 8420CLK~ ECAS~1 ECAS~0 SRDY~ VCC
If (Vcc) /SRDY~ = /CS~ */ADS~ *
/DT12~ */NOACC~ */8420CLK~
+/SRDY~ */ADS~ */NOACC~
+/SRDY~ */ADS~ */8420CLK~
/ECAS~0: = /CS~ *S01*WIN~ */A0*/HSA~ *PCLK
+ /CS~ *S01*WIN~ */A0*/HSA~ *ADS~ *PCLK
+ /CS~ *LREQ~ */A0*/HSA~ *WIN~ *PCLK
+ /CS~ */ADS~ */SRDY~ *NOACC~ */A0*PCLK
+ /ECAS~0*/ADS~ *NOACC~

/ECAS~1: = /CS~ *S01*WIN~ */BHE~ */HSA~ *PCLK
+ /CS~ *S01*WIN~ */BHE~ */HSA~ *ADS~ *PCLK
+ /CS~ *LREQ~ */BHE~ */HSA~ *WIN~ *PCLK
+ /CS~ */ADS~ */SRDY~ *NOACC~ */BHE~ *PCLK
+ /ECAS~1*/ADS~ *NOACC~

/8420CLK~ := /PCLK
/NOACC~ := /SRDY~ */ADS~
+ /NOACC~ */PCLK
+ /NOACC~ *CS~ */ADS~
+ /NOACC~ */S01
/LREQ~ := /CS~ *S01*HSA~ */ADS~
+ /CS~ *S01*/RFRQ~ */ADS~
+ /LREQ~ */ADS~
/ADS~ := CS~ *S01*ADS~ */RFRQ~ *PCLK
+ /LREQ~ */HSA~ *PCLK
+ /ADS~ *NOACC~
+ /ADS~ */NOACC~ *RFRQ~ */HSA~
+ /ADS~ */NOACC~ */PCLK

;READ WITH ADS~ LOW
;READ WITH ADS~ HIGH
;READ DELAYED ACCESS

;READ WITH ADS~ LOW
;READ WITH ADS~ HIGH
;READ DELAYED ACCESS

;READ WITH ADS~ LOW
;READ WITH ADS~ HIGH
;READ DELAYED ACCESS

;READ WITH ADS~ LOW
;READ WITH ADS~ HIGH
;READ DELAYED ACCESS
80286/DP8421A Page Mode Timing (Design #1)

- **CLK**
- **8420CLK**
- **CS**
- **CPU S01**
- **ADS**
- **WN**
- **ADDRESS**
- **RFQ**
- **DTACK~ (DT12-)**
- **SRDY~**
- **NOACC~**
- **ECAS~0,1**
- **RAS~0,1**
- **RAS~2,3**
- **CAS~0-3**
- **DATA**

Timing diagram showing:
- READ BANK 0
- WRITE BANK 1
- REFRESH WITH PENDING READ BANK 1 ACCESS

TL/F/10442-2
At high frequencies (CLK > 32 MHz) the WIN~ input may need to be sampled by a flip-flop (clocked by 8420CLK~) before being input to the PAL to meet the setup requirements of the PAL inputs. This would have the effect of delaying ECAS~0,1 becoming valid by one clock period (CLK~) during read accesses, this would not affect the performance of this interface.
80286/DP8421A Page Mode Timing (Design #2)
A PAL Interface for a Dual Access DP8422A/68030/74F632 Error Detecting and Correcting Memory System

I INTRODUCTION

This application note describes a 3 PAL design that interfaces two 68030 microprocessors, both synchronous to the same system clock, to a DP8422A DRAM controller and a 74F632 Error Detection and Correction (EDAC) chip. It is assumed that the reader is already familiar with the 68030 CPU, the DP8422A DRAM controller, the 74F632 EDAC, and the basics of PAL design. The National Semiconductor DP8402A EDAC chip can be used in place of the 74F632 though it is a slower device.

This application note supports the following types of memory accesses:

1. Read accesses with 6 wait states inserted (8 clock periods total in the synchronous mode read access), any single bit errors are automatically corrected before sending the data to the CPU (EDAC unit in always correct mode/error monitoring mode is also described);
2. Write accesses with 3 wait states inserted (5 clock periods total in the synchronous mode write access);
3. Byte write accesses with 7 wait states inserted (9 clock periods total in the synchronous mode byte write access);
4. Burst read accesses with 3 wait states in the burst portion of the access (4 clock periods total per synchronous mode burst read memory access);
5. Scrubbing during DRAM refreshes (6 clock periods total during the refresh if no errors, 8 clock periods total during the refresh if any errors), any single bit errors are corrected. The corrected word is then written back to the DRAM.

II DESCRIPTION OF 25 MHz DUAL ACCESS 68030 SYSTEM INTERFACED TO THE DP8422A AND THE 74F632

This design allows two 68030 microprocessors to access a common error corrected dynamic memory system. The error corrected memory system is implemented using the 74F632 EDAC chip in the always correct mode. Whichever 68030 accessed the memory last has a higher priority. Both 68030s are interfaced to the DRAM in the synchronous mode of operation (the accesses are terminated with the 68030 STERM~ input). This allows the DRAM system to support burst mode accesses.

During read accesses the data is always processed through the EDAC chip (always correct type of system). If a single bit error occurs during a read access this design guarantees correct data to the CPU, but does not write the corrected data back to the DRAM. Single bit soft errors in memory are only corrected (written back to memory) during scrubbing type refreshes. The memory is scrubbed often enough that the probability of accumulating two soft errors in memory is very unlikely.

During read accesses the data is always processed through the 74F632 EDAC chip (i.e., the EDAC data buffers are enabled to provide the data to the CPU). The 74F632 is always put into latch and correct mode during read accesses, even though the data from the memory may be correct. This allows CAS~ to be toggled early (before the CPU has sampled the data), during burst mode accesses, to start accessing the next word of the burst access.

This design drives two banks of DRAM, each bank being 39 bits in width (32 data bits plus 7 check bits) giving a maximum memory capacity of 32 Mbytes of error corrected memory (using 4 M-bit x 1 DRAMs). By choosing a different RAS~ and CAS~ configuration mode (see programming mode bits section of DP8422A data sheet) this application can support 4 banks of DRAM, giving a memory capacity of 64 Mbytes (using 4M-bit x 1 DRAMs, NOTE that when driving 64 Mbytes the timing calculations will have to be adjusted to the greater capacitive load).

The memory banks are interleaved on every four word (32-bit word) boundary. This means that the address bit (A4) is tied to the bank select input of the DP8422A (B1). Address bits A3,2 are tied to the highest row and column address inputs (R9, C9 for 1 Mbit DRAMs) to support burst accesses using nibble mode DRAMs. nibble mode DRAMs must be used! The reason for this is that nibble mode DRAMs support address wrap-around during a burst access. Address wrap-around is needed during an internal cache miss where the 68030 starts a burst memory access on a non-page boundary (i.e., the first of a 4 word burst may have the least significant address bits, "A3,A2" = 10). Given this condition, the CPU expects word 2, word 3, word 0, word 1. On incrementing from word 3 to word 0 the address bit A4 must not change (the nibble page must remain the same). Nibble mode DRAMs support the address wrap-around feature.

Address bits A1, A0 are used to produce the four byte select data strobes, used in byte reads and writes. If the majority of accesses made by the 68030 are sequential, the 68030 can be doing burst accesses most of the time. Each burst of four words can alternate memory banks (address bit A4 tied to DP8422A pin B1), allowing one memory bank to be pre-charging (RAS~ precharge) while the other bank is being accessed. This is a higher performance memory system than a non-interleaved memory system (bank select on the higher address bits). Each separate memory access to the same memory bank will generally require extra wait states to be inserted into the CPU access cycles to allow for the RAS~ precharge time.

The logic shown in this application note forms a complete 68030 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, Port B, and refreshing the DRAM;
B. the insertion of wait states to the processor (Port A and Port B) when needed (i.e., if RAS~ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access ... etc.).
C. performing byte writes and reads to the 32-bit words in memory;
D. normal and burst access operations.

By making use of the enable input on the 74AS244 buffer, this application allows dual access applications. The addresses and chip select are TRI-STATE® through this buffer, the write input (WIN~), lock input (LOCK~), and ECASO-3 ~ inputs must also be able to be TRI-STATE (another 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A allows dual accessing to be performed.

III ANOTHER OPTION FOR A 68030 25 MHz DUAL ACCESS EDAC DESIGN: THE EDAC ERROR MONITORING METHOD IN CONJUNCTION WITH THE 68030 ASYNCHRONOUS LATE RETRY FEATURE

The 68030 dual access EDAC system design could use the error monitoring method in conjunction with the 68030 asynchronous late retry feature, instead of the always correct method (design shown in this application note). The error monitoring method can yield a slight improvement in system performance.

By using the error monitoring method of error correction single read accesses or the first read access during a burst access can be shortened by one clock period, allowing a synchronous read access to have only 5 wait states inserted, 7 clock periods total (compared to 6 wait states, 8 clock periods total when doing the always correct method). All other types of accesses (burst reads, byte writes, word writes, refresh scrubbing) will execute in the same number of clock cycles, and in the same manner as described in this application note.

Read accesses can save one wait state because the data from the DRAM memory is assumed to be correct in the error monitoring system design. Therefore the DRAM data is given directly to the CPU instead of running it through the EDAC chip as was done in the always correct method.

In order to do this design it is required that the asynchronous late retry feature of the 68030 and registered transceivers (74F646) be employed.

The asynchronous late retry feature of the 68030 involves pulling the 68030 input signals "BERR~ and HALT~" both low before the falling clock edge of the last clock cycle of the access. Given that this is done the 68030 will suspend all bus activity until HALT~ is brought high and then will retract the aborted bus cycle (unless that access is not currently needed by the CPU). This feature is useful for the case where an error is detected in the DRAM data. In this case BERR~ and HALT~ are brought low until the data from the DRAM is corrected (by the EDAC chip) and written back to the DRAM. BERR~ and HALT~ are then brought high to continue CPU processing.

Registered transceivers (74F646) are necessary during burst mode read accesses because CAS~ transitions high before the CPU has sampled the DRAM data. The registered transceivers hold the data valid until the CPU samples it during these cases.

A read, read with a single bit error, and burst read access timing are shown at the end of this application note implemen­ting the error monitoring method. The user can see how these access cycles differ from the always correct method access cycles.

IV 68030 25 MHz DUAL ACCESS DESIGN, PROGRAMMING MODE BITS

<table>
<thead>
<tr>
<th>Programming Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0 = 1</td>
<td>RAS~ low four clocks, RAS~ precharge of three clocks</td>
</tr>
<tr>
<td>R1 = 1</td>
<td>DTACK~ 1 is chosen, DTACK~ low first rising CLK edge after access RAS~ is low.</td>
</tr>
<tr>
<td>R2 = 1</td>
<td>No WAIT states during burst accesses</td>
</tr>
<tr>
<td>R3 = 0</td>
<td>R3 = 0</td>
</tr>
<tr>
<td>R4 = 0</td>
<td>R4 = 0</td>
</tr>
<tr>
<td>R5 = 0</td>
<td>R5 = 0</td>
</tr>
<tr>
<td>R6 = 0</td>
<td>If WAITIN~ = 0, add one clock to DTACK~. WAITIN~ may be tied high or low in this application depending upon the number of wait states the user desires to insert into the access.</td>
</tr>
<tr>
<td>R7 = 1</td>
<td>Select DTACK~</td>
</tr>
<tr>
<td>R8 = 1</td>
<td>Select DTACK~</td>
</tr>
<tr>
<td>R9 = X</td>
<td>Non-interleaved mode</td>
</tr>
<tr>
<td>C0 = X</td>
<td>Select based upon the input “DELCLK” frequency. Example: if the input clock frequency is 20 MHz then choose C0,1,2 = 0,0,0 (divide by ten, this will give a frequency of 2 MHz). If DELCLK of the DP8422A is over 20 MHz do an initial divide by two externally and then run that output into the DELCLK input and choose the correct divider.</td>
</tr>
<tr>
<td>C1 = X</td>
<td>C1 = X</td>
</tr>
<tr>
<td>C2 = X</td>
<td>C2 = C2</td>
</tr>
<tr>
<td>C3 = X</td>
<td>C3 = C3</td>
</tr>
<tr>
<td>C4 = 0</td>
<td>C4 = C4</td>
</tr>
<tr>
<td>C5 = 0</td>
<td>C5 = C5</td>
</tr>
<tr>
<td>C6 = 1</td>
<td>C6 = C6</td>
</tr>
<tr>
<td>C7 = 1</td>
<td>C7 = 1 Column address setup time of 0 ns</td>
</tr>
<tr>
<td>C8 = 1</td>
<td>C8 = 1 Row address hold time of 15 ns</td>
</tr>
<tr>
<td>C9 = 1</td>
<td>C9 = 1 Delay CAS~ during write accesses to one clock after RAS~ transitions low</td>
</tr>
<tr>
<td>B0 = 1</td>
<td>B0 = 1 Fall-thru latches</td>
</tr>
<tr>
<td>B1 = 1</td>
<td>B1 = 1 Access mode 1</td>
</tr>
</tbody>
</table>

ECASO~ = 0 Non-extend CAS~
0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either high or low voltage level (don't care condition)
**V 68030 25 MHz WORST CASE TIMING CALCULATIONS**

The worst case access is an access from Port B. This occurs because the time to RAS~ and CAS~ low is longer for the Port B access than; a Port A access, a refresh with scrubbing access, or an access which has been delayed from starting (due to refresh, RAS~ precharge time, or the other Port accessing memory).

A. Worst case time to RAS~ low from the beginning of an access cycle:

\[
40 \text{ ns (T1 clock period of 68030) + 10 ns (PAL16R4D maximum combinational output delay to produce AREQ~) + 41 ns (DP8422A-25 parameter #102, AREQ~ to RAS~ delay maximum)} = 91 \text{ ns}
\]

B. Worst case time to CAS~ low from the beginning of an access cycle:

\[
40 \text{ ns + 10 ns + 94 ns (DP8422A-25 parameter #118a, AREQ~ to CAS~ delay maximum)} = 144 \text{ ns}
\]

C. Worst case time to DRAM data valid:

\[
144 \text{ ns (from "B" above, maximum time to CAS~) + 50 ns (CAS~ access time "tCAC" for a typical 100 ns DRAM)} = 194 \text{ ns}
\]

D. Worst case time to data valid on the EDAC data bus:

\[
194 \text{ ns (from "C" above) + 7 ns (74AS244 maximum delay) = 201 ns}
\]

E. Worst case time until the error flags are valid from the 74F632:

\[
201 \text{ ns (from "D" above) + 31 ns (74F632 maximum time to error flags valid)} = 232 \text{ ns}
\]

F. Worst case time until corrected data is valid from the 74F632:

\[
201 \text{ ns (from "D" above) + 28 ns (74F632 maximum time from data in to corrected data out)} = 229 \text{ ns}
\]

G. Worst case time until corrected data is available at the CPU:

\[
229 \text{ ns (from "F" above) + 7 ns (74F245 maximum delay) = 236 ns}
\]

**VI 68030 25 MHz DUAL ACCESS DESIGN, TIMING CALCULATIONS**

1. Minimum ADS~ low setup time to CLOCK~ high for DTACK~ logic to work correctly (DP8422A-25 needs 25 ns, parameter #40b):

\[
40 \text{ ns (one clock period) + 10 ns (PAL16R4D combinational output maximum that produces AREQ~, ADS~)} = 50 \text{ ns}
\]

2a. Minimum address setup time to ADS~ low (DP8422A-25 needs 14 ns, parameter #404):

\[
40 \text{ ns (one clock period) - 20 ns (assumed 68030 max time to address valid from CLK high) - 6.2 ns (74AS244 buffer delay max) + 2.5 ns (minimum PAL16R4D combinational output delay that produces AREQ~, ADS~)} = 16.3 \text{ ns}
\]

2b. Minimum address setup time to CLK high (used in #3B calculation below):

\[
40 \text{ ns (one clock period) - 20 ns (assumed 68030 max time to address valid from CLK high) - 6.2 ns (74AS244 buffer delay max)} = 13.8 \text{ ns}
\]

3a. Minimum CS~ setup time to ADS~ low (DP8422A-25 needs 5 ns, parameter #401):

\[
16.3 \text{ ns (#2a) - 9 ns (max 74AS138 decoder)} = 7.3 \text{ ns}
\]

3b. Minimum CS~ setup time to CLK high (PAL equations need 0 ns):

\[
13.8 \text{ ns (#2b) - 9 ns (max 74AS138 decoder)} = 4.8 \text{ ns}
\]

4. Determining tRAC during a normal access (RAS~ access time needed by the DRAM):

\[
200 \text{ ns (five and one-half clock periods to get data from the DRAM to the 74F632 data inputs) - 3 ns (74F632 data setup time to mode input S0 high) + 2.5 ns (minimum PAL16R4D combinational output delay for "S0") - 84 ns (from "A" of worst case times, from the beginning of the access to RAS~ low) - 6.2 ns (74F244 DRAM buffer delay maximum)} = 129.3 \text{ ns}
\]

Therefore the tRAC of the DRAM must be 129.3 ns or less.

5. Determining tCAC during a normal access (CAS~ access time) and column address access time needed by the DRAM:

\[
220 \text{ ns (five and one-half clock periods to get data from the DRAM to the 74F632 data inputs) - 3 ns (74F632 data setup time to mode input S0 high) + 2.5 ns (minimum PAL16R4D combinational output delay for "S0") - 138 ns (from "B" of worst case times, from the beginning of the access to CAS~ low) - 6.2 ns (74F244 DRAM buffer delay maximum)} = 75.3 \text{ ns}
\]

Therefore the tCAC of the DRAM must be 75.3 ns or less.

6. Determining the nibble mode access time needed during a burst access:

\[
100 \text{ ns (two and one-half clock periods to do the burst) - 8 ns (PAL16R4D clocked output delay maximum for ENCAS} \sim \text{ output) - 27 ns (DP8422A-25 ECASn} \sim \text{ to CASn} \sim \text{ asserted maximum, parameter #14) - 3 ns (74F632 data setup time to mode input S0 high) + 2.5 ns (minimum PAL16R4D combinational output delay for "S0") - 6.2 ns (74F244 DRAM buffer delay maximum)} = 58.3 \text{ ns}
\]

Therefore the nibble mode access time of the DRAM must be 58.3 ns or less.

7. Maximum time to DTACK1 low (PAL16R4D needs 10 ns setup to CLK):

\[
40 \text{ ns (One clock) - 28 ns (DTACK2 low from CLK high on DP8422A-25, parameter #18) = 12 ns}
\]

8. Minimum STERM~ setup time to CLK (0 ns to CLK rising edge is needed by the 68030):

\[
20 \text{ ns (one-half clock period) - 10 ns (PAL16R4D combinational output maximum)} = 10 \text{ ns}
\]

**Note:** That calculations can be performed for different frequencies and/or different combinations of wait states by substituting the appropriate values into the above equations.
VII PAL INPUT DESCRIPTIONS

- **BCLK** - System Clock
- **CLK** - System Clock
- **CSA** - Chip Select from Port A 68030
- **ASA** - Address Strobe from Port A 68030
- **CSASA** - Chip selected access request from Port A 68030
- **CSB** - Chip Select from Port B 68030
- **ASB** - Address Strobe from Port B 68030
- **DTACK** - Data Transfer ACKnowledge for Port B accesses
- **ATTACKB** - Transfer ACKnowledge for Port B accesses
- **R** - Read/Write ~ (R/W~) indicator from the currently granted CPU
- **CBREQ** - Cache Burst REQuest indicator from the currently granted CPU
- **WCBREQ** - When low this signal indicates either a write access or a non-burst access
- **RFIP** - Indicates that a DRAM refresh is in progress
- **RAS0** - RAS0~ output from the DP8422A DRAM controller
- **WORD** - Indicates a word access (32 bits) as opposed to a byte or multi-byte access (less than 32 bits)
- **GRANTB** - GRANTB output from the DP8422A DRAM controller, when high this output indicates that Port B currently is granted to access the DRAM

VIII PAL OUTPUT DESCRIPTIONS

- **AREQ** - DRAM Access REQuest for Port A 68030
- **AREQ~** - DRAM Access REQuest for Port A 68030
- **COUNT~** - The enable for the shift register counter (outputs D1~6~)
- **D1~6** - Shift register counter, these outputs are used to drive the PAL control outputs in the proper sequence for each access (Port A, Port B, refresh) and are clocked outputs
- **ENCAS** - This output, when low, enables the CAS~ outputs of the DP8422A DRAM controller and is a clocked output
- **EXRF** - This output is used to EXTend the Refresh cycle to allow an access from one of the banks of DRAM, if an error occurs (ERR~ low) the refresh cycle is extended even longer to allow the corrected data to be written back to memory
- **S0~** - This output controls the S0 mode input of the 74F632
- **S1~** - This output controls the S1 mode input of the 74F632
- **TRAN~EN** - This output is used to enable the data transceivers for the currently enabled Port (A or B)
- **OEB~** - This output is used to drive the OEB0~3~ inputs of the 74F632 to provide byte output control of the latched corrected data
- **OECB** - This output controls when to enable the check bits out of the 74F632
- **LEDBo** - This output is used to latch the corrected data in the output latches of the 74F632

IX 68030 25 MHz DUAL ACCESS EDAC SYSTEM DESIGN

PAL EQUATIONS IN ABEL FORMAT

**DP1 device "PAL16R4D"**

- **BCLK** - pin 1; **VCC** - pin 20;
- **CLK** - pin 2; **AREQ~**, **ICSASA~** - pin 19;
- **CSASA~** - pin 3; **AREQB~**, **ICLKL~** - pin 18;
- **CSB~** - pin 4; **D1~**, **D2~** - pin 17;
- **ASB~** - pin 5; **D3~** - pin 16;
- **DTACK~** - pin 6; **D4~**, **D5~** - pin 15;
- **ATTACKB~** - pin 7; **ENCAS~** - pin 14;
- **WCBREQ~** - pin 8; **COUNT~** - pin 13;
- **RFIP~** - pin 9; **RAS0~** - pin 12;
- **GRANTB** - pin 4; **OE~** - pin 11;
- **IAREQ~** = **ICSASA~** & **CLK**
  # #IAREQ~** & **ICSASA~**
  # #IAREQ~ & **ICLKL~**
- **IAREQB~** = **CSB~** & **IASB~** & **CLK**
  # #IAREQB~ & **ICSB~** & **IASB~**
  # #IAREQB~ & **ICLKL~**
- **ICOUNT~** = **IAREQB~** & **IDTACK~** & **ICSASA~**
  # #IAREQB~ & **IATACKB~** & **IASB~**
  # #IRFIP~ & **IRAS0~**;
- **ID1~** = **IAREQ~** & **IDTACK~**
  # #IATACKB~ & **IAREQB~**
  # #IRFIP~ & **IRAS0~**;
- **ID2~** = **D1~** & **D3~** & **ICOUNT~**
  # #D3~ & **IAREQ~** & **IDTACK~** & **RFIP~**;
- **ID3~** = **ID2~** & **ICOUNT~**;
- **IENCAS~** = **IWBREQ~**
  # #D1~
  # #ID2~
  # #D3~
  # #IRFIP~;

**EQUATIONS**

- **EXRF** - pin 19; **VCC** - pin 20;
- **R** - pin 2; **EXRF~** - pin 18;
- **WORD~** - pin 3; **S0~** - pin 18;
- **GRANTB** - pin 4; **S1** - pin 17;
- **RFIP~** - pin 5; **TRAN~EN~** - pin 16;
- **SERR~** - pin 6; **OEB~** - pin 15;
- **D2~** - pin 7; **OECB~** - pin 14;
- **D5~** - pin 8; **TERMA~** - pin 13;
- **D6~** - pin 9; **STERMB~** - pin 12;
- **GND** - pin 10; **OE~** - pin 11;
**EQUATIONS**

**IOEXF** = **IRFIP** & **S1** & **ID2** & **D5** & **D6** & & **SERR**

# **IOEXF** = **IRFIP** & **S1** & **D5** & **D6**
# **IRFIP** & **ID5** & **ISERR**

**IS0 = IR & IWORD & RFIP**

# **ID2** & **D5**
# **IS0 & BCLK**
# **ID5** & **IBCLK**
# **IS0** & **ID5**
# **IS0** & **ID6**
# **IS1 & ISERR** & **IRFIP**

**IS1 = IR & IWORD & RFIP**

# **ID5** & **IBCLK**
# **IS1** & **ID5**
# **IS1 & ID6** & **IR & WORD**
# **IS1 & ID6** & **IRFIP**
# **IS1 & ISERR** & **IRFIP**

**ITRAN_EN** = **R & ID5** & **IBCLK** & **RFIP**

# **ITRAN_EN** = **R & ID5** & **ID6** & **RFIP**
# **R & ID5** & **ISTERMA** & **RFIP**
# **R & ID5** & **ISTERMB** & **RFIP**
# **R & IWORD** & **ID5** & **IBCLK** & **RFIP**
# **R & IWORD** & **ID5** & **IBCLK** & **RFIP**
# **R & IWORD** & **ID5** & **IBCLK** & **RFIP**
# **R & IWORD** & **ID5** & **IBCLK** & **RFIP**
# **R & IWORD** & **ID5** & **IBCLK** & **RFIP**

**IOEBC** = **IR & IWORD & RFIP** & **IS1**

# **IRFIP** & **ID5** & **IBCLK** & **ISERR**
# **IOEBC** & **IRFIP** & **ID5** & **ISERR**
# **IOEBC** & **IRFIP** & **ID5** & **ISERR**
# **IOEBC** & **IRFIP** & **ID5** & **ISERR**
# **IR & IWORD** & **ID5** & **IBCLK**
# **IOEBC** & **IR & IWORD** & **ID5**
# **IOEBC** & **IR & IWORD** & **ID6**

**ISTERMA** = **R & RFIP** & **ID5** & **D6** & **IGRANTB** & **IBCLK**

# **ISTERMA** & **R & RFIP** & **ID5** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **R & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**

**ISTERMB** = **R & RFIP** & **ID5** & **D6** & **IGRANTB** & **IBCLK**

# **ISTERMB** = **R & RFIP** & **ID5** & **ID6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**
# **IR & IWORD & RFIP** & **ID2** & **D6** & **IGRANTB** & **IBCLK**

**IOEB** = **R & ID5** & **IBCLK**

# **IOEB** & **R & ID5**
# **IRFIP** & **ID5** & **IBCLK** & **ISERR**
# **IOEB** & **IRFIP** & **ID5** & **ID6** & **ISERR**
# **IOEB** & **IRFIP** & **ID6** & **ISERR**
# **IR & IWORD** & **ID5** & **IBCLK**
# **IOEB** & **IR & IWORD** & **ID5**
# **IOEB** & **IR & IWORD** & **ID6**

**IOECB** = **IR & IWORD & RFIP** & **IS1**

# **IRFIP** & **ID5** & **IBCLK** & **ISERR**
# **IOECB** & **IRFIP** & **ID5** & **ISERR**
# **IOECB** & **IRFIP** & **ID5** & **ISERR**
# **IOECB** & **IRFIP** & **ID5** & **ISERR**
# **IR & IWORD** & **ID5** & **IBCLK**
# **IOECB** & **IR & IWORD** & **ID5**
# **IOECB** & **IR & IWORD** & **ID6**

**EQUATIONS**

*ILED80 = ID2 & IS0 & S1 & ICOUNT & ICLKe**

# ILED80 & ID3 & IS0 & ICLK

**ISERR** = **ID4** & **SO** & **S1** & **ICOUNT** & **ICLKe**

# **ISERR** & **ICLKe**

**IBERR** = **D4** & **SO** & **S1** & **ICOUNT** & **IMERR** & **ICLKe**

# **IBERR** & **ICOUNT**

**WE** = **IS1 & ID2 & D3 & ICOUNT & IOECB**

**ID4** : = **ID3 & ICOUNT**
**ID5** : = **ID4 & ICOUNT**
**ID6** : = **ID5 & ICOUNT**

**Key: Reading PAL equations**

**EXAMPIE EQUATIONS:**

**IAREQ** = **ICASASA** & **CLK**

# **IAREQ** & **ICASASA**
# **IAREQ** & **ICLKe**

This example reads: the output "AREQ~" will transition low given that one of the following conditions are valid:

1. the input "CASASA~" is low AND the input "CLK" is high, OR
2. the output "AREQ~" is low AND the input "CASASA~" is low, OR
3. the output "AREQ~" is low AND the input "CASASA~" is low.
Control logic in this system needs the following: 3 PAL®s and some logic gates

*CBACK is tied low back to 68030

**FIGURE 1. Block Diagram of Dual Access 68030 Error Detecting and Correcting (74F632) Memory System**
*If WORD is low then 32 bits are being accessed from the memory system.
If WORD is high then less than 32 bits are being accessed from the memory system.

FIGURE 2. Control Logic for 68030 Dual Access EDAC Memory System
FIGURE 3. 68030 EDAC Read Access Timing
FIGURE 4. 68030 EDAC Burst Read Access Timing
FIGURE 5. 68030 EDAC Word Write Access Timing
FIGURE 6. 68030 EDAC Byte Write Access Timing
FIGURE 7. 68030 EDAC DRAM Refresh with Scrubbing
FIGURE 8. 68030 EDAC Write Access during Refresh Timing
FIGURE 9. 68030 EDAC Port B Access during Port A Access
FIGURE 10. 68030 EDAC Error Monitoring Method Using the Asynchronous Late Retry Feature of the 68030
FIGURE 11. 68030 EDAC Error Monitoring Method Using the Asynchronous Late Retry Feature of the 68030
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Physical Dimensions
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A.1 Basic Operators and Theorems

A gate is an electronic circuit which operates on one or more input signals to produce an output signal. There are three basic gates from which all other logic can be realized: AND, OR, and INVERTER gates. Figure A.1.1 shows these three basic gates and their truth table.

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**FIGURE A.1.1. Basic Gates**

To express the function of these gates by Boolean algebra, we need to define Boolean operators as follows:

- Logical Equality
- Negate (Not, Invert, Complement)
- OR (Sum)
- AND (Product)
- Exclusive OR

The function of an AND gate in Figure A.1.1 can be expressed as:

\[ F = A \land B \]

The function of an OR gate and INVERTER can be expressed as:

\[ F = A \lor B \]

\[ F = \overline{A} \]

Boolean operators are logical operators, which are different from arithmetic operators. For example, \( + \) is logical addition; \( \cdot \) is logical multiplication. We call such equations Boolean equations or logic equations.

A number of logic theorems and laws will be used to manipulate and reduce logical equations. These theorems and laws are as follows:

**Theorem 1**  \[ A + 0 = A \]

**Theorem 2**  \[ A \cdot 0 = 0 \]

**Theorem 3**  \[ A + 1 = 1 \]

**Theorem 4**  \[ A \cdot 1 = A \]

**Theorem 5**  \[ A + A = A \]

**Theorem 6**  \[ A \cdot A = A \]

**Theorem 7**  \[ A + \overline{A} = 1 \]

**Theorem 8**  \[ A \cdot \overline{A} = 0 \]

**Theorem 9**  \[ \overline{A} = A \]

**Theorem 10**  \[ A + A \cdot B = A \]

**Theorem 11**  \[ A \cdot (A + B) = A \]

**Theorem 12**  \[ (A + B) \cdot (A + C) = A + B \cdot C \]

**Theorem 13**  \[ A + \overline{A} \cdot B = A + B \]

**Commutative Law**

\[ A + B = B + A \]

\[ A \cdot B = B \cdot A \]

**Associative Law**

\[ A + (B + C) = (A + B) + C = A + (B + C) \]

\[ A \cdot (B \cdot C) = (A \cdot B) \cdot C = A \cdot (B \cdot C) \]

**Distributive Law**

\[ A + (B \cdot C + D) = (A + B) \cdot (A + C) \cdot (A + D) \]

\[ A \cdot (B + C + D) = A \cdot B + A \cdot C + A \cdot D \]

**DeMorgan's Theorem**

\[ (A + B + C) = \overline{A} \cdot \overline{B} \cdot \overline{C} \]

\[ (A \cdot B \cdot C) = \overline{A} + \overline{B} + \overline{C} \]

The complement of any Boolean expression, or a part of any expression, may be found by means of DeMorgan's theorem. Two steps are used to form a complement in this theorem:

1. OR symbols are replaced with AND symbols or AND symbols with OR symbols.
2. Each of the terms in the expression is complemented.

DeMorgan's theorem is one of the most powerful tools for engineering applications. It is very useful for designing with programmable logic devices because it provides a quick and simple conversion method between PRODUCT-OF-SUMS and SUM-OF-PRODUCTS expressions, which will be defined later.
A.2 Derivation of a Boolean Expression

Any logic expression can be reduced to a two-level form and expressed as either a SUM-OF-PRODUCTS (SOP) or PRODUCT-OF-SUMS (POS). Before we define SOP or POS, we need to define "terms".

1. **Product Term**: A product term is a single variable or the logical product of several variables. The variable may or may not be complemented.

2. **Sum Term**: A sum term is a single variable or the sum of several variables. The variables may or may not be complemented.

3. **Normal Term**: A normal term is a product or sum term in which no variable appears more than once.

4. **Minterm**: A minterm is a product term containing every variable once and only once (either true or complemented).

5. **Maxterm**: A maxterm is a sum term containing every variable once and only once (either true or complemented).

For example, the term $A \cdot B \cdot C$ is a product term; $A + B$ is a sum term; $A$ is both a product term and a sum term; $A + B + C$ is neither a product term nor a sum term; $A + \overline{B}$ is a sum term; $A \cdot \overline{B} \cdot \overline{C}$ is a product term; $\overline{B}$ is both a sum term and a product term. We now define two most important forms:

1. **SUM-OF-PRODUCTS Expression**: A sum-of-products expression is a product term or several product terms logically added together.

2. **PRODUCT-OF-SUMS Expression**: A product-of-sums expression is a sum term or several sum terms logically multiplied together.

For example, the expression $\overline{A} \cdot B + A \cdot \overline{B}$ is a sum-of-products expression; $(A + B) \cdot (A + B)$ is a product-of-sums expression.

One prime reason for using sum-of-products or product-of-sums expressions is their straightforward conversion to very simple gating networks. In their purest, simplest form they go into two-level networks, which are networks for which the longest path through which a signal must pass from input to output is two gates long.

When designing a logic circuit, the logic designer works from two sets of known values; the various states which the inputs to the logical network can take, and the desired outputs for each input condition. The logic expression is derived from these sets of values and the procedure is as follows:

1. Construct a table of the input and output values (Table A.2.1 left half).

2a. To derive a SUM-OF-PRODUCTS (SOP) expression:

   A product term column is added listing the inputs $A$, $B$, and $C$ according to their value in the input columns (Table A.2.1). Then the product terms from each row in which the output is a "1" are collected.

   Therefore:
   $$F = \overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} \quad (\text{Eq. A.2.1})$$

2b. To derive a PRODUCT-OF-SUMS (POS) expression:

   A sum term column is added listing the inputs $A$, $B$, and $C$ according to their complement value in the input columns (Table A.2.1). Then the sum terms from each row in which the output is "0" are collected.

   Therefore:
   $$F = \overline{A} \cdot B + C + \overline{A} \cdot B \cdot C + A \cdot B \cdot \overline{C} \quad (\text{Eq. A.2.2})$$

Figure A.2.1 is the logic circuit derived from Eq A.2.1 Figure A.2.2 is derived from Eq. A.2.2.

Eq. A.2.1 Can be simplified as shown below:

$$F = \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C}$$

$$= \overline{A} \cdot B \cdot (\overline{C} + C) + A \cdot B \cdot \overline{C}$$

$$= \overline{A} \cdot B + A \cdot \overline{B} \cdot C$$

$$= B \cdot (\overline{A} + \overline{C})$$

$$= \overline{A} \cdot B + B \cdot \overline{C}$$

Eq. A.2.2 can be simplified as shown:

$$F = (A + B + C) \cdot (A + B + \overline{C}) \cdot (\overline{A} + B + C)$$

$$= (A + B) \cdot (\overline{A} + \overline{C})$$

$$= B \cdot (\overline{A} + \overline{C})$$

$$= \overline{A} \cdot B + B \cdot \overline{C}$$
The two final expressions obtained are identical and can be implemented by the circuit shown in Figure A.2.3. This is much simpler than the circuits in Figures A.2.1 and A.2.2. This simplified procedure is called minimization.

FIGURE A.2.1. Logic Circuits of Eq. A.2.1

FIGURE A.2.2. Logic Circuits of Eq. A.2.2

FIGURE A.2.3. Simplified Logic Circuits
A.3 Minimization

Logic circuits can be represented by logic expressions or so-called logic equations. As discussed, we can minimize the logic circuit through logic equations minimization. For example, Figure A.3.1 can be expressed by Eq. A.3.1.

\[ F = (A \cdot B \cdot C + D) \cdot (B + D) + A \cdot \overline{C} \cdot (B + D) \]  
(Eq. A.3.1)

By using the theorems and laws mentioned in 3.1, we minimize Eq. A.3.1 as follows:

\[ F = A \cdot B \cdot C + B \cdot D + A \cdot B \cdot C \cdot D + D + A \cdot \overline{C} \cdot B + A \cdot \overline{C} \cdot D \]  
Distributive Law

\[ F = A \cdot B \cdot C + D + A \cdot \overline{C} \cdot B + A \cdot \overline{C} \cdot D \]  
Theory 3

\[ F = A \cdot B \cdot (C + \overline{C}) + D \cdot (1 + A \cdot \overline{C}) \]  
Distributive Law

\[ F = A \cdot B + D \]

The minimum SOP expression can now be implemented as the simple AND-OR logic circuits as shown in Figure A.3.2. We can use Boolean Algebra to reduce the number of product terms. However, Karnaugh Mapping and the Quine-McCluskey method are two other powerful tools to minimize the logic equations. We'll discuss Karnaugh Mapping method in the next section.

FIGURE A.3.1. A Random Logic Circuit

FIGURE A.3.2. Minimized Logic Circuit
A.4 K-Map Method

A Karnaugh map, hereafter called a K-map, is a graphical method for representing a Boolean function. It is similar to a truth table in that the K-map supplies the TRUE or FALSE value of a Boolean function for all possible combinations of its logical argument. There are many ways in which a K-map can be arranged. The most important considerations of the arrangement are:

1. There must be a unique location on the K-map for entering the TRUE/FALSE value of the function that corresponds to each combination of input variables.

2. The locations should be arranged so, with minimization mentioned in Section A.3, that they are readily apparent to the trained observer.

The second consideration implies that a successful K-mapping arrangement should point to groups of minterms or maxterms that can be combined into reduced forms. K-maps are also useful in expanding partially reduced expressions into standard forms prior to the minimization process.

The K-map is one of the most powerful tools at the hands of the logic designer. The power of the K-map does not lie in its application of any marvelous new theorems, but rather in its utilization of the remarkable ability of the human mind to perceive patterns in pictorial representations of data. This is not a new idea. Anytime we use a graph instead of a table of numerical data, we are utilizing the human ability to recognize complex patterns and relationships in a graphical representation far more rapidly and surely than in a tabular representation. A few examples of how to create a K-map follow.

First, consider a truth table for two variables. We list all four possible input combinations and the corresponding function values, i.e., the truth tables for AND and OR. (Figure A.4.1)

As an alternative approach, set up a diagram consisting of four small boxes, one for each combination of variables. Place a "1" in any box representing a combination of variables for which the function has the value 1. There is no logical objection to putting "0's" in the other boxes, but they are usually omitted for clarity.

The diagrams in Figure A.4.2(a) are perfectly valid K-maps, but it is more common to arrange the four boxes in a square, as shown in Figure A.4.2(b).

Since there must be one square for each input combination, there must be 2^n squares in a K-map for n-variables. Whatever the number of variables, we may interpret the map in terms of a graphical form of the truth table (Figure A.4.3(a)) or in terms of union and intersection of areas (Figure A.4.3(b)). The K-maps for some other three-variable functions are shown in Figure A.4.4.

Particularly note the functions mapped in Figure A.4.3(a) and A.4.4(b). These are both minterms. Each is represented by one square, obviously, and each one of the eight squares corresponds to one of the eight minterms of three variables. This is the origin of the name minterm. A minterm is the form of Boolean function corresponding to the minimum possible area, other than 0, on a K-map. A maxterm, on the other hand, is the form of Boolean function corresponding to the maximum possible area, other than 1, on a K-map. Figure A.4.3(b) and A.4.4(c) are two examples.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A * B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A + B</th>
</tr>
</thead>
<tbody>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

FIGURE A.4.2. K-Maps for AND and OR
A.4 K-Map Method (Continued)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>A \cdot B \cdot C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
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<td>1</td>
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<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

![K-Map Diagram](TL/L/9992-19)

$$A + B + C = A \cdot B \cdot C$$

(b)

FIGURE A.4.3 K-Maps for 3-Variable AND and OR
FIGURE A.4.4. Sample 3-Variable K-Maps

(a) $A\overline{C} + \overline{A}C$

(b) $AB C$

(c) $A + B + \overline{C}$

(d) $C + \overline{A}B$
A.4 K-Map Method (Continued)

Since each square on a K-map corresponds to a row in a truth table, it is appropriate to number the squares just as we numbered the row. These standard K-maps are shown in Figure A.4.5 for two and three variables. Now, if a function is stated in the form of the minterm list, all we need to do is enter 1's in the corresponding squares to produce the K-map.

If a function is stated as a maxterm list, we can enter 0's in the squares listed or 1's in those not listed. A map showing the 0's of a function is a perfectly valid K-map, although it is more common to show the 1's. For example, the K-map of \(f(A, B, C) = m(0, 2, 3, 7)\) is shown in Figure A.4.6 and the K-map of \(f(A, B, C) = M(0, 1, 5, 6)\) is shown in Figure A.4.7 where \(m\) means minterm, \(M\) means maxterm.

As shown, the K-map can be generated from the truth table on minterm expression or maxterm expression. For the remainder of this section, we will learn how to minimize the minterm expression by using the K-map.

The general principle of this minimization technique is "Any pair of \(n\)-variable minterms which are adjacent on a K-map may be combined into a single product term of \(n - 1\) literals." The definition of "adjacent" should include opposite edges of the K-map, for instance, Figure A.4.8(a) and A.4.8(b) both have a pair of adjacent minterms.

Consider this function

\[f(A, B, C) = m(0, 1, 4, 6)\]

\[= \overline{A} B C + \overline{A} BC + AB \overline{C} + ABC\]

which results on the K-map, on the pattern shown in Figure A.4.9.

Therefore, combine minterms 0 and 1, 4 and 6 to get a minimal expression:

\[f(A, B, C) = A B + AC\]

Figure A.4.10 shows some examples. Notice that it is permissible to include a minterm in several terms if it helps make the term shorter.
A.4 K-Map Method (Continued)

Quite often, some of the possible combinations of input values never occur. In this case, we "don't care" what the function does if these input combinations appear. The K-map makes it easy to take advantage of these "don't care" conditions by letting the "don't care" minterms be 1 or 0, depending on which value results in a simpler expression. Figure A.4.11 shows an example of the use of "don't cares" (redundancies) to simplify the terms.

![K-Map Diagram](image)

**FIGURE A.4.11. Minimization**

When working with larger functions, the tabular reduction developed by Quine and modified by McCluskey is an alternative to the K-map method. The Quine-McCluskey minimization method involves simple, repetitive operations that compare each minterm that is present in a sum-of-minterms expression for a Boolean function to all other minterms with which it may form a combinable grouping.

The reader can refer to "Introduction to Switching Theory and Logic Design" by Hill and Peterson to understand the Quine-McCluskey method.

A.5 Sequential Circuit Elements

Usually the subject of logic design is subdivided into two types: sequential and combinational. A purely combinational logic subsystem has no memory. Its outputs are completely defined by its present inputs. The analysis and design of combinational logic is much easier. A sequential logic subsystem has memory and its outputs are functions of not only present inputs but the previous outputs. Circuits of multiplexer/selector, decoder/encoder, adder, and comparator are examples of combinational circuits. Shift register, counter, state machine, and memory controller are examples of sequential circuits.

**FIGURE A.5.1. Basic Flip-Flops**

<table>
<thead>
<tr>
<th>Dn</th>
<th>Qn + 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tn</th>
<th>Qn + 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Qn</td>
</tr>
<tr>
<td>1</td>
<td>(Q)n</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R</th>
<th>S</th>
<th>Qn + 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Qn</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Qn + 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Qn</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(Q)n</td>
</tr>
</tbody>
</table>
Another memory element type, called a latch, is often described on data sheets with a truth table like the one for the D flip-flop in Figure A.5.1. It is definitely not like a D flip-flop, however, because the output changes as soon as the clock goes high and does not "latch" until the clock falls (if the input changes while the clock is high, the output follows it). Because of this characteristic, a latch is not usable in the synchronous logic.

A.6 State Machine Fundamentals

The relationships among present-state variables, primary input variables, next-state (or excitation) variables, and primary output variables that describe the behaviour of a sequential system can be specified in several ways. As an example, consider the simple sequential system that is shown in Figure A.6.1.

This system has two primary input variables, having four different combinations of values. There is one primary output variable and one state variable. It uses delay for memory. There are only two possible present states: y = 0 and y = 1. When combined with the four input combinations, these give eight different total present states. The values of the next-state variable, Y, and the primary output variable, F, must be specified for each total present state. The tabular arrangement shown in Table A.6.1 is a common method for presenting this information. This descriptive tool is called a state table.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next-State Y</th>
<th>Output F</th>
</tr>
</thead>
<tbody>
<tr>
<td>y = 0</td>
<td>0111</td>
<td>000000</td>
</tr>
<tr>
<td>y = 1</td>
<td>0111</td>
<td>000000</td>
</tr>
</tbody>
</table>

FIGURE A.6.1. A Typical Sequential Circuit

TABLE A.6.1. State Table

FIGURE A.6.2. State Diagram
A.6 State Machine Fundamentals (Continued)

A second method for describing the behavior of a sequential system is the use of a state diagram. This method presents a pictorial representation of the present-state/next-state sequences that apply to the sequential device. State changes are marked with directed arrows, with the primary input and output conditions that apply to each state transfer given beside the arrows. The state diagram for the system of Figure A.6.1 is shown in Figure A.6.2. A slash separates the input information from the output information.

State tables and state diagrams are essential tools in the analysis and design of sequential digital systems. The reader should be familiar with these two tools by reading the references listed in the end of this section.

Because a sequential system has feedback from its outputs to its input, certain types of instabilities and uncertainties can occur. When present, these conditions make the operation of circuit difficult or impossible to describe. They may even render the circuit useless, since its behavior may not be predictable or consistent. Several of these types of problems are listed below.

1. The input or output conditions of the system may be indeterminant. For example, the circuit in Figure A.6.3.

\[
\text{FIGURE A.6.3. Example of Hazard Circuit}
\]

2. The output condition of the system may be unstable, changing even though the external inputs do not change. Figure A.6.4 illustrates an example.

\[
\text{FIGURE A.6.4. Example of Unstable Circuit}
\]

3. The output condition of the system, even though stable, may not be predictable depending upon the primary input conditions. Figure A.6.5 is an example.

However, these problems mentioned above can be avoided by making certain restrictions in the way sequential systems are designed and used. For instance, the following are some restrictions:

1. Avoiding continuing instabilities (oscillations).
2. Allowing only fundamental-mode operation.
3. Allowing only pulse-mode operation.
A.7 Avoiding Logic Hazards

The flexible alternative which PLDs provide to design with standard logic requires care in understanding criteria specific to the new design methodology. Care must be taken in understanding the capabilities of the part chosen and in following the design procedure described later in this chapter. But even careful adherence to the design flow will not avoid some of the more common errors, which are common in other design methodologies, as well as PLDs. This section outlines some of the more common anomalies and suggests how they might be avoided.

HAZARDS AND GLITCHES

Not all devices have the same propagation delay. A hazard may be caused by configuring a set of gates such that a change in the input signals can cause a spurious output signal or "glitch". In combinational circuits, the hazard will be prevented since the outputs are presumed to be a function of steady-state input signals and are not scanned until all transients have stabilized. However, in sequential circuits, particularly where the outputs of such a combinational circuit are used as inputs to a sequential circuit, glitches may occur.

STATIC AND DYNAMIC HAZARDS

Depending on the initial and final value of the output, there can be two classes of hazards. When these values are the same, extraneous output signals result from a static hazard. As an example, the circuit shown in Figure A.7.1 will exhibit an output glitch due to a static hazard when both inputs A and B are high and the control input is changed from high to low. In a perfect world, the output signal would not change, but the propagation delay of the logic gates (in this case the inverter) will cause a momentary low glitch on the otherwise high output, as shown.

![FIGURE A.7.1. Circuit with Static Hazard](TL/L/9992-1)

If the initial and final states of the output of a circuit are different, then an extraneous output results from a dynamic hazard. As an example, this would be characterized by a circuit which moved through an intermediate state before settling in the final configurations, such as a 0-1-0-1 instead of a clean 0-1.

FUNCTION AND LOGIC HAZARDS

The causes of hazards are classed as either function or logic. Function hazards exist when logic is specified with a change in more than one input variable possible simultaneously. Figure A.7.2 shows a truth table which illustrates this. The circuit is intended to move from stable state XYZ = 000 to stable state XYZ = 101. If the input variable X and Z do not change absolutely simultaneously, an output glitch due to a function hazard will occur. Assume both X and Z transition from 0 to 1 at about the same time, but not simultaneously. If X changes before Z, a momentary state of 001 will exist, giving an output 0, which changes to 1 as X changes.

![FIGURE A.7.2. Truth Table Illustrating a Function Hazard](TL/L/9992-2)

Functional glitches can be avoided by assigning the state variables in such a manner that transitions between states require only one variable to change at a time. Unequal delays which occur because of the detailed logic implementation are called logic hazards. These can exist even if only one variable at a time changes, as illustrated by Figure A.7.3. This Karnaugh map displays a logic hazard in the Y input, which moves the circuit from the set XYZ to the set WYZ. Each group shown in Figure A.7.3 represents one product term that is an input to the circuit. In this example, it is an OR gate, and therefore at least one of the product terms must be 1 to give an output of 1. Due to circuit propagation delays, any real-world circuit will move out of the starting sets faster than it moves into the final sets. There is therefore the possibility of a brief interval when neither corresponding product is at 1.
A remedy for this is to ensure that any pair between which a transition may take place are in a single set. In other words, any 1-values which appear next to each other in the K-map must be contained within the same set, as shown in Figure A.7.3.

REMEDIES FOR MORE COMPLEX CIRCUITS

Once the number of terms exceeds two or three, K-maps become increasingly difficult to work with. A remedy for this can be found by adding additional terms to the original Boolean equations. From this, it can be determined whether a logic hazard exists by examining the modified equations. If a variable and its complement appear in separate product terms in the same equation and these product terms contain that are not mutually exclusive, a logic hazard exists. The hazard can be eliminated by generating a new product term to overlay each pair of product terms which pose a logic hazard. The new product term is selected from canonical product terms which differ only by the state of the variable causing the hazard. Hazards can exist irrespective of the design methodology used. In manual design, generation and careful examination of K-maps, particularly multiple inputs for state change, can reveal potential hazards. Computer-aided design tools such as ABEL and CUPL are not completely hazard-free and a similar examination of their results may reveal hazards and require adjustment of minimization level and the addition of redundant terms, as for manual design.

As an example of hazard recognition and correction, consider the circuit shown in Figure A.7.4. The Boolean equation describing this is:

\[ X\overline{Y}Z + WYZ \]

Examining the equation reveals a logic hazard because both \( Y \) and \( \overline{Y} \) appear in separate product terms and inputs \( W \) and \( X \) are not mutually exclusive. The problem can be eliminated in two steps. Firstly, expand the expression to its canonical form, which gives:

\[ WX\overline{Y}Z + WX\overline{Y}Z + WXYZ + WX\overline{Y}Z \]

Secondly, develop a new product term from those which overlay the original two and differ only by the state of the variable causing the hazard, in this case \( Y \). This gives:

\[ X\overline{Y}Z + WX(Y + \overline{Y}) + WYZ \]

\[ = X\overline{Y}Z + WXZ + WYZ \]

In this case, the new product term \( WXZ \) overlays the original and is illustrated on the K-map of Figure A.7.3. Therefore, the addition of an AND gate and an input to the OR gate will result in elimination of the hazard, as shown in Figure A.7.4.

References

Hill & Peterson, "Introduction to Switching Theory and Logical Design".
Kohavi, "Switching and Finite Automata Theory".
Rhyne, "Fundamentals of Digital Systems Designs".
Krieger, "Basic Switching Circuit Theory".
Appendix B
Theory of PLD Testing

B.1 Testing Methods

There are many test methods for LSI circuits, each with its own way of generating and processing test data. These approaches can be divided into two broad categories—concurrent and explicit.\(^2\)

In concurrent approaches, normal user-application input patterns serve as diagnostic patterns. Thus testing and normal computation proceed concurrently. In explicit approaches, on the other hand, special input patterns are applied as tests. Hence, normal computation and testing occur at different times.

**CONCURRENT TESTING**

Systems that are tested concurrently are designed such that all the information transferred among various parts of the system is coded with different types of error detecting codes. In addition, special circuits monitor this coded data continuously and signal detection of any fault.

Different coding techniques are required to suit the different types of information used inside LSI systems. For example, \(m\)-out-of-\(n\) codes (\(n\)-bit patterns with exactly \(m\) 1's and \(n - m\) 0's) are suitable for coding control signals, while arithmetic codes are best suited for coding ALU operands.\(^3\)

The monitoring circuits—checkers—are placed in various locations inside the systems so that they can detect most of the faults. A checker is sometimes designed in a way that enables it to detect a fault in its own circuitry as well as in the monitored data. Such a checker is called a self-checking checker.\(^3\)

Hayes and McCluskey surveyed various concurrent testing methods that can be used with microprocessor-based LSI systems.\(^2\) Concurrent testing approaches provide the following advantages:

- Explicit testing expenses (e.g., for test equipment, down time, and test pattern generation) are eliminated during the life of the system, since the data patterns used in normal operation serve as test patterns.
- The faults are detected instantaneously during the use of the LSI chip, hence the first faulty data pattern caused by a certain fault is detected. Thus, the user can rely on the correctness of his output results within the degree of fault coverage provided by the error detection code used. In explicit approaches, on the other hand, nothing can be said about the correctness of the results until the chip is explicitly tested.
- Transient faults, which may occur during normal operation, are detected if they cause any faulty data pattern. These faults cannot be detected by any explicit testing method.

Unfortunately, the concurrent testing approach suffers from several problems that limit its usage in LSI testing:

- The application patterns may not exercise all the storage elements or all the internal connection lines. Defects may exist in places that are not exercised, and hence the faults these defects would produce will not be detected. Thus, the assumption that faults are detected as they occur, or at least before any other fault occurs, is no longer valid. Undetected faults will cause fault accumulation. As a result, the fault detection mechanism may fail because most error detection codes have a limited capability for detecting multiple faults.
- Using error detecting codes to code the information signals used in an LSI chip requires additional I/O pins. At least two extra pins are needed as error signal indicators. (A single pin cannot be used, since such a pin stuck at the good value could go undetected). Because of constraints on pin count, however, such requirements cannot be fulfilled.
- Additional hardware circuitry is required to implement the checkers and to increase the width of the data carriers used for storing and transferring the coded information.
- Designing an LSI circuit for concurrent testing is a much more complicated task than designing a similar LSI circuit that will be tested explicitly.
- Concurrent approaches provide no control over critical voltage or timing parameters. Hence, devices cannot be tested under marginal timing and electrical conditions.
- The degree of fault coverage usually provided by concurrent methods is less than that provided by explicit methods.

The above-mentioned problems have limited the use of concurrent testing for most commercially available LSI circuits. However, as digital systems grow more complex and difficult to test, it becomes increasingly attractive to build test procedures into the UUT (unit under test) itself. We will not consider the concurrent approach further in this article. For a survey of work in concurrent testing, see Hayes and McCluskey.\(^2\)

**EXPLICIT TESTING**

All explicit testing methods separate the testing process from normal operation. In general, an explicit testing process involves three steps:

- **Generating the test patterns.** The goal of this step is to produce those input patterns which will exercise the UUT under different modes of operation while trying to detect any existing fault.
Applying the test patterns to the UUT. There are two ways to accomplish this step. The first is external testing—the use of special test equipment to apply the test patterns externally. The second is internal testing—the application of test patterns internally by forcing the UUT to execute a self-testing procedure. Obviously, the second method can only be used with systems that can execute programs (for example, with microprocessor-based systems). External testing gives better control over the test process and enables testing under different timing and electrical conditions. On the other hand, internal testing is easier to use because it does not need special test equipment or engineering skills.

Evaluating the responses obtained from the UUT. This step is designed with one of two goals in mind. The first is the detection of an erroneous, which indicates the existence of one or more faults (go/no-go testing). The other is the isolation of the fault, if one exists, in an easily replaceable module (fault location testing). Our interest in this article will be go/no-go testing, since fault location testing of LSI circuits sees only limited use.

Many explicit test methods have evolved in the last decade. They can be distinguished by the techniques used to generate the test patterns and to detect and evaluate the faulty responses (Figure B.1.1). In what follows, we concentrate on explicit testing and present in-depth discussions of the methods of test generation and response evaluation employed with explicit testing.

B.2 Test Generation Techniques
The test generation process represents the most important part of any explicit testing method. Its main goal is to generate those test patterns that, when applied to the UUT, sensitize existing faults and propagate a faulty response to an observable output of the UUT. A test sequence is considered good if it can detect a high percentage of the possible UUT faults; it is considered good, in other words, if its degree of fault coverage is high.

Rigorous test generation should consist of three main activities:
- Selecting a good descriptive model, at a suitable level, for the system under consideration. Such a model should reflect the exact behavior of the system in all its possible modes of operation.
- Developing a fault model to define the types of faults that will be considered during test generation. In selecting a fault model, the percentage of possible faults covered by the model should be maximized, and the test costs associated with the use of the model should be minimized. The latter can be accomplished by keeping the complexity of the test generation low and the length of the tests short. Clearly, these objectives contradict one another—a good fault model is usually found as a result of a trade-off between them. The nature of the fault model is usually influenced by the model used to describe the system.
- Generating tests to detect all the faults in the fault model. This part of test generation is the soul of the whole test process. Designing a test sequence to detect a certain fault in a digital circuit usually involves two problems. First, the fault must be excited; i.e., a certain test sequence must be applied that will force a faulty value to appear at the fault site if the fault exists. Second, the test must be made sensitive to the fault; i.e., the effect of the fault must propagate through the network to an observable output.

Rigorous test generation rests heavily on both accurate descriptive (system) models and accurate fault models. Test generation for digital circuits is usually approached either at the gate-level or at the functional level. The classical approach of modeling digital circuits as a group of connected gates and flip-flops has been used extensively. Using this level of description, test designers introduced many types of fault models, such as the classical stuck-at model. They also assumed that such models could describe physical circuit failures in terms of logic. This assumption has sometimes restricted the number of physical failures that can be modeled, but it has also reduced the complexity of test generation since failures at the elementary level do not have to be considered.

FIGURE B.1.1. LSI Test Technology
Many algorithms have been developed for generating tests for a given fault in combinational networks.\(^1\),\(^4\),\(^5\),\(^6\),\(^7\) However, the complexity of these algorithms depends on the topology of the network; it can become very high for some circuits. Ibarra and Sahni have shown that the problem of generating tests to detect single stuck-at faults in a combinational circuit modeled at the gate level is an NP-complete problem.\(^8\) Moreover, if the circuit is sequential, the problem can become even more difficult depending on the deepness of the circuit's sequential logic.

Thus, for LSI circuits having many thousands of gates, the gate level approach to the test generation problem is not very feasible. A new approach, the functional level, is needed.

Another important reason for considering faults at the functional level is the constraint imposed on LSI testing by a user environment—the test patterns have to be generated without a knowledge of the implementation details of the chip at the gate level. The only source of information usually available is the typical IC catalog, which describes the different modes of operation and describes the general architecture of the circuit. With such information, the test designer finds it easier to define the functional behavior of the circuit and to associate faults with the functions. He can partition the UUT into various modules such as registers, multiplexers, ALUs, ROMs, and RAMs. Each module can be treated as a "black box" performing a specified input/output mapping. These modules can then be tested for functional failures; explicit consideration of faults affecting the internal lines is not necessary. The example given below clarifies the idea.

Consider a simple one-out-of-four multiplexer such as the one shown in Figure B.2.1. This multiplexer can be modeled at the gate level as shown in Figure B.2.1(a), or at the functional level as shown in Figure B.2.1(b).

Many algorithms have been developed for generating tests for a given fault in combinational networks.\(^1\),\(^4\),\(^5\),\(^6\),\(^7\) However, the complexity of these algorithms depends on the topology of the network; it can become very high for some circuits. Ibarra and Sahni have shown that the problem of generating tests to detect single stuck-at faults in a combinational circuit modeled at the gate level is an NP-complete problem.\(^8\) Moreover, if the circuit is sequential, the problem can become even more difficult depending on the deepness of the circuit's sequential logic.

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A possible fault model for the gate-level description is the single stuck-at fault model. With this model, the fault list may contain faults such as the line labeled with \( f \) is stuck at 0, or the control line "C0" is stuck at 1.

At the functional level, the multiplexer is considered a black box with a well-defined function. Thus, a fault model for it may specify the following as possible faults: selection of wrong source, selection of no source, or presence of stuck-at faults in the input lines or in the multiplexer output. With this model, the fault list may contain faults such as source "X" is selected instead of source "Y", or line "Z" is stuck at 1.

Ad hoc methods—which determine what faults are the most probable—are sometimes used to generate fault lists. But if no fault model is assumed, then the tests derived must be either exhaustive or a rather ad hoc check of the functionality of the system. Exhaustive tests are impossible for even small systems because of the enormous number of possible states, and superficial tests provide neither good coverage nor even an indication of what faults are covered.

Once the fault list has been defined, the next step is to find the test patterns required to detect the faults in the list. As previously mentioned, each fault first has to be excited so that an error signal will be generated somewhere in the UUT. Then this signal has to be sensitized at one of the observable outputs of the UUT. The three examples below describe how to excite and sensitize different types of faults in the types of modules usually encountered in LSI circuits.

Consider the gate-level description of the three-bit incrementer shown in Figure B.2.2.

The incrementer output, \( Y_2Y_1Y_0 \) is the binary sum of \( C_i \) and the three-bit binary number \( X_2X_1X_0 \), while \( C_0 \) is the carry-out bit of the sum. Note that \( X_0(Y_0) \) is the least significant bit of the incrementer input (output).

Assume we want to detect the fault "line \( f \) is stuck at 0." To excite that fault we will force a 1 to appear on line \( f \) so that, if it is stuck at 0, a faulty value will be generated at the fault site. To accomplish this both \( X_0 \) and \( C_i \) must be set to 1. To sensitize the faulty 0 at \( f \), we have to set \( X_1 \) to 1; this will propagate the fault to \( Y_2 \) independent of the value of \( X_2 \). Note that if we set \( X_1 \) to 0, the fault will be masked since the AND gate output will be 0, independent of the value at \( f \). Note also that \( X_2 \) was not specified in the above test. However, by setting \( X_2 \) to 1, the fault will propagate to both \( Y_2 \) and \( C_0 \), which makes the response evaluation task easier.

Consider a microprocessor RAM and assume we want to generate a test sequence to detect the fault "accessing
word / in the RAM results in accessing the word / instead." To excite such a fault, we will use the following sequence of instructions (assume a microprocessor with single-operand instructions):

Load the word 00 ... 0 into the accumulator.

Store the accumulator contents into memory address /.

Load the word 11 ... 1 into the accumulator.

Store the accumulator contents into memory address /.

If the fault exists, these instructions will force a 11 ... 1 word to be stored in memory address / instead of 00 ... 0. To sensitize the fault, we need only read what is in memory address /, using the appropriate instructions. Note that the RAM and its fault have been considered at the functional level, since we did not specify how the RAM is implemented.

Consider the program counter (PC) of a microprocessor and assume we want to generate a test sequence that will detect any fault in the incrementing mode of this PC, i.e., any fault that makes the PC unable to be incremented from \( x \) to \( x + 1 \) for any address \( x \). One way to excite this fault is to force the PC to step through all the possible addresses. This can be easily done by initializing the PC to zero and then executing the no-operation instruction \( x + 1 \) times. As a result, the PC will contain an address different than \( x + 1 \). By executing another no-operation instruction, the wrong address can be observed at the address bus and the fault detected. In practice, such an exhaustive test sequence is very expensive, and more economical tests have to be used. Note that, as in the example immediately above, the problem and its solution have been considered at the functional level.

Four methods are currently used to generate test patterns for LSI circuits: manual test generation, algorithmic test generation, simulation-aided test generation, and random test generation.

**MANUAL TEST GENERATION**

In manual test generation, the test designer carefully analyzes the UUT. This analysis can be done at the gate level, at the functional level or at a combination of the two. The analysis of the different parts of the UUT is intended to determine the specific patterns that will excite and sensitize each fault in the fault list. At one time, the manual approach was widely used for medium- and small-scale digital circuits. Then, the formulation of the D-algorithm and similar algorithms eliminated the need for analyzing each circuit manually and provided an efficient means to generate the required test patterns. However, the arrival of LSI circuits and microprocessors required a shift back toward manual test generation techniques, because most of the algorithmic techniques used with SSI and MSI circuits were not suitable for LSI circuits.

Manual test generation tends to optimize the length of the test patterns and provides a relatively high degree of fault coverage. However, generating tests manually takes a considerable amount of effort and requires persons with special skills. Realizing that test generation has to be done economically, test designers are now moving in the direction of automatic test generation.

One good example of manual test generation is the work done by Sridhar and Hayes, who generated test patterns for a simple bit-sliced microprocessor at the functional level. A bit-sliced microprocessor is an array of \( n \) identical ICs called slices, each of which is a simple processor for operands of \( k \) bit length, where \( k \) is typically 2 or 4. The interconnections among the \( n \) slices are such that the entire array forms a processor for \( nk \) bit operands. The simplicity of the individual slices and the regularity of the interconnections make it feasible to use systematic methods for fault analysis and test generation.

Sridhar and Hayes considered a one-bit processor slice as a simplified model for the commercially available bit-sliced processors such as the Am2901. A slice can be modeled as a collection of modules interconnected in a known way. These modules are regarded as black boxes with well-defined input-output relationships. Examples of these functional modules are ALUs, multiplexers, and registers. Combinational modules are described by their truth tables, while sequential modules are defined by their state tables (or state diagrams).

The following fault categories were considered:

- For combinational modules, all possible faults that induce arbitrary changes in the truth table of the module, but that cannot convert it into a sequential circuit.
- For sequential modules, all possible faults that can cause arbitrary changes in the state table of the module without increasing the number of states.

Only one module was assumed to be faulty at any time. To test for the faults allowed by the above-mentioned fault model, all possible input patterns must be applied to each combinational module (exhaustive testing), and a checking sequence to each sequential module. In addition, the responses of each module must be propagated to observable output lines. The tests required by the individual modules were easily generated manually—a direct consequence of the small operand size \( (k = 1) \). And because the slices were identical, the tests for one slice were easily extended to the whole array of slices. In fact, Sridhar and Hayes showed that an arbitrary number of simple interconnected slices could be tested with the same number of tests as that required for a single slice, as long as only one slice was faulty at one time. This property is called C-testability. Note that the use of carry-lookahead when connecting slices eliminates C-testability. Also note that slices with operand sizes equal to 2 or more usually are not C-testable.

The idea of modeling a digital system as a collection of interconnected functional modules can be used in modeling any LSI circuit. However, using exhaustive tests and checking sequences to test individual modules is feasible only for toy systems. Hence, the fault model proposed by Sridhar and Hayes, though very powerful, is not directly applicable to LSI testing.
PATH SENSITIZATION AND THE D-ALGORITHM

One of the classical fault detection methods at the gate and flip-flop level is the D-algorithm\(^1\), \(^5\) employing the path sensitization testing technique.\(^4\) The basic principle involved in path sensitization is relatively simple. For an input \(X_i\) to detect a fault “line \(a\) is stuck at \(j, j = 0, 1\),” the input \(X_i\) must cause the signal \(a\) in the normal (fault-free) circuit to take the value \(j\). This condition is necessary but not sufficient to detect the fault. The error signal must be propagated along some path from its site to an observable output.

To generate a test to detect a stuck-at fault in a combinational circuit, the following path sensitization procedure must be followed:

- **Excitation**—The inputs must be specified so as to generate the appropriate value (0 for stuck-at 1 and 1 for stuck-at 0) at the site of the fault.
- **Error propagation**—A path from the fault site to an observable output must be selected, and additional signal values to propagate the fault signal along this path must be specified.
- **Error propagation**—A path from the fault site to an observable output must be selected, and additional signal values to propagate the fault signal along this path must be specified.
- **Line justification**—Input values must be specified so as to produce the signals values specified in the step above.

There may be several possible choices for error propagation and line justification. Also, in some cases there may be a choice of ways in which to excite the fault. Some of these choices may lead to an inconsistency, and so the procedure must backtrack and consider the next alternative. If all the alternatives lead to an inconsistency, this implies that the fault cannot be detected.

To facilitate the path sensitization process, we introduce the symbol \(D\) to represent a signal which has the value 1 in a normal circuit and 0 in a faulty circuit, and \(\overline{D}\) to represent a signal which has the value 0 in a normal circuit and 1 in a faulty circuit. The path sensitization procedure can be formulated in terms of a cubical algebra\(^1\), \(^5\) to enable automatic generation of test. This also facilitates test generation for more complex fault models and for fault propagation through complex logic elements.

We shall define three types of cubes (i.e., line values specified in positional notation):

- For a circuit element \(E\) which realizes the combinational function \(f\), the “primitive cubes” offer a typical presentation of the prime implicants of \(f\) and \(\overline{f}\). These cubes concisely represent the logical behavior of \(E\).
- A “primitive D-cube of a fault” in a logic element \(E\) specifies the minimal input conditions that must be applied to \(E\) in order to produce an error signal (\(D\) or \(\overline{D}\)) at the output of \(E\).
- The “propagation D-cubes” of a logic element \(E\) specify the minimal input conditions to the logic element that are required to propagate an error signal on an input (or inputs) to the output of that element.

To generate a test for a stuck-at fault in a combinational circuit, the D-algorithm must perform the following:

1. **Fault excitation**—A primitive D-cube of the fault under consideration must be selected. This generates the error signal \(D\) or \(\overline{D}\) at the site of the fault. (Usually a choice exists in this step. The initial choice is arbitrary, and it may be necessary to backtrack and consider another choice).

2. **Implication**—In Step 1 some of the gate inputs or outputs may be specified so as to uniquely imply values on other signals in the circuit. The implication procedure is performed both forwards and backwards through the circuit. Implication is performed as follows: Whenever a previously unspecified signal value becomes specified, all the elements associated with this signal are placed on a list \(B\) and processed one at a time (and removed). For each element processed, it is determined if new values of 0, 1, \(D\), and \(\overline{D}\) are implied, based on the previously specified inputs and outputs. These implied line values are determined by intersecting the test cube (which specifies all the previously determined signal values of the circuit) with the primitive cubes of the element. If any line values are implied, the area specified in the test cube, and the associated gates are placed on the list \(B\). An inconsistency occurs when a value is implied on a line which has been specified previously to a different value. If an inconsistency occurs, the procedure must backtrack to the last point a choice existed, reset all lines to their values at that point, and begin again with the next choice.

3. **D-propagation**—All the elements in the circuit whose output values are unspecified and whose input has some signal \(D\) or \(\overline{D}\) are placed on a list called the D-frontier. In this step, an element from the D-frontier is selected and values are assigned to its unspecified inputs so as to propagate the \(D\) or \(\overline{D}\) on its inputs to one of its outputs. This is accomplished by intersecting the current test cube describing the circuit signal values with a propagation D-cube of the selected element of the D-frontier, resulting in a new test cube. If such intersection is impossible, a new element in the D-frontier is selected. If intersection falls for all the elements in the D-frontier, the procedure backtracks to the last point at which a choice existed.

4. **Implication of D-propagation**—Implication is performed for the new test cube derived in Step 3.

5. Steps 3 and 4 are repeated until the faulty signal has been propagated to an output of the circuit.
PATH SENSITIZATION AND THE D-ALGORITHM (Continued)

6. Line justification—Execution of Steps 1 to 5 may result in specifying the output value of an element E but leaving some of the inputs to the element unspecified. The unspecified inputs of such an element are assigned values so as to produce the desired output value. This is done by intersecting the test cube with any primitive cube of the element which has no specified signal values that differ from those of the test cube.

7. Implication of line justification—Implication is performed on the new test cube derived in Step 6.

8. Steps 6 and 7 are repeated until all specified element outputs have been justified. Backtracking may again be required.

REFERENCES

ALGORITHMIC TEST GENERATION

In algorithmic test generation, the test designer devises a set of algorithms to generate the 1's and 0's needed to test the UUT. Algorithmic test techniques are much more economical than manual techniques. They also provide the test designer with a high level of flexibility. Thus, he can improve the fault coverage of the tests by replacing or modifying parts of the algorithms. Of course, this task is much simpler than modifying the 1's and 0's in a manually generated test sequence.

Techniques that use the gate-level description of the UUT, such as path sensitization and the D-algorithm, can no longer be used in testing complicated LSI circuits. Thus, the problem of generating meaningful sets of tests directly from the functional description of the UUT has become increasingly important. Relatively little work has been done on functional-level testing of LSI chips that are not memory elements. Functional testing of memory chips is relatively simple because of the regularity of their design and also because their components can be easily controlled and observed from the outside. Various test generation algorithms have been developed to detect different types of faults in memories. In the rest of this section we will concentrate on the general problem of generating tests for irregular LSI chips, i.e., for LSI chips which are not strictly memory chips.

It is highly desirable to find an algorithm that can generate tests for any LSI circuit, or at least most LSI circuits. One good example of work in this area is the algorithm proposed by Thatte and Abraham for generating tests for microprocessors. Another approach, pursued by the authors of this article, is a test generation procedure capable of handling general LSI circuits.

THE THATTE-ABRAHAM TECHNIQUE

Microprocessors constitute a high percentage of today's LSI circuits. Thatte and Abraham approached the microprocessor test generation problem at the functional level.

- The test generation procedure they developed was based on:
  - A functional description of the microprocessor at the register-transfer level. The model is defined in terms of data flow among storage units during the execution of an instruction. The functional behavior of a microprocessor is thus described by information about its instruction set and the functions performed by each instruction.
  - A fault model describing faults in the various functional parts of the UUT (e.g., the data transfer function, the data storage function, the instruction decoding and control function). This fault model describes the faulty behavior of the UUT without knowing its implementation details.

The microprocessor is modeled by a graph. Each register in the microprocessor (including general-purpose registers and accumulator, stack, program counter, address buffer, and processor status word registers) is represented by a node of the graph. Instructions of the microprocessors are classified as being of transfer, data manipulation, or branch type. There exists a directed edge (labeled with an instruction) from one node to another if during an execution of the instruction data flow occurs from the register represented by the first node to that represented by the second. Examples of instruction representation are given in Figure B.2.3.

Having described the function or the structure of the UUT, one needs an appropriate fault model in order to derive useful tests. The approach used by Thatte and Abraham is to partition the various functions of a microprocessor into five classes: the register decoding function, the instruction decoding and control function, the data storage function, the data transfer function, and the data manipulation function. Fault models are derived for each of these functions at a higher level and independently of the details of implementation for the microprocessor. The fault model is quite general. Tests are derived allowing any number of faults, but only in one function at a time; this restriction exists solely to cut down the complexity of test generation.
The fault model for the register decoding function allows any possible set of registers to be accessed instead of a particular register. (If the set is null then no register is accessed.) This fault model is thus very general and independent of the actual realization of the decoding mechanism.

For the instruction decoding and control function, the faulty behavior of the microprocessor is specified as follows. When instruction $I_j$ is executed any one of the following can happen:

- Instead of instruction $I_j$, some other instruction $I_k$ is executed. This fault is denoted by $F(I_j / I_k)$.
- In addition to instruction $I_j$, some other instruction $I_k$ is activated. This fault is denoted by $F(I_j / I_j + I_k)$.
- No instruction is executed. This fault is denoted by $F(I_j / \emptyset)$.

Under this specification, any number of instructions can be faulty.

In the fault model for the data storage function, any cell in any data storage module is allowed to be stuck at 0 or 1. This can occur in any number of cells.

The fault model for the data transfer function includes the following types of faults:

- A line in a path used in the execution of an instruction is stuck at 0 or 1.
- Two lines of a path used in the instruction are coupled, i.e., they fail to carry different logic values.

Note that the second fault type cannot be modeled by single stuck-at faults. The transfer paths in this fault model are logical paths and thus will account for any failure in the actual physical paths.

Since there is a variety of designs for the ALU and other functional units such as increment or shift logic, no specific fault model is used for the data manipulation function. It is assumed that complete test sets can be derived for the functional units for a given fault model.

By carefully analyzing the logical behavior of the microprocessor according to the fault models presented above, Thatte and Abraham formulated a set of algorithms to generate the necessary test patterns. These algorithms step the microprocessor through a precisely defined set of instructions and addresses. Each algorithm was designed for detecting a particular class of faults, and theorems were proved which showed exactly the kind of faults detected by each algorithm. These algorithms employ the excitation and sensitization concepts previously described.

To gain insight into the problems involved in using the algorithms, Thatte investigated the testing of an eight-bit microprocessor from Hewlett-Packard. He generated the test patterns for the microprocessor by hand, using the algorithms. He found that 96 percent of the single stuck-at faults that could affect the microprocessor were detected by the test sequence he generated. This figure indicates the validity of the technique.

THE ABADIR-REGHBATI TECHNIQUE

Here we will briefly describe a test generation technique we developed for LSI circuits. We assume that the tests would be generated in a user environment in which the gate- and flip-flop-level details of the chip were not known.

We developed a module-level model for LSI circuits. This model bypasses the gate and flip-flop levels and directly describes blocks of logic (modules) according to their functions. Any LSI circuit can be modeled as a network of interconnected modules such as counters, registers, ALUs, ROMs, RAMs, multiplexers and decoders.

Each module in an LSI circuit was modeled as a black box having a number of functions defined by a set of binary decision diagrams (see box). This type of diagram, a functional description tool introduced by Akers in 1978, is a concise means for completely defining the logical operation of one or more digital functions in an implementation-free form. The information usually found in an IC catalog is sufficient to derive the set of binary decision diagrams describing the functions performed by the different modules in a device. These diagrams—like truth tables and state tables—are amenable to extensive logical analysis. However, unlike truth tables and state tables, they do not have the unpleasant property of growing exponentially with the number of variables involved. Moreover, the diagrams can be stored and processed easily in a digital computer. An important feature of these diagrams is that they state exactly how the module will behave in every one of its operation modes. Such information can be extracted from the module’s diagrams in the form of a set of experiments. Each of these experiments describes the behavior of the module in one of its modes of operation. The structure of these experiments makes them suitable for use in automatic test generation.

We also developed a functional-level fault model describing faulty behavior in the different modules of an LSI chip. This model is quite independent of the details of implementation and covers functional faults that alter the behavior of a module during one of its modes of operation. It also covers stuck-at faults affecting any input or output pin or any interconnection line in the chip.

Using the above-mentioned models, we proposed a functional test generation procedure based on path sensitization and D-algorithm. The procedure takes the module-level model of the LSI chip and the functional description of its modules as parameters and generates tests to detect faults in the fault model. The fault collapsing technique was used to reduce the length of the test sequence. As in the D-algorithm, the procedure employs three basic operations, name-
We also presented algorithmic solutions to the problems of performing these operations on functional modules. For each of the three operations, we gave an algorithm which takes the module's set of experiments and current state (i.e., the values assigned to the module inputs, outputs, and internal memory elements) as parameters and generates all the possible states of the module after performing the required operation.

We have also reported our efforts to develop test sequences based on our test generation procedure for typical LSI circuits. More specifically, we considered a one-bit microprocessor slice C that has all the basic features of the four-bit Am2901 microprocessor slice. The circuit C was modeled as a network of eight functional modules: an ALU, a latch register, an addressable register, and five multiplexers. The functions of the individual modules were described in terms of binary decision diagrams or equivalent sets of experiments. Test capable of detecting various faults covered by the fault model were then generated for the circuit C. We showed that if the fault collapsing technique is used, a significant reduction in the length of the final test sequence results.

The test generation effort was quite straightforward, indicating that the technique can be automated without much difficulty. Our study also shows that for a simplified version of the circuit C the length of the test sequence generated by our technique is very close to the length of the test sequence manually generated by Sridhar and Hayes for the same circuit. We also described techniques for modeling some of the features of the Am2909 four-bit microprogram sequencer that are not covered by the circuit C.

The results of our case study were quite promising and showed that our technique is a viable and effective one for generating tests for LSI circuits.

SIMULATION-AIDED TEST GENERATION

Logic simulation techniques have been used widely in the evaluation and verification of new digital circuits. However, an important application of logic simulation is to interpret the behavior of a circuit under a certain fault or faults. This is known as fault simulation. To clarify how this technique can be used to generate tests for LSI systems, we will first describe its use with SSI/MSI-type circuits.

To generate a fault simulator for an SSI/MSI circuit, the following information is needed:

- the gate-level description of the circuit, written in a special language;
- the initial conditions of the memory elements; and
- a list of the faults to be simulated, including classical types of faults such as stuck-at faults and adjacent pin shorts.

The above is fed to a simulation package which generates the fault simulator of the circuit under test. The resulting simulator can simulate the behavior of the circuit under normal conditions as well as when any faults exist.

Now, by applying various input patterns (either generated by hand, by an algorithm, or at random) the simulator checks to see if the output response of the correct circuit differs from one of the responses of the faulty circuits. If it does, then this input pattern detects the fault which created the wrong output response; otherwise the input pattern is useless. If an input pattern is found to detect a certain fault, this fault is deleted from the fault list and the process continues until either the input patterns or the faults are finished. At the end, the faults remaining in the fault list are those which cannot be detected by the input patterns. This directly measures the degree of fault coverage of the input patterns used.

Two examples of this type of logic simulator are LAMP—the Logic Analyzer for Maintenance Planning developed at Bell Laboratories, and the Testaid III fault simulator developed at the Hewlett-Packard Company. Both work primarily at the gate level and simulate stuck-at faults only. One of the main applications of such fault simulators is to determine the degree of fault coverage provided by a test sequence generated by any other test generation technique.

There are two key requirements that affect the success of any fault simulator:

- the existence of a software model for each primitive element of the circuit, and
- the existence of a good fault model for the UUT which can be used to generate a fault list covering most of the actual physical faults.

These two requirements have been met for SSI/MSI circuits, but they pose serious problems for LSI circuits. If it can be done at all, modeling LSI circuits at the gate level requires great effort. One part of the problem is the lack of detailed information about the internal structure of most LSI chips. The other is the time and memory required to simulate and LSI circuit containing thousands of gates. Another severe problem facing almost all LSI test generation techniques is the lack of good fault models at a level higher than the gate level.

The Abadir-Reghbatii description model proposed in the previous section permits the test designer to bypass the gate-level description and, using binary decision diagrams, to define blocks of logic according to their functions. Thus, the simulation of complex LSI circuits can take place at a higher level, and this eliminates the large time and memory requirements. Furthermore, the Abadir-Reghbatii fault model is quite efficient and is suitable for simulation purposes. In fact, the implication operation employed by the test generation procedure represents the main building block of any fault simulator. It must be noted that fault simulation techniques are very useful in optimizing the length of the test sequence generated by any test generation technique.
BINARY DECISION DIAGRAMS

Binary decision diagrams are a means of defining the logical operation of digital functions. They tell the user how to determine the output value of a digital function by examining the values of the inputs. Each node in these diagrams is associated with a binary variable, and there are two branches coming out from each node. The right branch is the "1" branch, while the left branch is the "0" branch. Depending on the value of the node variable, one of the two branches will be selected when the diagram is processed.

To see how binary decision diagrams can be used, consider the half-adder shown in Figure B.2.4(a). Assume we are interested in defining a procedure to determine the value of C, given the binary values of X and Y. We can do this by looking at the value of X. If $X = 0$, then $C = 0$, and we are finished. If $X = 1$, we look at Y. If $Y = 0$, then $C = 0$, else $C = 1$, and in either case we are finished. Figure B.2.4(b) shows a simple diagram of this procedure. By entering the diagram at the node indicated by the arrow labeled with C and then proceeding through the diagram following the appropriate branches until a 0 or 1 value is reached, we can determine the value C. Figure B.2.4(c) shows the diagram representing the function S of the half-adder.

![Half-Adder Diagram](TL/L/9993-6)

**FIGURE B.2.4.** (a) Half-Adder; (b) Binary Decision Diagram for $C = X \oplus Y$; (c) Binary Decision Diagram for $S = X \cdot Y$

To simplify the diagrams, any diagram node which has two branches as exit branches can be replaced by the variable itself or its complement. These variables are called exit variables. Figure B.2.5 shows how this convention is used to simplify the diagrams describing the half-adder.

![Simplified Half-Adder Diagrams](TL/L/9993-7)

**FIGURE B.2.5 Simplified Binary Decision Diagrams for the Half-Adder**

In the previous discussion, we have considered only simple diagrams in which the variables within the nodes are primary input variables. However, we can expand the scope of these diagrams by using auxiliary variables as the node variables. These auxiliary variables are defined by their diagrams. Thus, when user encounters such a node variable, say $g$, while tracing a path, he must first process the diagram defining $g$ to determine the value of $g$, and then return to the original node and take the appropriate branch. This process is similar to the use of subroutines in high-level programming languages.

For example, consider the full-adder defined by:

$$C_{j+1} = E_j C_j + \overline{E_j} A_j$$

$$S_j = E_j + C_j,$$

where $E_j = A_j + B_j$. Figure B.2.6 shows the diagrams for these three equations. If the user wants to know the value of $C_{j+1}$ when the values of the three primary inputs $A_j$, $B_j$, and $C$ are all 1's, he enters the $C_{j+1}$ diagram, where he encounters

![Full-Adder Diagrams](TL/L/9993-8)

**FIGURE B.2.6.** Binary Decision Diagrams for a Full-Adder
BINARY DECISION DIAGRAMS (Continued)

the node variable $E_j$ by traversing the $E_j$ diagram, he obtains a value of 0. Returning to the original $C_j + y$ diagram with $E_j = 0$ will result in taking the 0 branch and exiting with $C_j + y = A_j = 1$.

Since node variables can refer to other auxiliary functions, we can simply describe complex modules by breaking their functions into small subfunctions. Thus, the system diagram will consist of small diagrams connected in a hierarchical structure. Each of these diagrams describes either a module output or an auxiliary variable.

Akers\textsuperscript{19} described two procedures to generate the binary decision diagram of a combinational function $f$. The first one uses the truth table description of $f$, while the other uses the boolean expression of $f$. A similar procedure can be derived to generate the binary decision diagram for any sequential function defined by a state table.

Binary decision diagrams can be easily stored and processed by a computer through the use of binary tree structures. Each node can be completely defined by an ordered triple: the node variable and two pointers to the two nodes to which its 0 and 1 branches are directed. Binary decision diagrams can be used in functional testing.\textsuperscript{20}

REFERENCES

RANDOM TEST GENERATION
This method can be considered the simplest method for testing a device. A random number generator is used to simultaneously apply random input patterns both to the UUT and to a copy of it known to be fault-free. (This copy is called the golden unit.) The results obtained from the two units are compared, and if they do not match, a fault in the UUT is detected. This response evaluation technique is known as comparison testing; we will discuss it later. It is important to note that every time the UUT is tested, a new random test sequence is used.

The important question is how effective the random test is, or, in other words, what fault coverage a random test of given length provides. This question can be answered by employing a fault simulator to simulate the effect of random test patterns of various lengths. The results of such experiments on SSI and MSI circuits show that random test generation is most suitable for circuits without deep sequential logic. However, by combining random patterns with manually generated ones, test designers can obtain very good results.

The increased sequentiality of LSI circuits reduces the applicability of random testing. Again, combining manually generated test patterns with random ones improves the degree of fault coverage. However, two factors restrict the use of the random test generation technique:

- The dependency on the golden unit, which is assumed to be fault-free, weakens the level of confidence in the results.
- There is no accurate measure of how effective the test is, since all the data gathered about random tests are statistical data. Thus, the amount of fault coverage provided by a particular random test process is unpredictable.

B.3 Response Evaluation Techniques
Different methods have been used to evaluate UUT responses to test patterns. We restrict our discussion to the case where the final goal is only to detect faults or, equivalently, to detect any wrong output response. There are two ways of achieving this goal—using a good response generator or using a compact testing technique.

GOOD RESPONSE GENERATION
This technique implements an ideal strategy: comparing UUT responses with good response patterns to detect any faulty response. Clearly, the key problems are how to obtain a good response and at what stage in the testing process that response will be generated. In current test systems, two approaches to solving these problems are taken—stored response testing and comparison testing.

STORED RESPONSE TESTING
In stored response testing, a one-shot operation generates the good response patterns at the end of the test generation stage. These patterns are stored in an auxiliary memory (usually a ROM). A flow diagram of the stored response testing technique is shown in Figure B.3.1.

Different methods can be used to obtain good responses of a circuit to a particular test sequence. One way is to do it manually by analyzing the UUT and the test patterns. This method is the most suitable if the test patterns were generated manually in the first place.

The method most widely used to obtain good responses from the UUT is to apply the test patterns either to a known good copy of the UUT—the golden unit—or to a software-simulated version of the UUT. Of course, if fault simulation techniques were used to generate the test patterns, the UUT's good responses can be obtained very easily as a partial product from the simulator.

FIGURE B.3.1. Stored Response Testing
The use of a known good device depends on the availability of such a device. Hence, different techniques must be used for the user who wants to test his LSI system and for the designer who wants to test his prototype design. However, golden units are usually available once the device goes into production. Moreover, confidence in the correctness of the responses can be increased by using three or five good devices together to generate the good responses.

The major advantage of the stored response technique is that the good responses are generated only once for each test sequence, thus reducing the cost of the response evaluation step. However, the stored response technique suffers from various disadvantages:

- Any change in the test sequence requires the whole process to be repeated.
- A very large memory is usually needed to store all the good responses to a reasonable test sequence, because both the length and the width of the responses are relatively large. As a result, the cost of testing equipment increases.
- The speed with which the test patterns can be applied to the UUT is limited by the access time of the memory used to store the good responses.

COMPARISON TESTING

Another way to evaluate the responses of the UUT during the testing process is to apply the test patterns simultaneously to both the UUT and a golden unit and to compare their responses to detect any faulty response. The flow diagram of the comparison testing technique is shown in Figure B.3.2. The use of comparison testing makes possible the testing of the UUT at different speeds under different electrical parameters, given that these parameters are within the operating limits of the golden unit, which is assumed to be ideal.

Note that in comparison testing the golden unit is used to generate the good responses every time the UUT is tested. In stored response testing, on the other hand, the golden unit is used to generate the good responses only once.

The disadvantages of depending on a golden unit are more serious here, however, since every explicit testing process requires one golden unit. This means that every tester must contain a golden copy of each LSI circuit tested by that tester.

One of the major advantages of comparison testing is that nothing has to be changed in the response evaluation stage if the test sequence is altered. This makes comparison testing highly desirable if test patterns are generated randomly.

COMPACT TESTING

The major drawback of good response generation techniques in general, and stored response testing in particular, is the huge amount of response data that must be analyzed and stored. Compact testing methods attempt to solve this by compressing the response data R into a more compact from \( f(R) \) from which most of the fault information in R can be derived. Thus, because only the compact form of the good responses has to be stored, the need for large memory or expensive golden units is eliminated. An important property of the compression function \( f \) is that it can be implemented with simple circuitry. Thus, compact testing does not require much test equipment and is especially suited for field maintenance work. A general diagram of the compact testing technique is shown in Figure B.3.3.

Several choices for the function \( f \) exist, such as “the number of 1’s in the sequence,” “the number of 0 to 1 and 1 to 0 transitions in the sequence” (transition counting), or “the signature of the sequence” (signature analysis). For each compression function \( f \), there is a slight probability that a response \( R_1 \) different from the fault-free response \( R_0 \) will be compressed to a form equal to \( f(R_0) \), i.e., \( f(R_1) = f(R_0) \). Thus, the fault causing the UUT to produce \( R_1 \) instead of \( R_0 \) will not be detected, even though it is covered by the test patterns.

The two compression functions that are the most widely accepted commercially are transition counting and signature analysis.

![Figure B.3.2. Comparison Testing](image-url)
**Transition Counting**

In transition counting, the number of logical transitions (0 to 1 and vice versa) is computed at each output pin by simply running each output of the UUT into a special counter. Thus, the number of counters needed is equal to the number of output pins observed. For every \( m \)-bit output data stream (at one pin), an \( n \)-bit counter is required, where \( n = \lceil \log_2 m \rceil \).

As in stored response testing, the transition counts of the good responses are obtained by applying the test sequence to a golden copy of the UUT and counting the number of transitions at each output pin. This latter information is used as a reference in any explicit testing process.

In the testing of an LSI circuit by means of transition counting, the input patterns can be applied to the UUT at a very high rate, since the response evaluation circuitry is very fast. Also, the size of the memory needed to store the transition counts of the good responses can be very small. For example, a transition counting test using 16 million patterns at a rate of 1 MHz will take 16 seconds, and the compressed stored response will occupy only \( K \) 24-bit words, where \( K \) is the number of output pins. This can be contrasted with the 16 million \( K \)-bit words of storage space needed if regular stored response testing is used.

The test patterns used in a transition counting test system must be designed such that their output responses maximize the fault coverage of the test. The example below shows how this can be done.

Consider the one-out-of-four multiplexer shown in Figure B.3.4. To check for multiple stuck-at faults in the multiplexer input lines, eight test patterns are required, as shown in Table B.3.1. The sequence of applying these eight patterns to the multiplexer is not important if we want to evaluate the output responses one by one. However, this sequence will greatly affect the degree of fault coverage if transition counting is used. To illustrate this fact, consider the eight single stuck-at faults in the four input lines \( X_1, X_2, X_3 \) and \( X_4 \) (i.e., \( X_1 \) stuck-at 0, \( X_1 \) stuck-at 1, \( X_2 \) stuck-at 0, and so on). Each of these faults will be detected by only one pattern among the eight test patterns. For example, the fault “\( X_1 \) stuck-at 0” will be detected by the first test pattern in Table B.3.1, but the other seven test patterns will not detect this fault. Now, suppose we want to use transition counting to evaluate the output responses of the multiplexer. Applying the eight test patterns in the sequence shown in Table B.3.1 (from top to bottom) will produce the output response 10101010 (from left to right), with a transition count of seven. Any possible combination of the eight faults described above will change the transition count to a number different from seven, and the fault will be detected. (Note that no more than four of the eight faults can occur at any one time.) Thus, the test sequence shown in Table B.3.1 will detect all single and multiple stuck-at faults in the four input lines of the multiplexers.

Now, if we change the sequence of the test patterns to the one shown in Table B.3.2, the fault coverage of the test will decrease considerably. The output responses of the sequence of Table B.3.2 will be 11001100, with a transition count of three. As a result, six of the eight single stuck-at faults will not be detected, because the transition count of the six faulty responses will remain three. For example, the fault “\( X_1 \) stuck-at 1” will change the output response to 11011100, which has a transition count of three. Hence, this fault will not be detected. Moreover, most of the multiple combinations of the eight faults will not change the transition count of the output, and hence they will not be detected either.

It is clear from the above example that the order of applying the test patterns to the UUT greatly affects the fault coverage of the test. When testing combinational circuits, the test designer is completely free to choose the order of test patterns. However, he cannot do the same with test patterns for sequential circuits. More seriously, because he is dealing with LSI circuits that probably have multiple output lines, he will find that a particular test sequence may give good results at some outputs and bad results at others. One way to solve these contradictions is to use simulation techniques to find the optimal test sequence. However, because of the limitations discussed here, transition counting cannot be recognized as a powerful compact LSI testing method.
TABLE B.3.1. The Eight Test Patterns Used for Testing the Multiplexer of Figure B.3.4

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<th>S1</th>
<th>X1</th>
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<th>X3</th>
<th>X4</th>
<th>Y</th>
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TABLE B.3.2. A Different Sequence of the Eight Multiplexer Test Patterns

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SIGNATURE ANALYSIS

In 1977 Hewlett-Packard Corporation introduced a new compact testing technique called signature analysis, intended for testing LSI systems. In this method, each output response is passed through a 16-bit linear feedback shift register whose contents \( f(R) \), after the test patterns have been applied, are called the test signature. Figure B.3.5 shows an example of a linear feedback shift register used in signature analysis.

The signature provided by linear feedback shift registers can be regarded as a unique fingerprint—hence, test designers have extremely high confidence in these shift registers as tools for catching errors. To better understand this confidence, let us examine the 16-bit linear feedback shift register shown in Figure B.3.5. Let us assume a data stream of length \( n \) is fed to the serial data input line (representing the output response to be evaluated). There are \( 2^n \) possible combinations of data streams, and each one will be compressed to one of the \( 2^{16} \) possible signatures. Linear feedback shift registers have the property of equally distributing the different combinations of data streams over the different signatures. This property is illustrated by the following numerical examples.

- Assume \( n = 16 \). Then each data stream will be mapped to a distinctive signature (one-to-one mapping).
- Assume \( n = 17 \). Then exactly two data streams will be mapped to the same signature. Thus, for a particular data stream (the UUT good output response), there is only one other data stream (a faulty output response) that will have the same signature; i.e., only one fault response out of \( 2^{17} - 1 \) possible faults will not be detected.
- Assume \( n = 18 \). Then four different data streams will be mapped to the same signature. Hence, only three faults out of \( 2^{18} - 1 \) possible faults will not be detected.

We can generalize the results obtained above. For any response data stream of length \( n > 16 \), the probability of missing a faulty response when using a 16-bit signature analyzer is

\[
\frac{2^n - 16 - 1}{2^n - 1} \approx 2^{-16}, \text{ for } n > 16.
\]

Hence, the possibility of missing an error in the bit stream is very small (on the order of 0.002 percent). Note also that a great percentage of the faults will affect more than one output pin—hence the probability of not detecting these kinds of faults is even lower.

![Figure B.3.5. The 16-Bit Linear Feedback Shift Register Used In Signature Analysis](image-url)
Signature analysis provides a much higher level of confidence for detecting faulty output responses than that provided by transition counting. But, like transition counting, it requires only very simple hardware circuitry and a small amount of memory for storing the good signatures. As a result, the signatures of the output responses can be calculated even when the UUT is tested at its maximum speed. Unlike transition counting, the degree of fault coverage provided by signature analysis is not sensitive to the order of the test patterns. Thus, it is clear that signature analysis is the most attractive solution to the response evaluation problem.

The rapid growth of the complexity and performance of digital circuits presents a testing problem of increasing severity. Although many testing methods have worked well for SSI and MSI circuits, most of them are rapidly becoming obsolete. New techniques are required to cope with the vastly more complicated LSI circuits.

In general, testing techniques fall into the concurrent and explicit categories. In this article, we gave special attention to explicit testing techniques, especially those approaching the problem at the functional level. The explicit testing process can be partitioned into three steps: generating the test, applying the test to the UUT, and evaluating the UUT’s responses. The various testing techniques are distinguished by the methods they used to perform these three steps. Each of these techniques has certain strengths and weaknesses.

We have tried to emphasize the range of testing techniques available, and to highlight some of the milestones in the evolution of LSI testing. The details of an individual test method can be found in the source we have cited.

References
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NS Package Number J20A

All dimensions are in inches (millimeters)

24 Lead Ceramic Dual-In-Line Package (J)
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Pioneer
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Pioneer Standard
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Time Electronics
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Time Electronics
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Zeus Components
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Stafford
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(613) 226-8840

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St. Laurent
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(514) 355-1000
Zentronics
(514) 737-9700
Willowdale
ElectroSonic Inc.
(416) 494-1666
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<td>(801) 322-4747</td>
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<td>(414) 782-1818</td>
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