INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input waveforms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types of shift registers and RAMs (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage gold doped process utilizing a collector sinker to minimize VCE SAT.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost.

Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions (V&lt;sub&gt;a&lt;/sub&gt; – V&lt;sub&gt;b&lt;/sub&gt;) – 17V</th>
<th>Value</th>
<th>Units</th>
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<tr>
<td>I&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>C&lt;sub&gt;In&lt;/sub&gt; = 0.0022 μF, R&lt;sub&gt;IN&lt;/sub&gt; = 0 Ω</td>
<td>15</td>
<td>ns</td>
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<td>C&lt;sub&gt;L&lt;/sub&gt; = 0.0001 μF, R&lt;sub&gt;L&lt;/sub&gt; = 50 Ω</td>
<td>30</td>
<td>ns</td>
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<td>t&lt;sub&gt;R&lt;/sub&gt;</td>
<td>R&lt;sub&gt;0&lt;/sub&gt; = 50 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 1000 pF</td>
<td>25</td>
<td>ns</td>
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<td>t&lt;sub&gt;f&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = – V&lt;sub&gt;b&lt;/sub&gt; = 0 V, I&lt;sub&gt;OUT&lt;/sub&gt; = – 1 mA</td>
<td>150</td>
<td>ns</td>
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Positive Output Voltage Swing

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<tr>
<th>Parameter</th>
<th>Conditions (V&lt;sub&gt;a&lt;/sub&gt; – V&lt;sub&gt;b&lt;/sub&gt;) – 17V</th>
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<tbody>
<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 10 mA, I&lt;sub&gt;OUT&lt;/sub&gt; = 1 mA</td>
<td>17</td>
<td>mA</td>
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Negative Output Voltage Swing

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<tr>
<th>Parameter</th>
<th>Conditions (V&lt;sub&gt;a&lt;/sub&gt; – V&lt;sub&gt;b&lt;/sub&gt;) – 17V</th>
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<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 10 mA</td>
<td>7.5</td>
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On Supply Current (V<sub>a</sub>):

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<tr>
<th>Parameter</th>
<th>Conditions (V&lt;sub&gt;a&lt;/sub&gt; – V&lt;sub&gt;b&lt;/sub&gt;) – 17V</th>
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<tr>
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<td>7.5</td>
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<td>25</td>
<td>ns</td>
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<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt; = 10 mA, I&lt;sub&gt;OUT&lt;/sub&gt; = 1 mA</td>
<td>28</td>
<td>mA</td>
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<table>
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<th>Conditions (V&lt;sub&gt;a&lt;/sub&gt; – V&lt;sub&gt;b&lt;/sub&gt;) – 17V</th>
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The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent—derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, \( P_{DC} \)
3. Average ac power, \( P_{AC} \)
4. Numbers of drivers per package, \( n \)

From the package heat sink, and maximum ambient temperature one can determine \( P_{MAX} \), which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

\[
P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \quad (1)
\]

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

\[
P_{DC} = P_{IN} + P_{OFF} + P_{ON} \quad (2)
\]

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored. Thus:

\[
P_{DC} = P_{ON} = \frac{(V^+ - V^-)^2}{R_{eq} \times (DC)}
\]

where:

- \( V^+ - V^- \) = Total voltage across the driver
- \( R_{eq} \) = Equivalent device resistance in the "ON" state
- \( = V^+ - V^- / IS_{(ON)} \) \quad (3)
- \( DC \) = Duty Cycle
- \( "ON" \) Time
- \( = "ON" \) Time ÷ "OFF" Time

For the DS0025, \( R_{eq} \) is typically 1 kΩ while \( P_{ON} \) is typically 600Ω for the DS0026. Graphical solutions for \( P_{DC} \) appear in Figure 1. For example if \( V^+ = +5V, V^- = -12V, R_{eq} = 500Ω, \) and DC = 25%, then \( P_{DC} = 145 mW \). However, if the duty cycle was only 5%, \( P_{DC} = 29 mW \). Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

\[
P_{AC} = \frac{(V^+ - V^-)^2 \times f \times C_L}{2} \quad (4)
\]

where:
- \( f \) = Operating frequency
- \( C_L \) = Load capacitance

Graphical solutions for \( P_{AC} \) are illustrated in Figure 2. Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.
A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or approximately 20 MM5013’s.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. Figures Al-3, Al-4, All-2 and All-3 illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load $C_L$ being reflected (usually as $C_{L,ref}$) into the driver; and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{V_{OUT PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic “0” to logic “1” levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, “rise time” as used in this note is “voltage fall” and “fall time” is “voltage rise”.

Power Supply Decoupling

Although power supply decoupling is a widespread and accepted practice, the question often rises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1 μF decoupling to ground at the $V_a$ and $V_b$ supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the $V_b$ lead. If the external interconnecting wire from the driving circuit to the $V_b$ lead is electrically long or has significant dc resistance, the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if $V_b$ is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed $V_{SS}$, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in Figure 3. In this instance, a small damping resistor is inserted between the output of the clock driver and the load. The critical value for $R_S$ is given by:

$$R_S = 2 \sqrt{\frac{L_S}{C_L}}$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in $R_S$ can approach $(V_a - V_b)^2 f CL$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of $t_r$ and $t_f$ by use of damping resistors cannot be tolerated. Figure 4 shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

$$t_f(\text{MAX}) - t_r(\text{MAX}) \leq 2.2 R_S C_L$$

FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot
Cross Talk: Voltage spikes from \( \phi_1 \) may be transmitted to \( \phi_2 \) (and vice versa) during the transition of \( \phi_1 \) to MOS logic “1”. The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Figure 5 illustrates the problem.

Input Capacitive Coupling
Generally, MOS shift registers are powered from \(+5V\) and \(-12V\) supplies. A level shift from the TTL levels \(+5V\) to MOS levels \(-12V\) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION
The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guidelines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

REFERENCES

APPENDIX I
DS0025 Circuit Operation
The schematic diagram of the DS0025 is shown in Figure 7. With the TTL driver in the logic “0” state Q1 is “OFF” and Q2 is “ON” and the output is at approximately one \( V_{BE} \) below the \( V^+ \) supply.
When the output of the TTL driver goes high, current is supplied to the base of Q1, through CIN, turning it “ON.” As the collector of Q1 goes negative, Q2 turns “OFF.” Diode CR2 assures turn-on of Q1 prior to Q2’s turn-off minimizing current spiking on the V+ line, as well as providing a low impedance path around Q2’s base emitter junction.

The negative voltage transition (to MOS logic “1”) will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns “ON” and Q2 turns “OFF” charging the load to within a VBE of the V+ supply.

### Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, CL, the available input current and total voltage swing. As shown in Figure 8, the input current must charge the Miller capacitance of Q1, CTC, as well as supply sufficient base drive to Q1 to discharge CL rapidly.

By inspection:

\[
\begin{align*}
I_{IN} &= I_{M} + I_B + I_{R1} \\
I_{IN} &= I_{M} + I_B, \text{ for } I_M > I_{R1} \text{ and } I_B > I_{R1} \\
I_B &= I_{IN} - C_{TC} \frac{\Delta V}{\Delta t} \\
I_C &= I_B h_{FEQ1} - I_L + I_M
\end{align*}
\]

If the current through R2 is ignored,

\[
I_C = I_B h_{FEQ1} - I_L + I_M
\]

where:

\[
I_L = C_L \frac{\Delta V}{\Delta t}
\]

Combining equations AI-1, AI-2, and AI-3 yields:

\[
\frac{\Delta V}{\Delta t} \left[ C_L + C_{TC} (h_{FEQ1} + 1) \right] = h_{FEQ1} I_{IN}
\]

or

\[
t_r = \frac{[C_L + (h_{FEQ1} + 1)C_{TC}] \Delta V}{h_{FEQ1} I_{IN}}
\]

Equation (AI-5) may be used to predict tr as a function of CL and ΔV. Values for CTC and hFE are 10 pF and 25 pF respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

\[
\frac{(1000 \text{ pF} + 250 \text{ pF})(17\text{V})}{(50 \text{ mA})(20)}
\]

or 21 ns may be expected for V+ = 5.0V, V- = −12V. Figure 9 gives rise time for various values of CL.

### Fall Time Considerations

The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, CL, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated with the circuit of Figure 10. In actual practice, the base drive to Q2 drops as the output voltage rises toward V+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V+. The result is that equation (AI-7) predicts conservative values of tf for the output voltage at the beginning of the voltage rise and optimistic values at the end. Figure 11 shows tf as function of CL.
Assuming $h_{FE2}$ is a constant of the total transition:

$$\Delta V = \frac{V^+ - V^-}{2R2} C_{TCQ1} + C_L/h_{FEQ1} + 1 \quad (A1-6)$$

or

$$t_r \approx 2R2 \left( C_{TCQ1} + \frac{C_L}{h_{FEQ1} + 1} \right) \quad (A1-7)$$

**DS0025 Input Drive Requirements**

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but $t_{ON}$ and $t_r$ will be somewhat degraded.

**Input Capacitor Selection**

The DS0025 may be operated in either the logically controlled mode (pulse width out = pulse width in) or $C_{IN}$ may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.

The logic “1” output impedance of the DM7440 is approximately 65Ω and the peak current ($I_{MAX}$) is about 50 mA. The pulse width for $C_{IN} = 2.2$ nF is:

$$t_{PW} = \frac{25 \text{ ns} + 150 \text{ ns}}{2} + \frac{(65Ω)(2.2 \text{ nF}) \ln}{2.5 \text{ mA}} $$

A plot of pulse width for various types of drivers is shown in Figure 13. For applications in which the output pulse width is logically controlled, $C_{IN}$ should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (A1-10).

**DC Coupled Operation**

The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in Figure 14 driving the address or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DH0034 may be employed as shown in Figure 15. Finally, the level shift may be accomplished using PNP transistors as shown in Figure 16.
APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in Figure 17. The device is typically AC coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q4, Q5, and Q6 are "OFF" allowing Q7 and Q8 to come "ON." R9 assures that the output will pull up to within a VBE of V1 volts. When the TTL input starts toward logic "1," current is supplied via CIN to the bases of Q5 and Q6 turning them "ON." Simultaneously, Q7 and Q8 are snapped "OFF." As the input voltage rises (to about 1.2V), Q1 and Q4 turn-on. Multiple emitter transistor Q1 provides additional base drive to Q5 and Q6 assuring their complete and rapid turn-on. Since Q7 and Q8 were rapidly turned "OFF," minimal power supply current spiking will occur when Q9 comes "ON."
Q4 now provides sufficient base drive to Q9 to turn it "ON." The load capacitance is then rapidly discharged toward V−. Diodes D6 and D7 prevent avalanching Q7's and Q8's base-emitter junction as the collectors of Q5 and Q6 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V−.

When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on CIN. Transistors Q2 and Q3 turn-on, pulling stored base charge out of Q4 and Q9 assuring their rapid turn-off. With Q1, Q5, Q6 and Q9 "OFF," Darlington connected Q7 and Q8 turn-on and rapidly charge the load to within a VBE of V−.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

\[ t_r = \left[ \frac{C_L}{250 \times 10^{-12}} \right] \Delta V \]  

For \( C_L = 1000 \text{ pF}, V^+ = 5.0\text{V}, V^- = -12\text{V}, t_r = 21\text{ ns}. \]

Figure 18 shows DS0026 rise times vs \( C_L \).

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

\[ t_f = (2.2)(R5) \left( \frac{C_S + C_L}{h\text{FE}^2} \right) \]  

\[ = (4.4 \times 10^3) \left( \frac{C_S + C_L}{h\text{FE}^2} \right) \]  

where:

\[ C_S = \text{Capacitance to ground seen at the base of Q3} = 2\text{ pF} \]

\[ h\text{FE}^2 = (h_{\text{FEQ3}} + 1)(h_{\text{FEQ4}} + 1) \]

\[ = 500 \]

For the values given and \( C_L = 1000 \text{ pF}, t_f = 17.5\text{ ns}. \)

Figure 19, gives \( t_f \) for various values of \( C_L \).

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in Figure 20. There is breakpoint at \( V_{IN} = 0.6\text{V} \) which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600\text{\mu}A (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150\text{\mu}A (R1 || R2 || R3 || R4).

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width = output pulse width. Selection of \( C_{IN} \) boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

\[ t_1 = R0C_{IN} \ln \frac{I_{\text{MAX}}}{I_{\text{MIN}}} \]  

or

\[ C_{IN} = \frac{t_1}{R0 \ln \frac{I_{\text{MAX}}}{I_{\text{MIN}}}} \]
In this case $R_0$ equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). $I_{\text{MIN}}$ from Figure 21 is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns, 

$$C_{\text{IN}} = \frac{500 \times 10^{-9}}{(150Ω + 150Ω) \ln \frac{20 \text{ mA}}{1 \text{ mA}}} = 560 \text{ pF}$$

In actual practice it’s a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for $C_{\text{IN}}$ vs desired output pulse width is shown in Figure 22.

![Figure 21. Logical "1" Output Voltage vs Source Current](image1)

![Figure 22. Suggested Input Capacitance vs Output Pulse Width](image2)

DC Coupled Applications

The DS0026 may be applied in direct coupled applications. Figure 23 shows the device driving address or pre-charge lines on an MM1103 RAM.

![Figure 23. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)](image3)

For applications requiring a dc level shift, the circuits of Figure 24 or 25 are recommended.

![Figure 24. Transistor Coupled MOS Clock Driver](image4)
APPENDIX III

MOS Interface Circuits

MOS Clock Drivers
MH0007 Direct coupled, single phase, TTL compatible clock driver.
MH0008 Two phase, direct or ac coupled clock driver.
MH0012 10 MHz, single phase direct coupled clock driver.
MH0013 Two phase, ac coupled clock driver.
DS0025C Low cost, two phase clock driver.
DS0026C Low cost, two phase, high speed clock driver.
DS3674 Quad MOS clock driver.
DS75361 Dual TTL-to-MOS driver.
DS75365 Quad TTL-to-MOS driver.

MOS RAM Memory Address and Precharge Drivers
DS0025C Dual address and precharge driver.
DS0026C Dual high speed address and precharge driver.

TTL to MOS Interface
DH0034 Dual high speed TTL to negative level converter.

FIGURE 25. DC Coupled MOS Clock Driver

DS8800 Dual TTL to negative level converter.
DS88L12 Active pull-up TTL to positive high level MOS converter gates.
DS3647A Quad TRI-STATE™ MOS driver I/O register.
DS3648/DS3678 TRI-STATE MOS driver multiplexer.
DS3649/DS3679 Hex TRI-STATE MOS driver.
DS36149/ DS36179 Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps
DS8800 Dual TTL to negative level converter.
DS88L12 Active pull-up TTL to positive high level MOS converter gates.
DS3647A Quad TRI-STATE™ MOS driver I/O register.

Voltage Regulators for MOS Systems
Series
LM320 Series Negative regulators.
LM325 Series Dual ± regulators.
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