

8-Channel, Micropower Sampling 12-Bit Serial I/O A/D Converter

August 1996

FEATURES

- **12-Bit Resolution**
- **Auto Shutdown to 1nA**
- Low Supply Current: 320 μ A Typ
- **Guaranteed $\pm 3/4$ LSB Max DNL**
- Single Supply 5V Operation
- 8-Channel Multiplexer
- Separate MUX Output and ADC Input Pins
- MUX and ADC May Be Controlled Separately
- Sampling Rate: 16.8ksps
- I/O Compatible with SPI, MICROWIRE™, etc.
- 24-Pin SSOP Package

APPLICATIONS

- Pen Screen Digitizing
- Battery-Operated Systems
- Remote Data Acquisition
- Isolated Data Acquisition
- Battery Monitoring
- Temperature Measurement

DESCRIPTION

The LTC®1598 is an 8-channel, 5V micropower, 12-bit sampling A/D converter. It typically draws only 320 μ A of supply current when converting and automatically powers down to typically 1nA between conversions. The LTC1598 is available in a 24-pin SSOP package and operates on a 5V supply. The 12-bit, switched-capacitor, successive approximation ADC includes an 8-channel MUX and a sample-and-hold.

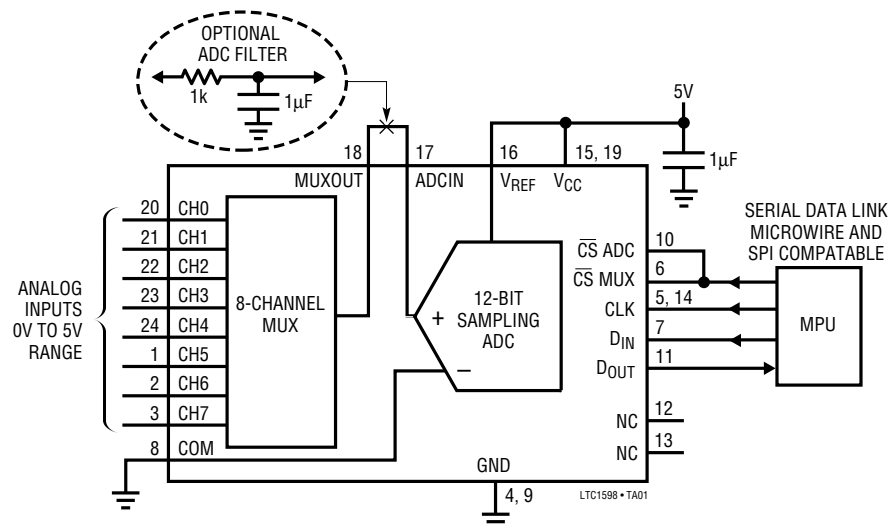
On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three or four wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

The circuit can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

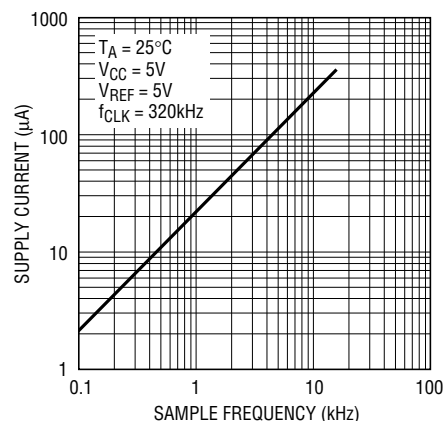
LT, LTC and LT are registered trademarks of Linear Technology Corporation.
MICROWIRE is a trademark of National Semiconductor Corporation.

TYPICAL APPLICATION

24 μ W, 8-Channel, 12-Bit ADC Samples at 200Hz and Runs Off a 5V Supply



Supply Current vs Sample Rate



1598 TA02

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND 12V
VoltageAnalog Reference $-0.3V$ to $(V_{CC} + 0.3V)$ Analog Inputs $-0.3V$ to $(V_{CC} + 0.3V)$ Digital Inputs $-0.3V$ to 12VDigital Output $-0.3V$ to $(V_{CC} + 0.3V)$

Power Dissipation 500mW

Operating Temperature Range

LTC1598CG $0^{\circ}C$ to $70^{\circ}C$ LTC1598IG $-40^{\circ}C$ to $85^{\circ}C$ Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$ Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
CH5 [1]	24 CH4	LTC1598CG LTC1598IG
CH6 [2]	23 CH3	
CH7 [3]	22 CH2	
GND [4]	21 CH1	
CLK [5]	20 CH0	
\overline{CS} MUX [6]	19 V_{CC}	
D_{IN} [7]	18 MUX OUT	
COM [8]	17 ADC IN	
GND [9]	16 V_{REF}	
\overline{CS} ADC [10]	15 V_{CC}	
D_{OUT} [11]	14 CLK	
NC [12]	13 NC	
G PACKAGE 24-LEAD PLASTIC SSOP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 110^{\circ}C/W$		

Consult factory for Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)		4.5		5.5	V
f_{CLK}	Clock Frequency	$V_{CC} = 5V$	(Note 4)		320	kHz
t_{CYC}	Total Cycle Time	$f_{CLK} = 320kHz$	60			μs
t_{hDI}	Hold Time, D_{IN} After $CLK\uparrow$	$V_{CC} = 5V$	150			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}\downarrow$ Before First $CLK\uparrow$ (See Operating Sequence)	$V_{CC} = 5V$	1			μs
t_{suDI}	Setup Time, D_{IN} Stable Before $CLK\uparrow$	$V_{CC} = 5V$	400			ns
t_{WHCLK}	CLK High Time	$V_{CC} = 5V$	1			μs
t_{WLCLK}	CLK Low Time	$V_{CC} = 5V$	1			μs
$t_{WH\overline{CS}}$	\overline{CS} High Time Between Data Transfer Cycles	$f_{CLK} = 320kHz$	16			μs
$t_{WL\overline{CS}}$	\overline{CS} Low Time During Data Transfer	$f_{CLK} = 320kHz$	44			μs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1598CG			LTC1598IG			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 6)	●			± 3			± 3	LSB
Differential Linearity Error		●			$\pm 3/4$			± 1	LSB
Offset Error		●			± 3			± 3	LSB
Gain Error		●			± 8			± 8	LSB
REF Input Range	(Notes 7, 8)				$1.5V$ to $V_{CC} + 0.05V$				V
Analog Input Range	(Notes 7, 8)				$-0.05V$ to $V_{CC} + 0.05V$				V
MUX Channel Input Leakage Current	Channel On or Off (Note 9)	●			± 200			± 200	nA
MUX OUT Leakage Current	All Channels Off	●			± 200			± 200	nA
ADC IN Input Leakage Current		●			± 1			± 1	μA

DYNAMIC ACCURACY (Note 5) $f_{\text{SMPL}} = 16.8\text{kHz}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		71		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		-78		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		80		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		-80		dB

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{\text{CC}} = 5.25\text{V}$	●	2.6		V
V_{IL}	Low Level Input Voltage	$V_{\text{CC}} = 4.75\text{V}$	●		0.8	V
I_{IH}	High Level Input Current	$V_{\text{IN}} = V_{\text{CC}}$	●		2.5	μA
I_{IL}	Low Level Input Current	$V_{\text{IN}} = 0\text{V}$	●		-2.5	μA
V_{OH}	High Level Output Voltage	$V_{\text{CC}} = 4.75\text{V}$, $I_{\text{O}} = 10\mu\text{A}$ $V_{\text{CC}} = 4.75\text{V}$, $I_{\text{O}} = 360\mu\text{A}$	● ●	4.0 2.4	4.64 4.62	V V
V_{OL}	Low Level Output Voltage	$V_{\text{CC}} = 4.75\text{V}$, $I_{\text{O}} = 1.6\text{mA}$	●		0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{\text{CS}} = \text{High}$	●		± 3	μA
I_{SOURCE}	Output Source Current	$V_{\text{OUT}} = 0\text{V}$		-25		mA
I_{SINK}	Output Sink Current	$V_{\text{OUT}} = V_{\text{CC}}$		45		mA
R_{REF}	Reference Input Resistance	$\overline{\text{CS}} = V_{\text{IH}}$ $\overline{\text{CS}} = V_{\text{IL}}$		5000 55		M Ω k Ω
I_{REF}	Reference Current	$\overline{\text{CS}} = V_{\text{CC}}$ $t_{\text{CYC}} \geq 760\mu\text{s}$, $f_{\text{CLK}} \leq 25\text{kHz}$ $t_{\text{CYC}} \geq 60\mu\text{s}$, $f_{\text{CLK}} \leq 320\text{kHz}$	● ●	0.001 90 90	2.5 140	μA μA μA
I_{CC}	Supply Current	$\overline{\text{CS}} = V_{\text{CC}}$, $\text{CLK} = V_{\text{CC}}$, $D_{\text{IN}} = V_{\text{CC}}$ $t_{\text{CYC}} \geq 760\mu\text{s}$, $f_{\text{CLK}} \leq 25\text{kHz}$ $t_{\text{CYC}} \geq 60\mu\text{s}$, $f_{\text{CLK}} \leq 320\text{kHz}$	● ●	0.001 320 320	± 5 640	μA μA μA

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence 1		1.5		CLK Cycles
$f_{\text{SMPL(MAX)}}$	Maximum Sampling Frequency	See Operating Sequence 1	●	16.8		kHz
t_{CONV}	Conversion Time	See Operating Sequence 1		12		CLK Cycles
t_{dDO}	Delay Time, $\text{CLK}\downarrow$ to D_{OUT} Data Valid	See Test Circuits	●	250	600	ns
t_{dis}	Delay Time, $\overline{\text{CS}}\uparrow$ to D_{OUT} Hi-Z	See Test Circuits	●	135	300	ns
t_{en}	Delay Time, $\text{CLK}\downarrow$ to D_{OUT} Enabled	See Test Circuits	●	75	200	ns
t_{hDO}	Time Output Data Remains Valid After $\text{CLK}\downarrow$	$C_{\text{LOAD}} = 100\text{pF}$		230		ns
t_{f}	D_{OUT} Fall Time	See Test Circuits	●	50	150	ns
t_{r}	D_{OUT} Rise Time	See Test Circuits	●	50	150	ns
t_{ON}	Enable Turn-On Time	See Operating Sequence 1	●	260	700	ns
t_{OFF}	Enable Turn-Off Time	See Operating Sequence 2	●	100	300	ns
t_{OPEN}	Break-Before-Make Interval		●	35	160	ns
C_{IN}	Input Capacitance	Analog Inputs On-Channel Off-Channel Digital Input		20 5 5		pF pF pF

AC CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: This device is specified at 5V. Consult factory for 3V specified devices.

Note 4: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} = 200\text{kHz}$ at 85°C , $f_{CLK} \geq 120\text{kHz}$ at 70°C and $f_{CLK} \geq 1\text{kHz}$ at 25°C .

Note 5: $V_{CC} = 5\text{V}$, $V_{REF} = 5\text{V}$ and $CLK = 320\text{kHz}$ unless otherwise specified.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC} . This spec allows 50mV forward bias of either diode for $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range, it will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Recommended operating condition.

Note 9: Channel leakage current is measured after the channel selection.

PIN FUNCTIONS

CH5 (Pin 1): Analog Multiplexer Input.

CH6 (Pin 2): Analog Multiplexer Input.

CH7 (Pin 3): Analog Multiplexer Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CLK (Pin 5): Shift Clock. This clock synchronizes the serial data transfer to both MUX and ADC. It also determines the conversion speed of the ADC.

$\overline{\text{CS MUX}}$ (Pin 6): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUX OUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{\text{CS ADC}}$.

D_{IN} (Pin 7): Digital Data Input. The multiplexer address is shifted into this input.

COM (Pin 8): Negative Analog Input. This input is the negative analog input to the ADC and must be free of noise with respect to GND.

GND (Pin 9): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{\text{CS ADC}}$ (Pin 10): ADC Chip Select Input. A logic high on this input deselects and powers down the ADC and three-states D_{OUT} . A logic low on this input enables the ADC to sample the selected channel and start the conversion. For normal operation drive this pin in parallel with $\overline{\text{CS MUX}}$.

D_{OUT} (Pin 11): Digital Data Output. The A/D conversion result is shifted out of this output.

NC (Pin 12): No Connection.

NC (Pin 13): No Connection.

CLK (Pin 14): Shift Clock. This input should be tied to Pin 5.

V_{CC} (Pin 15): Power Supply Voltage. This pin provides power to the A/D Converter. It must be bypassed directly to the analog ground plane.

V_{REF} (Pin 16): Reference Input. The reference input defines the span of the ADC.

ADC IN (Pin 17): ADC Input. This input is the positive analog input to the ADC. Connect this pin to MUX OUT for normal operation.

MUX OUT (Pin 18): MUX Output. This pin is the output of the multiplexer. Tie to ADC IN for normal operation.

V_{CC} (Pin 19): Power Supply Voltage. This pin should be tied to Pin 15.

CH0 (Pin 20): Analog Multiplexer Input.

CH1 (Pin 21): Analog Multiplexer Input.

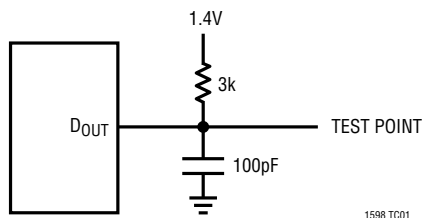
CH2 (Pin 22): Analog Multiplexer Input.

CH3 (Pin 23): Analog Multiplexer Input.

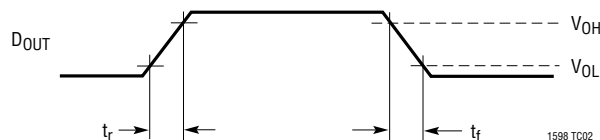
CH4 (Pin 24): Analog Multiplexer Input.

TEST CIRCUITS

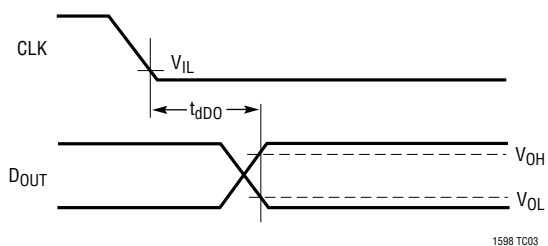
Load Circuit for t_{dDO} , t_r and t_f



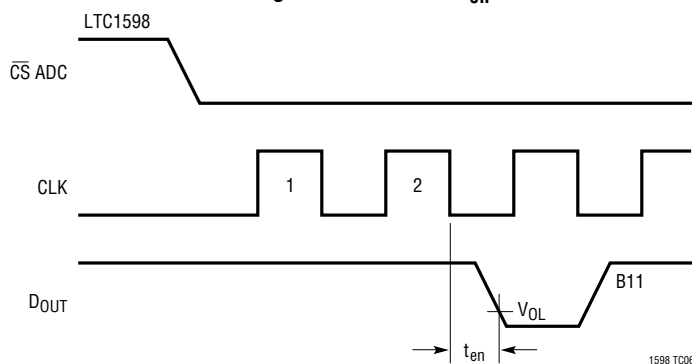
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r , t_f



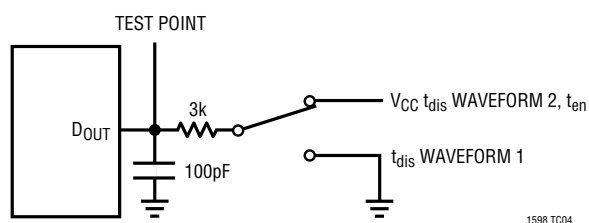
Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



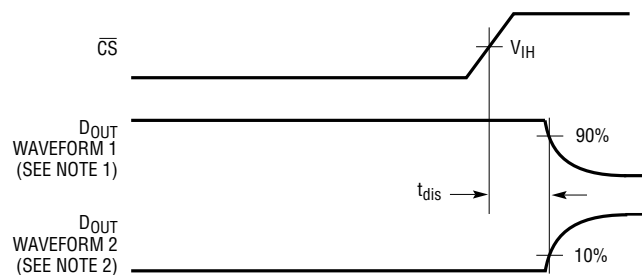
Voltage Waveforms for t_{en}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

APPLICATIONS INFORMATION

INPUT DATA WORD

The LTC1598 uses its Chip Select and D_{IN} pins to select one of its eight channels as shown in the operating sequence figures and Table 1. For this discussion we will assume that \overline{CS} MUX and \overline{CS} ADC are tied together and will refer to them as simply, \overline{CS} .

When \overline{CS} is high, the input data on the D_{IN} pin is latched into the 4-bit shift register on the rising edge of the clock. The input data word consists of an “EN” bit and a string of three bits for channel selection. If the “EN” bit is logic high as illustrated in Operating Sequence 1, it enables the selected channel. To ensure correct operation, the \overline{CS} must be pulled low before the next rising edge of the clock. More than four input bits can be sent to the ADC without problems. The channel will be determined by the last four bits clocked in before \overline{CS} falls.

Once the \overline{CS} is pulled low, all channels are simultaneously switched off to ensure a break-before-make interval. After a delay of t_{ON} , the selected channel is switched on, allowing signal transmission. The selected channel remains on, until the next falling edge of \overline{CS} . After a delay of t_{OFF} , it terminates the analog signal transmission and switches to the next selected channel. If the “EN” bit is logic low, as illustrated in Operating Sequence 2, it disables all channels. Table 1 shows the various bit combinations for channel selection.

Table 1. Logic Table for Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1
CH4	1	1	0	0
CH5	1	1	0	1
CH6	1	1	1	0
CH7	1	1	1	1

ANALOG CONSIDERATIONS

Grounding

The LTC1598 should be used with an analog ground plane and single-point grounding techniques. To achieve the optimum performance use a printed circuit board. The Ground pins (Pins 4 and 9) should be tied directly to the ground plane with minimum lead length.

Bypassing

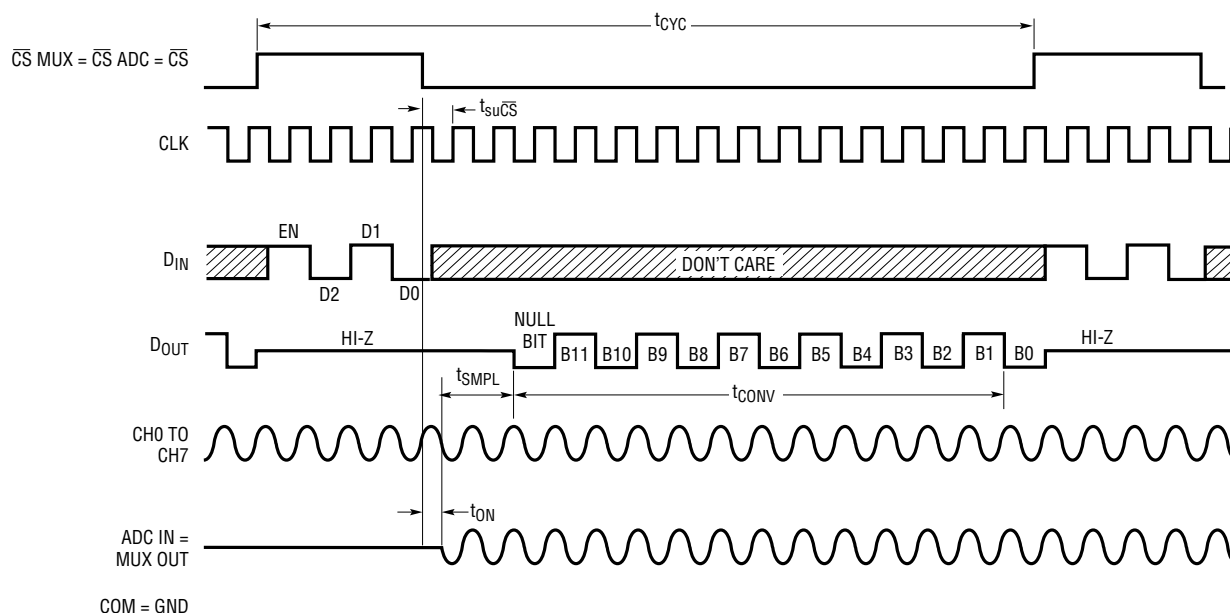
For good performance, the LTC1598 V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC} and V_{REF} voltages with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with minimum of 0.1 μ F capacitors and lead lengths as short as possible.

Analog Inputs

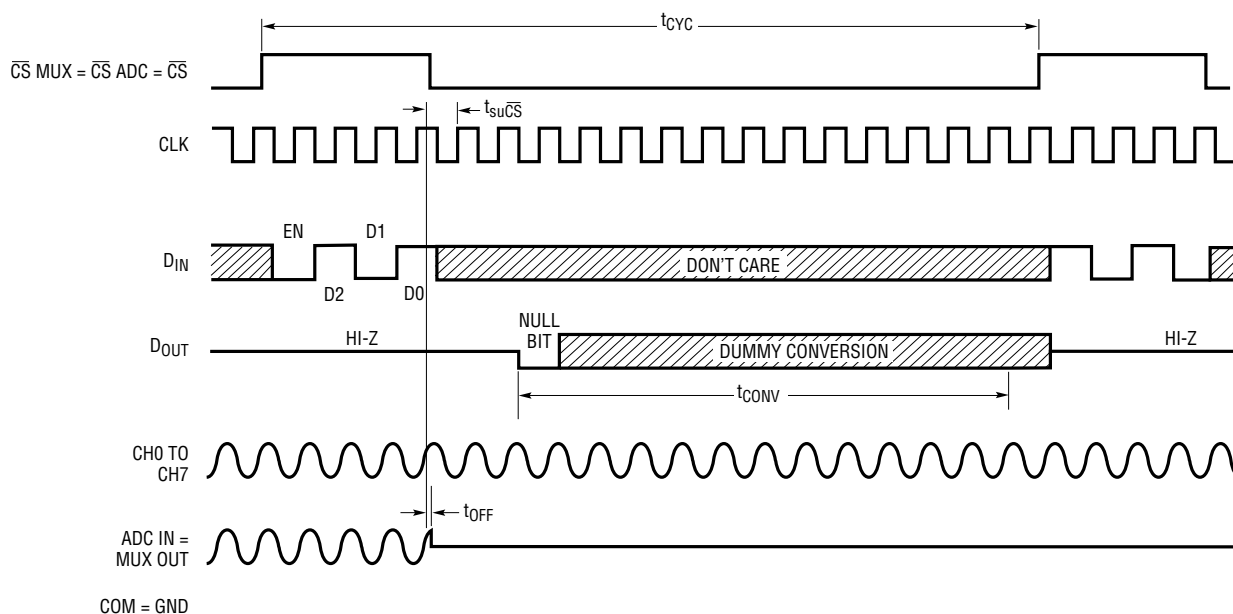
Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1598 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

APPLICATIONS INFORMATION

Operating Sequence 1
Example: (CH2, GND)



Operating Sequence 2
Example: (ALL Channels Off)



TYPICAL APPLICATIONS

Microprocessor Interfaces

The LTC1598 can interface directly (without external hardware) to most popular microprocessors' (MPU) synchronous serial formats including MICROWIRE™, SPI and QSPI. If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1598. Included here is one serial interface example.

MICROWIRE is a trademark of National Semiconductor Corp.

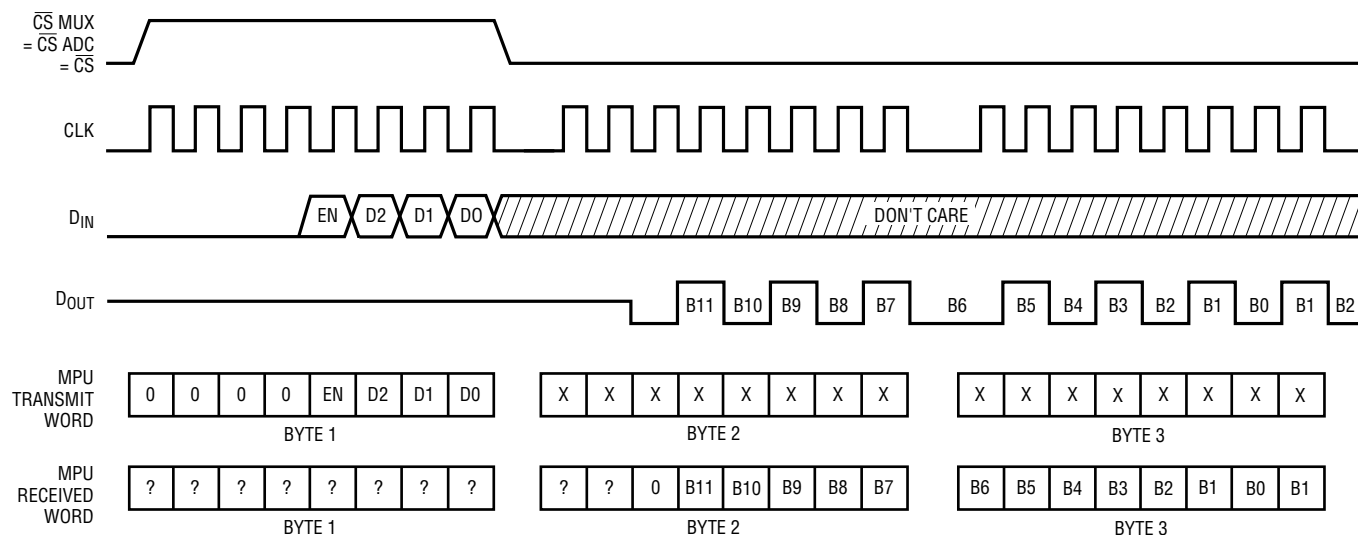
Motorola SPI (MC68HC05)

The MC68HC05 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B7 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits B6 through B0 into the MPU. ANDing the second byte with 1F_{HEX} clears the three most significant bits and ANDing the third byte with FE_{HEX} clears the least significant bit. Shifting the data to the right by one bit results in a right justified word.

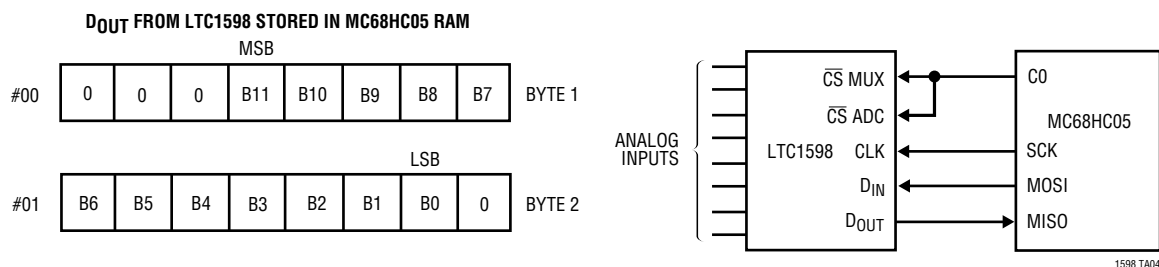
MC68HC05 CODE		
LDA	#\$52	Configuration data for serial peripheral control register (Interrupts disabled, output enabled, master, Norm = 0, Ph = 0, Clk/16)
STA	\$0A	Load configuration data into location \$0A (SPCR)
LDA	#\$FF	Configuration data for I/O ports (all bits are set as outputs)
STA	\$04	Load configuration data into Port A DDR (\$04)
STA	\$05	Load configuration data into Port B DDR (\$05)
STA	\$06	Load configuration data into Port C DDR (\$06)
LDA	#\$08	Put D _{IN} word for LTC1598 into Accumulator (CH0 with respect to GND)
STA	\$50	Load D _{IN} word into memory location \$50
START	BSET 0,\$02	Bit 0 Port C (\$02) goes high (\overline{CS} goes high)
	LDA \$50	Load D _{IN} word at \$50 into Accumulator
	STA \$0C	Load D _{IN} word into SPI data register (\$0C) and start clocking data
LOOP1	TST \$0B	Test status of SPIF bit in SPI status register (\$0B)
	BPL LOOP1	Loop if not done with transfer to previous instruction
	BCLR 0,\$02	Bit 0 Port C (\$02) goes low (\overline{CS} goes low)
	LDA \$0C	Load contents of SPI data register into Accumulator
	STA \$0C	Start next SPI cycle
LOOP2	TST \$0B	Test status of SPIF
	BPL LOOP2	Loop if not done
	LDA \$0C	Load contents of SPI data register into Accumulator
	STA \$0C	Start next SPI cycle
	AND #\$1F	Clear 3 MSBs of first D _{OUT} word
	STA \$00	Load Port A (\$00) with MSBs
LOOP3	TST \$0B	Test status of SPIF
	BPL LOOP3	Loop if not done
	LDA \$0C	Load contents of SPI data register into Accumulator
	AND #\$FE	Clear LSB of second D _{OUT} word
	STA \$01	Load Port B (\$01) with LSBs
	JMP START	Go back to start and repeat program

TYPICAL APPLICATIONS

Data Exchange Between LTC1598 and MC68HC05



Hardware and Software Interface to Motorola MC68HC05



This circuit demonstrates how the LTC1598's independent analog multiplexer can simplify design of a 12-bit data acquisition system. All eight channels are MUXed into a single 1kHz, fourth-order Sallen-Key antialiasing filter, which is designed for single-supply operation. Since the LTC1598's data converter accepts inputs from ground to the positive supply, rail-to-rail op amps were chosen for the filter to maximize dynamic range. The LT1368 dual rail-to-rail op amp is designed to operate with 0.1μF load capacitors (C1 and C2). These capacitors provide frequency compensation for the amplifiers and help reduce the amplifier's output impedance and improve supply rejection at high frequencies. The filter contributes less than 1LSB of error due to offsets and bias currents. The

The combined MUX and A/D errors result in an integral nonlinearity error of $\pm 3\text{LSB}$ (maximum) and a differential nonlinearity error of $\pm 3/4\text{LSB}$ (maximum). The typical signal-to-noise plus distortion ratio is 71dB, with approximately -78dB of total harmonic distortion. The LTC1598 is programmed through a 4-wire serial interface that is compatible with MICROWIRE, SPI and QSPI. Maximum serial clock speed is 320kHz, which corresponds to a 16.8kHz sampling rate.

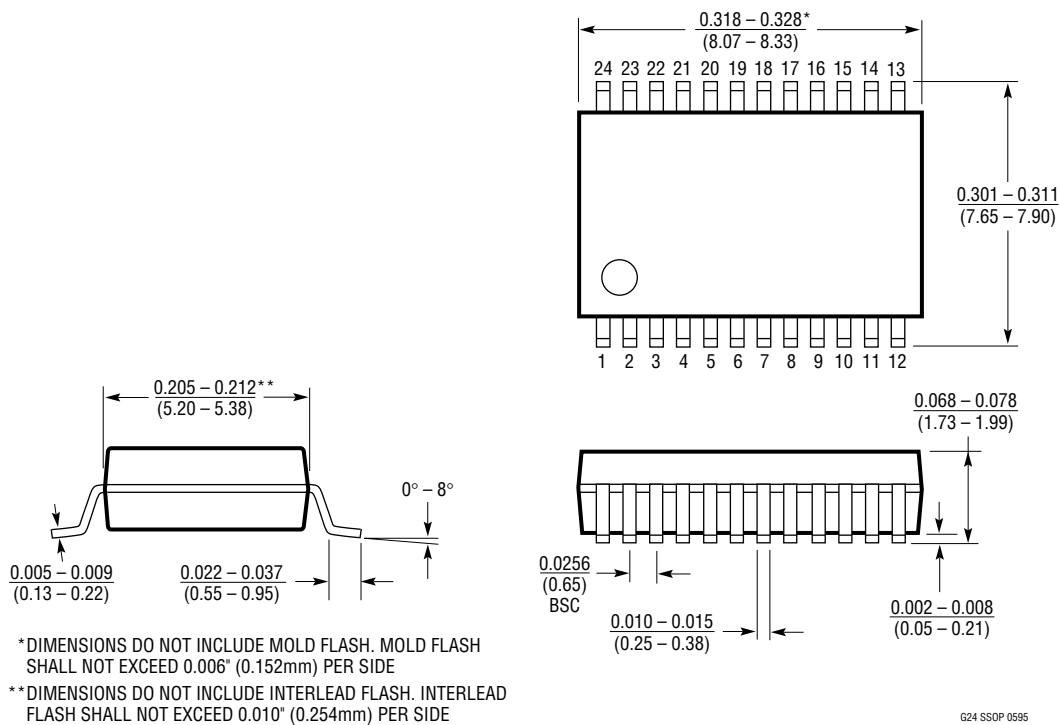
The complete circuit consumes approximately 800 μ A from a single 5V supply.

The schematic diagram illustrates the LTC1598 evaluation board. The LTC1598 chip is connected to an analog input multiplexer (MUX) and a digital interface. The MUX selects between 8 analog inputs (CH0-CH7) and routes them to the ADC's input. The ADC's output is connected to a digital interface (DATA IN, DATA OUT, CHIP SELECT, CLOCK). The circuit also includes a 5V supply, decoupling capacitors (C1, C2), and a feedback network for the ADC's internal op-amp.

PACKAGE DESCRIPTION

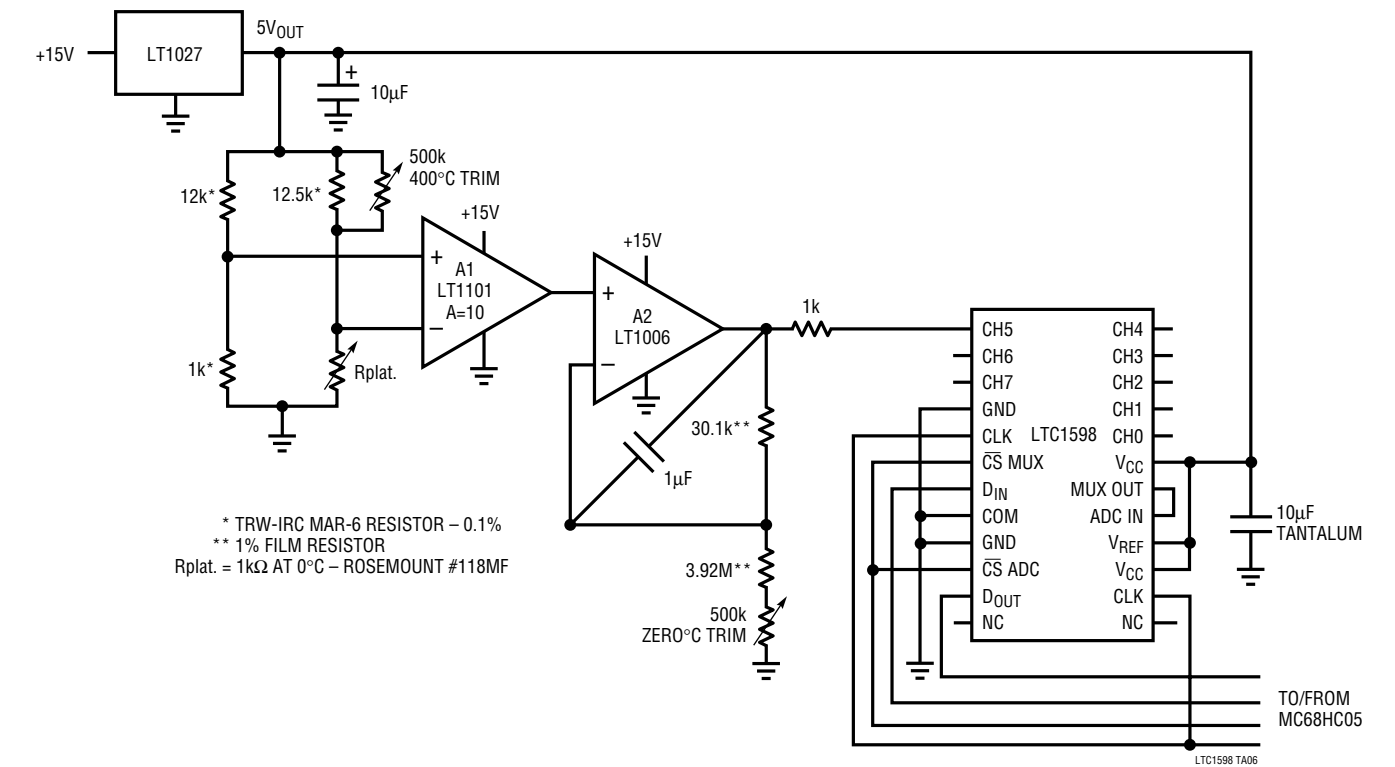
Dimensions in inches (millimeters) unless otherwise noted.

G Package 24-Lead Plastic SSOP (0.209) (LTC DWG # 05-08-1640)



TYPICAL APPLICATION

Digitally Linearized Platinum RTD Signal Conditioner



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1096/LTC1098	8-Pin SO, Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1096L/LTC1098L	8-Pin SO, 2.65V Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1196/LTC1198	8-Pin SO, 1Msps 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1282	3V High Speed Parallel 12-Bit ADC	140ksps, Complete with V _{REF} , CLK, Sample-and-Hold
LTC1285/LTC1288	8-Pin SO, 3V, Micropower	1- or 2-Channel, Auto Shutdown
LTC1289	Multiplexed 3V, 1A, 12-Bit ADC	8-Channel 12-Bit Serial I/O
LTC1594	4-Channel, 5V Micropower 12-Bit ADC	Low Power, Small Size, Low Cost
LTC1594L	4-Channel, 3V Micropower 12-Bit ADC	Low Power, Small Size, Low Cost