At Linear Technology Corporation (LTC) our overriding commitment is to achieve excellence in Quality, Reliability and Service (QRS) and total customer satisfaction. We interpret the word "excellence" to mean delivering products that consistently exceed all the requirements and expectations of our customers. The commitment to QRS extends from the president to every employee, from design to product qualification, and from manufacturing to shipping. To meet this commitment, LTC has established a comprehensive program called "Quality for the Nineties."

This program is divided into four separate, but highly interrelated programs; Quality Environment, Total Quality Management System (TQMS), Vendor Participation, and Focus for the Nineties.

**Quality Environment**

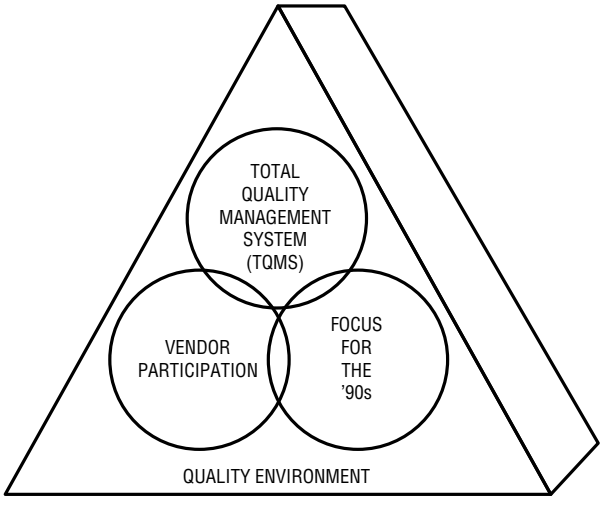
The first program, Quality Environment, serves as the building block for three other programs. It entails establishing an environment that is conducive to the participation of each and every employee in helping to build quality into our products. This program encourages every employee to identify any quality problem and participate in recommending solutions.

A comprehensive operator training and certification program has been established that covers every area of manufacturing from incoming raw material inspection, wafer fabrication, assembly, and test to shipping. Emphasis is placed on compliance with specifications, statistical process control (SPC) performance to quality goals, electrostatic discharge damage (ESD) awareness and controls, encouraging operators to think quality and recommend quality improvement ideas.

To ensure compliance with specifications, a Quality Audit Team performs a systems audit of key manufacturing areas and suppliers at periodic intervals. Compliance with process specifications and the detailed programs of the Corporate ISO9001 Quality Policy are verified, and discrepancies reported for quick resolution with special emphasis to eliminate recurring problems. The performance of each area is then rated, providing a strong incentive for each area to excel.

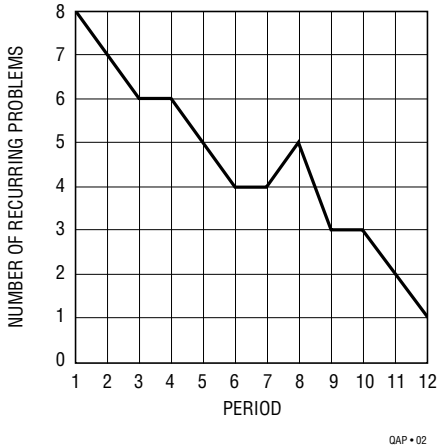
With the philosophy that each department, starting from incoming raw materials, is considered a customer of the preceding department, every effort is made by working closely together to meet or exceed our end-customer requirements and goals.

**Quality for the '90s**




QAP • 01

**Systems Quality Audit-Tracking Recurring Problems**




QAP • 02

### Total Quality Management System (TQMS)

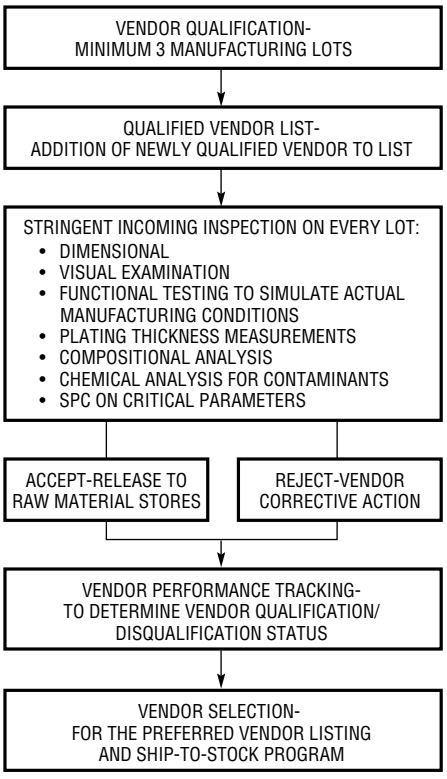
The second program starts with the incorporation of innovative but conservative design and layout rules to achieve the best performance without sacrificing quality and reliability. During the design and development cycle, design, product, package, manufacturing, quality and reliability engineering groups participate in design reviews to ensure that all program aspects are covered, ranging from product performance objectives to ensuring reproducibility and repeatability in wafer fabrication and assembly. Special emphasis is placed on devising input protection circuitry to minimize susceptibility to voltage spikes and ESD, optimizing thermal layout to minimize parametric drift, and optimizing bond pad layout to maximize assembly and electrical test yields, at the same time allowing the die to be assembled in a wide selection of packages.

Once the design is approved, a stringent manufacturing qualification test plan is conducted on the initial engineering runs. The test plan is selected to bring out any weaknesses in the design and any manufacturability problems, and includes reliability stress tests such as high temperature Operational Life and HAST (Highly Accelerated Stress Testing) for plastic packages, and MIL-STD-883 method 5005 qualification testing for hermetic packages. Product performance on these tests must be equal to or better than similar products within the same generic group to be considered qualified. Major design, package, material and process changes are also subjected to these same stringent qualification requirements. In addition to achieving the required reliability performance, an engineering change must also achieve manufacturing yield and quality performance levels equal to or better than the original product to be considered qualified. A major change control procedure is in place to notify customers of major changes for approval prior to implementation when required.

In manufacturing, process controls start with vendor qualification on raw material piece parts. A Qualified Vendor List is maintained and performance of each vendor is continuously monitored on a Vendor Rating Program. A dimensional, visual, functional and, where applicable, compositional analysis is performed on each direct raw material lot. Automated state-of-the-art wafer fabrication, assembly and test equipment, cassette-to-cassette handling in wafer fabrication and automated handling in assembly are utilized, where possible, to maintain manufacturing consistency and quality. Only fully trained and certified operators are allowed to work on production material.

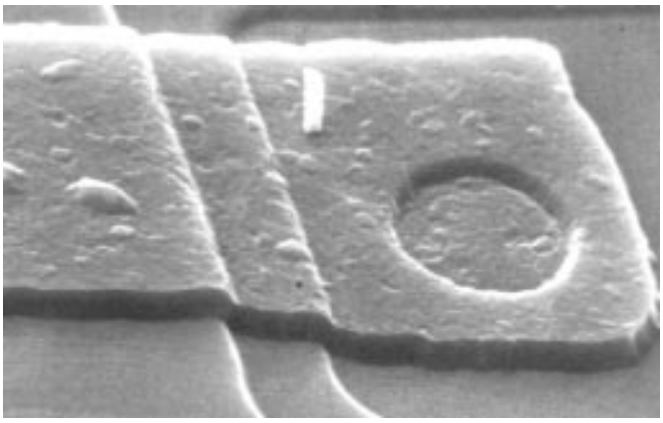
Stringent statistical process controls, typically beyond industry standards, are established for each critical manufacturing step in wafer fabrication, wafer test, assembly,

**Raw Material Controls**




QAP • 03

**SEM Monitor of Metallization Quality**



package finishing, mark and pack and shipping as depicted in the Wafer Fabrication, Assembly,Test and End-of-Line flowcharts.

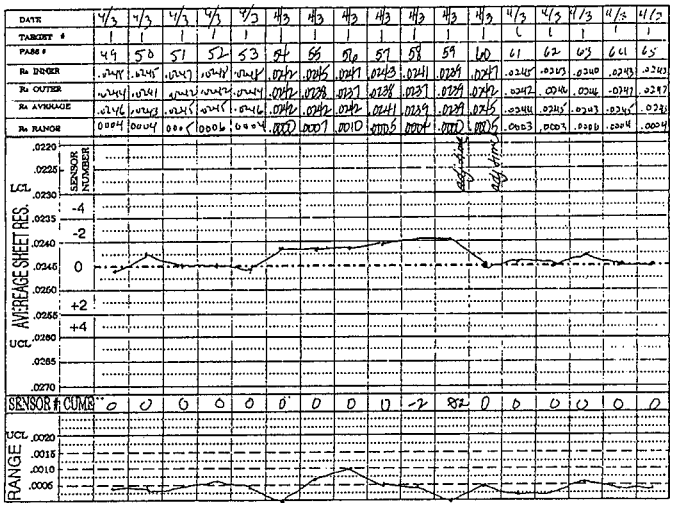
The process controls include monitors of critical assembly processes and lot acceptance inspection for operations requiring 100% production inspection. Preseal visual inspection is performed per MIL-STD-883 Method 2010 Test Condition B. Statistical process control techniques are employed in optimizing process parameters, and monitoring process performance through the use of control charts with action limits and upper and lower control limits, and in parametric distribution analysis at electrical test.

Electrical quality is guaranteed by conservative guardbanding on production test programs of a minimum of three machine guardbands, by using state-of-the-art test equipment and 0.04% AQL for lot acceptance testing at 25°C for all military and commercial lots. Additional tests, like rack burn-in, beyond the data sheet specifications on regulator products are performed by exercising the parts in a thermal shutdown mode. These tests are incorporated into the test flow to improve reliability and weed out infant mortality failures. Visual and mechanical quality is optimized by minimizing handling of parts in assembly, test and end-of-line operations. Lead finish processes have been selected that minimize solderability problems and all lots are subjected to a stringent major visual/mechanical inspection. Administrative errors due to mixed and wrong parts are minimized by strictly adhering to a one lot per station policy, and double-checking orders at order entry and shipping. Before shipment of a lot to the customer each lot is inspected to ensure that it meets internal and customer specifications and purchase order requirements. The level of attention paid to each unit is demonstrated by the fact that each unit is traceable to the wafer fabrication lot number via a side or back mark on both 883 and commercial products on all packages, except where there is a physical constraint.

Through the use of automated equipment, strict process controls (utilizing proven statistical process control techniques), periodic systems and quality audits (conducted by the Quality Audit Team), stringent facilities and environmental controls and monitors, LTC is able to ensure that quality is built into the product and to guarantee a consistently high quality level.

The manufacturing quality controls are complimented by a reliability audit program designed to weed out design, fabrication, packaging and assembly deficiencies. Additionally, controls are supported by a comprehensive failure analysis and corrective action program designed to provide timely feedback of findings to all operating groups for resolution. The analysis of customer returns, and corrective action taken, completes the closed loop of our Total Quality Management System.

**Actual $\bar{X}$ and R Chart of Aluminum Sputter Deposition Using Sensor Number Control**

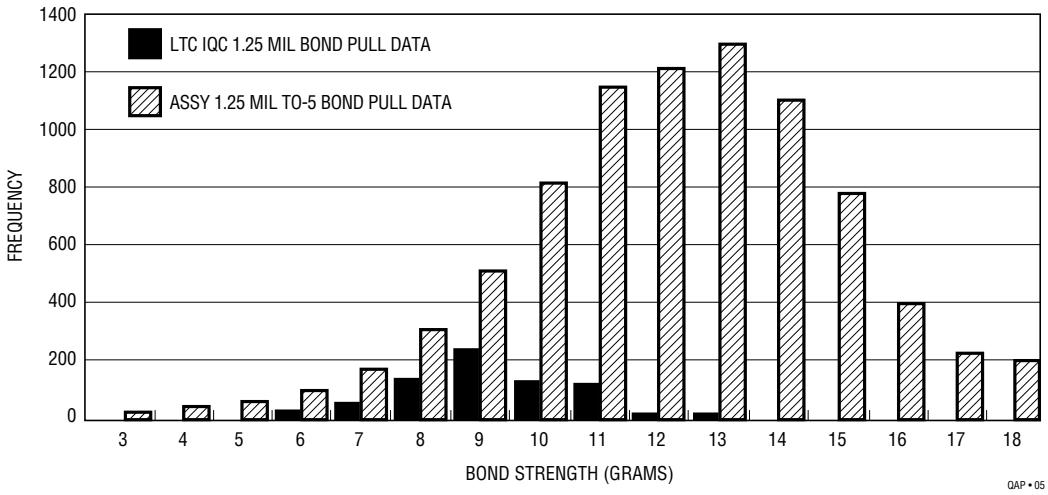



QAP • 04

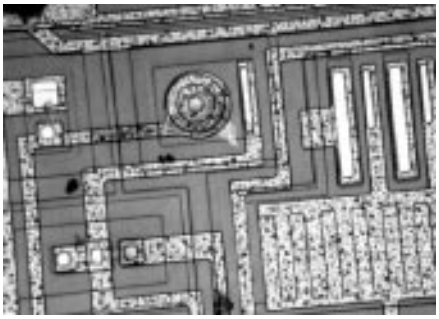
**Military and Commerical Products Share the Same Stringent Inspections and Controls**

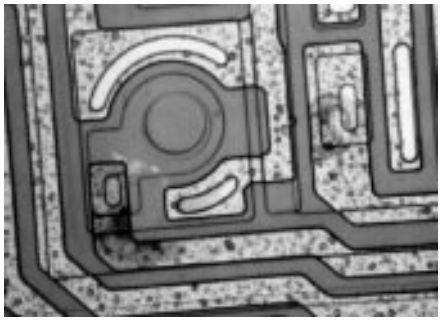
- WAFER FABRICATION PROCESS CONTROLS AND CLASS 100 PROCESSING.
- REGULAR SEM MONITORS.
- PRE-SEAL VISUAL INSPECTION PER MIL-STD-883 METHOD 2010. TEST CONDITION B.
- DIE SHEAR TEST PER MIL-STD-883 METHOD 2019.
- BOND PULL TEST PER MIL-STD-883 METHOD 2011.
- SOLDERABILITY TEST PER MIL-STD-883 METHOD 2003.
- MARK PERMANENCY TEST PER MIL-STD-883 METHOD 2015.
- HERMETICITY TESTING PER MIL-STD-883 METHOD 1014.
- QA ELECTRICAL TEST TO 0.04% AQL AT 25°C, AND TEMPERATURE TESTING.
- EXTERNAL VISUAL PER MIL-STD-883 METHOD 2009.

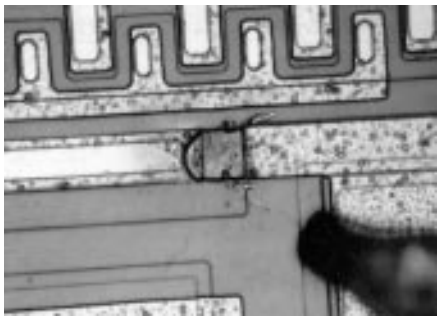
**Bond Strength Histogram**

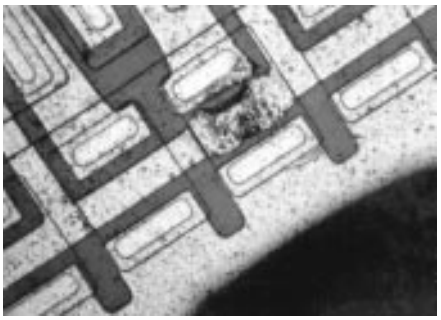



**Failure Analysis Photomicrographs**









### Vendor Participation

The requirements of high quality raw materials for integrated circuit manufacture range from ppb (parts per billion) impurity levels for electronic grade chemicals to ppm (parts per million) defective levels for lead frame packaging materials. It is not only essential, but critical for the semiconductor manufacturer to work closely with its vendors to attain the high quality levels needed in raw materials. At LTC a program has been established and implemented to allow vendor participation in formulating specifications and establishing percentage defective and lot rejection rate goals. This vendor participation ensures that the direct and raw material quality levels received are consistent with our manufacturing and end-product quality goals. Clearly, achieving optimum quality product requires the use of the best possible materials available and with continuous communication and feedback from our vendors to improve in this key area. A Preferred Vendor Program helps to drive vendors to manufacturing excellence.

### Focus for the ’90s

The following key quality improvements programs have been established to meet the quality requirements of the ’90s.

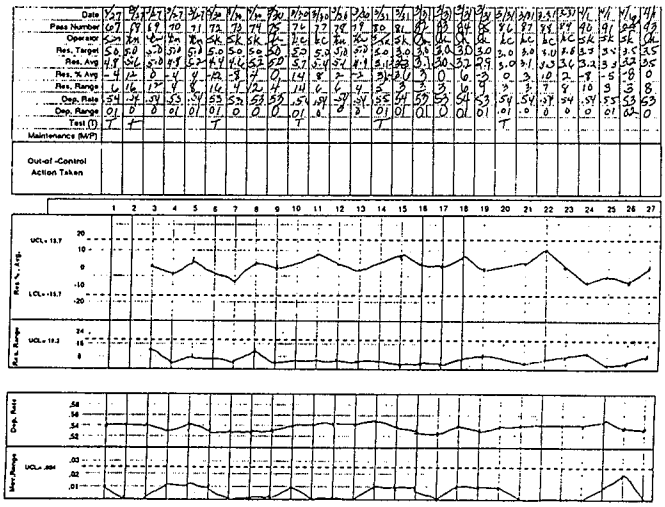
### PPM Goals

As demand for quality semiconductor components becomes increasingly more stringent, the percentage goals from the 1970s have given way to ppm goals in the ’80s and ’90s. At LTC ppm quality goals are established for every major operation, from incoming inspection to customer returns. Performance to goals is reviewed quarterly and, where goals are not met, quality improvement programs are defined and implemented. Quality goals are updated and tightened on an annual basis, and quality programs are redefined to achieve the new goals established. One of the early benefits of this program is demonstrated by the excellent average outgoing electrical quality (AOQ).

### Statistical Process Control (SPC)

The increased reliance on automated manufacturing and test equipment underlines the need for strict process control techniques. SPC is a valuable tool and at LTC we realize the importance of these methods. Engineering analysis is performed regularly using SPC techniques to establish the process capability. Various variable and attribute control charts are used to ensure that processes are within normal limits and action and shutdown limits are established for critical operations. The process capability of key processes are calculated using the Cpk capability index on an ongoing basis to ensure a program for continuous quality improvement.

**Actual Normalized X and Moving R Chart of Epitaxial Growth Reactor Controlling Resistivity and Deposition Rate**

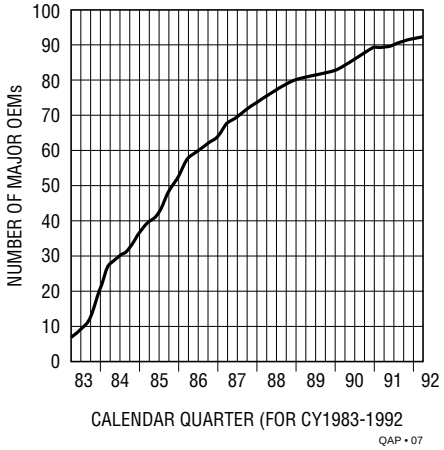



QAP • 06

## ESD Control

A comprehensive ESD control program has been established which encompasses design, handling, testing, storage and final packaging for shipment. The program includes the use of grounded table tops, floor mats, wrist straps and heel straps, topical antistatic treatment of floor coverings, banning of static bearing materials from the manufacturing environment, ionizers, and use of conductive or antistatic materials for handling and final packaging. Areas where ESD control must be enforced are designated as ESD Protected areas. ESD awareness training programs help to increase the operator's awareness for successful implementation of this program. Every effort is made to stamp out this silent chip killer. The benefits of this program are improved quality and reliability to the customer.

**Quality System Surveys MIL-Q-9858 and MIL-I-45208 Approval**

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**Based on the foregoing quality programs, Linear Technology Corporation is positioned to continuously improve its product quality and exceed the demands of its customers in the '90s and beyond.**

## ISO 9001 Certification

Realizing the importance of the ISO 9000 international standard for quality management, LTC received ISO 9001 certification in 1993 covering the company's design, manufacturing and service organizations. This has also helped to solidify customer confidence that they are dealing with a manufacturer with a proven international quality system.


TÜV CERT

CERTIFICATE

DAR

The TÜV-Zertifizierungsgemeinschaft e.V.
hereby certifies that

Linear Technology Corporation

Milpitas, CA

has established and applies
a quality system for

Design and manufacturing of a broad line of high performance linear integrated circuits

An audit was performed, Report No. 5098
Proof has been furnished that the requirements according to
DIN ISO 9001 / EN 29001
are fulfilled.

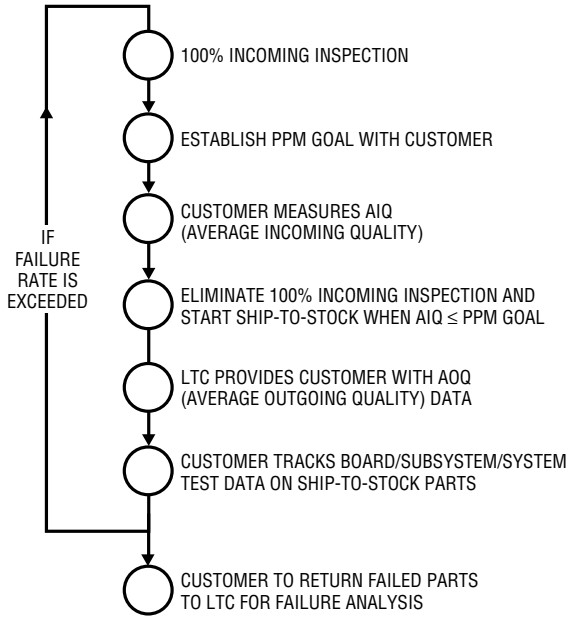
The certificate is valid until
March 31, 1996
Certificate Registration No.
09 100 3098

TÜV Rheinland Gruppe

## Customer Ship-To-Stock Program

LTC is working hand-in-hand with customers to consistently supply high quality products to achieve a ship-to-stock program by eliminating the need to do an incoming inspection. We recognize the benefits to our customers of a ship-to-stock program, namely, savings in the need to purchase and maintain incoming test equipment, savings in the need to maintain a safety stock in case of incoming lot rejections, and reduction in board failures and rework costs because of higher component quality.

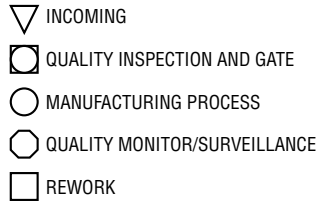
**Ship-To-Stock Program Flow**



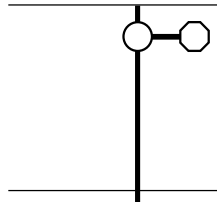
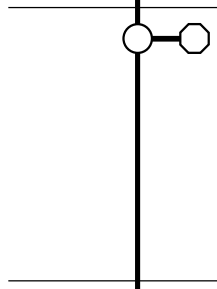
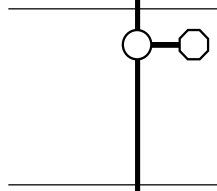
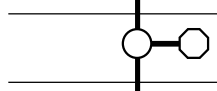
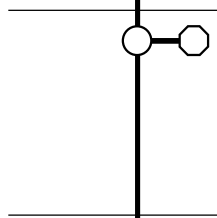
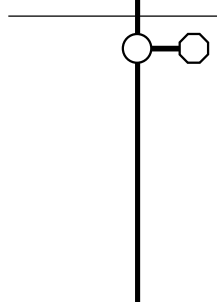
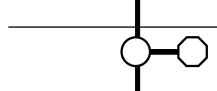
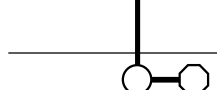
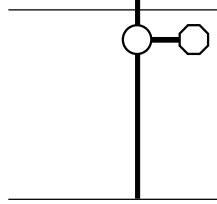

QAP • 08

## WAFER FABRICATION FLOWCHART
### Generic Bipolar Process

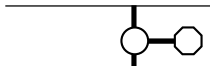
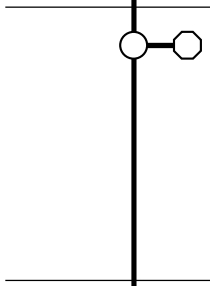
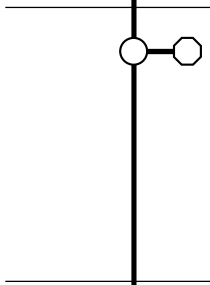
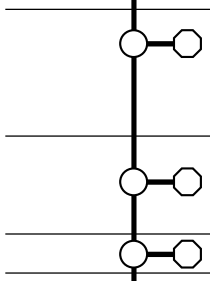
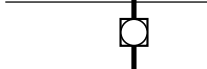
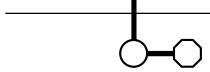
**Vendor:** Linear Technology Corporation
**Package:** Plastic SOIC/DIP
**Location of Wafer Fab:** Linear Technology Corporation, Milpitas, CA
**Assembly:** Carsem Unisem Penang Malaysia, ASAT Hong Kong
**Final Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Q.C. Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Source Accept Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Quality Contact:** QA Manager, LTC, Milpitas, CA
(408) 432-1900




| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
| | Incoming Raw Material Inspection | Wafers | Visual: Scratches, Pits, Haze, Craters, Dimples, Contamination, | 1X Inspection | 1.0% AQL to 2.5% AQL Level 1 | % LAR Trend Chart and % Defective Trend Chart |
| | | | Oxygen/Carbon Measurement | Infrared Spectrometer | S/S = 2, $A_{CC}$ = 0 | $\overline{X}$ and R |
| | | | Resistivity/ Conductivity | Magnetron V/I Meter | S/S = 2, $A_{CC}$ = 0 | $\overline{X}$ and S |
| | | | Dimensional | Calipers | 2.5% AQL, Level S1 | X and Moving R Run Chart |
| | | | Thickness and Taper/Bow | Dial Thickness Gauge | 2.5% AQL, Level S1 | |
| | | | Orientation | Break Test | S/S = 1, $A_{CC}$ = 0 | |
| | | | C of C Verification Against "MPS" Requirements | | Each Batch | |
| | | Photo Mask Plates | Visual C.D. Measurement | AMS-100 Calipers Comparator UV Lamp | Each Plate | Logbook |
| | | Chemicals | C of C Verification Against "MPS" Requirements | | Each Batch | Logbook |
| | | Gases | Plus Yearly Gas Analysis | Outside Lab | | Logbook |
| | | Targets | C of C Verification | | Each Target | Logbook |
| | Initial Oxidation | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
| | Collector Mask | Resist Mask HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | Collector Implant | Implant | | | | Logbook |

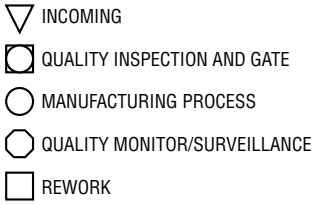
| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | Collector Diffusion | Oxidation and Diffusion Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field | Logbook |
| | | | Oxide Thickness | Nanospec | 2 Wafers/Run | |
| | | | $R_{\square}$ | 4 Point Probe | 1 Test Wafer/Run | |
| | | | XJ | Philtec Groove | 1 Test Wafer/Cycle | |
|  | EPI | Deposit EPI Gemini Reactor | Visual | UV Lamp | 100% for EPI Spike More Than 5 Wafers is Reject | |
| | | | | Interference Contrast Microscope | More Than 1 Slip and Stacking Fault is Reject | |
| | | | $R_{\square}$ | 4 Point Probe | 2 Reading/Pass | X and Moving R |
| | | | EPI Thickness | Nicolet | 2 Reading/Pass | Run Chart |
|  | EPI Re-Ox | Oxidation Furnace | Visual | UV Lamp | 100% | Logbook |
| | | | | 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | |
| | | | Oxide Thickness | Nanospec | 2 Wafers/Run | |
|  | Isolation Mask | Resist Mask HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan. 100% of the Wafers | Production Log |
|  | Isolation Predeposition | Boron Deposition Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | Trend Chart |
| | | | | 20X Microscope | 2 Wafers/Run < 4 Defects/Field of View | |
| | | | $R_{\square}$ | 4 Point Probe | 2 Test Wafers/Run | |
|  | Isolation Diffusion | Diffusion Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | Logbook |
| | | | | 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | |
| | | | $R_{\square}$ | 4 Point Probe | 2 Test Wafers/Run | |
| | | | XJ | Philtec Groove | 1 Test Chip/Run | Production Logbook |
| | | | TOX | Nanospec | 2 Product Wafers/ Run | |
|  | Sinker Mask | Resist Mask HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | |
|  | Sinker Predeposition | Deposition Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | Trend Chart |
| | | | $R_{\square}$ | 4 Point Probe | 2 Test Wafers/Run | |
|  | Sinker Diffusion | Diffusion Furnace | Visual | UV Lamp | 100% | Logbook |
| | | | | 20X Microscope | < 3 Defects/Field of View | |
| | | | $R_{\square}$ | 4 Point Probe | 2 Test Wafers/Run | |
| | | | TOX | Nanospec | 2 Test Wafers/Run | |

| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | Base Mask | Resist Mask HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | $\overline{X}$ and R |
|  | ISO Diode Check | Curve Tracer BVCSO | BVCSO | Curve Tracer | 4 Wafers/Run >1 Per 12 Readings Is Fail | Logbook |
|  | Base Predeposition | Deposition Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | $\overline{X}$ and R |
| | | | | 20X Microscope | 2 Wafers/Run < 4 Defects/Field of View | |
| | | | $R_{\square}$ | 4 Point Probe | 2 Test Wafers/Run | |
|  | Base Diffusion | Diffusion Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | Trend Chart |
| | | | | 20X Microscope | 2 Wafers/Run < 4 Defects/Field of View | |
| | | | $R_{\square}$ | 4 Point Probe | 2 Test Wafers/Run | |
| | | | TOX | Nanospec | 2 Product Wafers/ Run | |
|  | Emitter Mask | Resist Mask HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
|  | CB Diode Check | Curve Tracer | BVCBO | Curve Tracer | < 1 Out of 16 Readings is Fail | Logbook |
|  | Emitter Diffusion | Deposition Furnace | $R_{\square}$ | 4 Point Probe | 2 Test Chip/Cycle | Logbook |
| | | | Beta/LV | Curve Tracer | 3 Sites/Wafer Every Fourth Wafer > 2 Readings Out of Spec | |
|  | Contact Mask | Resist Mask HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | | | | Optical Microscope 1000X | Critical Dimension Measure. 2 Wafers/ Run Lot, Accept on 0 Failures | Trend Chart |
|  | Metal Deposition | Deposition Sputter Machine | Visual | UV Lamp | < 5 Defects/Wafer 100% | $\overline{X}$ and R |
| | | | $R_{\square}$/Thickness | 4 Point Probe | 2 Readings/Pass | |
|  | Metal Mask | Resist Mask Etchant Bath | Final Inspection | Optical Microscope 200X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | | | | Optical Microscope 1000X | Critical Dimension Measure. 2 Wafers/ Run Lot, Accept on 0 Failures | CD Logbook |

| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | Alloy | Anneal Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | Logbook |
|  | Electrical Test | To Evaluate Electrical Parameters LOMAC | | | 2 Wafers/Run | Logbook |
|  | LPOM | Passivation LPCVD Furnace | Visual | UV Lamp | 100%, > 2 Color Changes is Fail | $\overline{X}$ and R |
| | | | | 10X Microscope | 3 Wafers/Cycle < 3 Defects/Field of View | |
| | | | TOX | Nanospec | 3 Wafers/Cycle | |
| | | | Phosphorous Concentration | 10:1 HP Etch Rate | 3 Wafers/Cycle | |
|  | PEN | PECVD Nitride Deposition Furnace | Visual | UV Lamp | 100%, >2 Color Changes Is Fail | Trend Chart |
| | | | | 10X Microscope | 2 Wafers/Run, < 5 Defects/Field of View | |
| | | | Thickness | Nanospec | 3 Wafers/Cycle | |
| | | | Index of Refraction | Elipsometer | 3 Wafers/Cycle | |
|  | Pad Mask | Resist Mask RF Plasma Etch and Oxide Wet Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan. 100% of the Wafers | Production Log |
|  | Electrical Test | Evaluate Electrical Parameters | | | 100% | Logbook |
|  | Backlap | Disco. | N/A | N/A | N/A | Logbook |
|  | Backside Metal | Backside Metallization | Visual | Unaided Eye | 100% | Logbook |
|  | SEM | Step Coverage | 2 Photos | Scanning Electron Microscope | 1 Wafer/Week | Logbook |
| | | General Metallization | 1 Photo | | | |

## WAFER FABRICATION FLOWCHART
## Generic CMOS Process

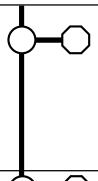
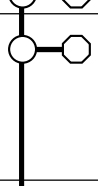
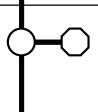
**Vendor:** Linear Technology Corporation
**Package:** Plastic SOIC/DIP
**Location of Wafer Fab:** Linear Technology Corporation, Milpitas, CA
**Assembly:** Carsem Unisem Penang Malaysia, ASAT Hong Kong
**Final Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Q.C. Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Source Accept Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Quality Contact:** QA Manager, LTC, Milpitas, CA
(408) 432-1900

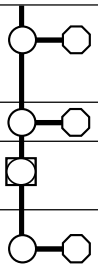



| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
| | Incoming Raw Material Inspection | Wafers | Visual: Scratches, Pits, Haze, Craters, Dimples, Contamination, | 1X Inspection | 1.0% AQL to 2.5% AQL Level 1 | % LAR Trend Chart and % Defective Trend Chart |
| | | | Oxygen/Carbon Measurement | Infrared Spectrometer | S/S = 2, $A_{CC}$ = 0 | |
| | | | Resistivity/ Conductivity | Magnetron V/I Meter | S/S = 2, $A_{CC}$ = 0 | |
| | | | Dimensional | Calipers | 2.5% AQL, Level S1 | |
| | | | Thickness and Taper/Bow | Dial Thickness Gauge | 2.5% AQL, Level S1 | |
| | | | Orientation | Break Test | S/S = 1, $A_{CC}$ = 0 | |
| | | | C of C Verification Against "MPS" Requirements | | Each Batch | |
| | | Photo Mask Plates | Visual C.D. Measurement | AMS-100 Calipers Comparator | Each Plate | Logbook |
| | | | | UV Lamp | Each Batch | Logbook |
| | | Chemicals | C of C Verification Against "MPS" Requirements | | | |
| | | Gases | Plus Yearly Gas Analysis | Outside Lab | Each Target | Logbook |
| | | Targets | C of C Verification | | | |
| | Initial Oxidation | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/ Field of View | Logbook |
| | | | Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
| | P-Well Mask | Resist Mask HF Etchant Bath | Visual | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | Pre-Implant Oxidation | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/ Field of View | Logbook |
| | | | Oxide Thickness | Nanospec | 3 Wafer/Cycle | |

| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | P-Well Implant | Implant | | | | Logbook |
|  | P-Well Drive | Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
|  | Strip All Oxide | HF Etchant Bath | | | | Logbook |
|  | Pad Oxidation | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
|  | Nitride Deposition | Nitride Furnace | Visual | UP Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | Nitride Thickness | Nanospec | 3 Wafers/Cycle | |
|  | Active Mask | RF Plasma Etch | Visual Inspection Critical Dimensions | Microscope 400X | "Z" Pattern Scan 100% of the Wafers | Production Log |
|  | Field Implant Mask | Resist Mask HF Etchant Bath | Visual Inspection | Microscope 400X | "Z" Pattern Scan 100% of the Wafers | Production Log |
|  | Boron Field Implant | Implant | | | | Logbook |
|  | CMOS Strip Resist | RF Plasma Sulfuric Acid | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Logbook |
|  | N-Field Implant Mask | Resist Mask HF Etchant Bath | UV Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Production Log |
| | | | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | |
|  | Photo Field Implant | Implant | | | | Logbook |
|  | CMOS Strip Resist | RF Plasma Sulfuric Acid | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Logbook |
|  | LOCOS Oxide | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
|  | Plasma Nitride Strip | RF Plasma Etch | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
|  | CMOS Cap Mask | Resist Mask HF Etchant Bath | Critical Dimensions | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
|  | Cap Implant | Implant | | | | Logbook |
|  | CMOS Strip Resist | RF Plasma Sulfuric Acid | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Logbook |
|  | Etch Pad Oxide | HF Etchant Bath | | | | Logbook |

| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
| | Gate Oxide | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | P-Channel Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
| | | | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | |
| | | | N-Channel Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
| | VTP Implant Mask | Resist Mask HF Etchant Bath | Visual | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | Boron VT Implant | Implant | | | | Logbook |
| | CMOS Strip Resist | RF Plasma Sulfuric Acid | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Logbook |
| | Poly Deposition | Furnace | Poly Thickness | | | Logbook |
| | Back Etch Mask | Resist Mask RF Plasma and HF Etchant Bath | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | Sinker Pre-Desposition | Deposition Furnace | Visual | UV Lamp (100%) 20X Microscope | 100% < 10 Defects/ Wafer | Trend Chart |
| | | | RS (Ω/sq) | 4 Point Probe | 2 Test Wafers/Run | |
| | CMOS Gate Mask | Resist Mask RF Plasma and HF Etchant Bath | Visual Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | P + Implant Mask | Resist Mask | Visual Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | P and S/D Implant | Implant | | | | Logbook |
| | CMOS Strip Resist | RF Plasma Sulfuric Acid | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | N + Implant Mask | Resist Mask | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Logbook |
| | N + S/D Implant | Implant | | | | Logbook |
| | CMOS Strip Resist | RF Plasma Sulfuric Acid | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Logbook |
| | Source Drain Re-Ox | Oxidation Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | P + Oxide Thickness | Nanospec | 3 Wafers/Cycle | |
| | | | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | |
| | | | N + Oxide Thickness | Nanospec | 3 Wafers/Cycle | |

| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | LPOE | LPOE LPCVD Furnace | Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Logbook |
| | | | LPOE Thickness | Nanospec | 3 Wafers/Cycle | |
|  | CMOS Getter | Furnace | RS (Ω/sq) | 4 Point Probe | 2 Test Wafers/Run | Trend Chart |
|  | CMOS Contact Mask | Resist Mask HF Etchant Bath | UV Visual | UV Lamp (100%) 20X Microscope | 2 Wafers/Run < 2 Defects/Field of View | Production Log |
| | | | Visual Inspection | Microscope 100X | "Z" Pattern Scan 100% of the Wafers | |
|  | Aluminum Desposition | Deposition Sputter Machine | Visual | UV Lamp | < 5 Defects/Wafer 100% | Logbook |
| | | | RS (Ω/sq) | 4 Point Probe | 2 Test Chip/Cycle | |
|  | CMOS Metal Mask | Resist Mask Metal Etchant Bath | Final Inspection Critical Dimensions | Optical Microscope 2 200X | "Z" Pattern Scan 100% of the Wafers | Production Log |
| | | | | Optical Microscope 2 1000X | Critical Dimension Measure 2 Wafers/ Run Lot, Accept On 0 Failures | |
|  | Alloy | Anneal Furnace | Visual | UV Lamp | 100% < 10 Defects/ Wafer | Logbook |
|  | Electrical Test | LOMAC Parametric Analyzer | | | 2 Wafers/Run | Logbook |
|  | LPOM | Passivation LPCVD Furnace | Visual | UV Lamp | 100%, More Than 2 Color Change Is Fail | Trend Chart |
| | | | | 10X Microscope | 3 Wafers/Cycle < 3 Defects/Field of View | |
| | | | LPOM Thickness | Nanospec | 3 Wafers/Cycle | |
| | | | Phosphorous Concentration | 10:1 HF Etch Rate | 3 Wafers/Cycle | |
|  | PEN | PECVD Nitride Deposition Furnace | Visual | UV Lamp | 100%, More Than 2 Color Change Is Fail | Trend Chart |
| | | | | 10X Microscope | 3 Wafers/Cycle < 5 Defects/Field of View | |
| | | | LPOM Thickness | Nanospec | 3 Wafers/Cycle | |
| | | | Index of Refraction | Elipsometer | 3 Wafers/Cycle | |
|  | Pad Mask | Resist Mask RF Plasma Etch and HF Etchant Bath | Final Inspection | Optical Microscope 100X | "Z" Pattern Scan 100% of the Wafers | Production Log |

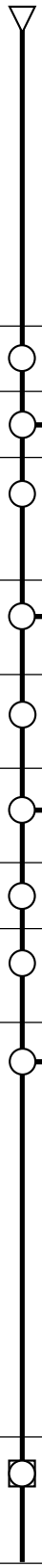
| FLOWCHART INCOMING FAB REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | Electrical Test | LOMAC Parametric Analyzer | | | 100% | Logbook |
| | Backlap | DISCO | N/A | N/A | N/A | Logbook |
| | Backside Gold | Backside Metallization | Visual | Unaided Eye | 100% | |
| | SEM | Step Coverage | 2 Photos | Scanning Electron Microscope | CMOS = 1 Wafer/ Week | Logbook |
| | | General Metal | 1 Photo | | N-Well and P-Well = 1 Wafer Every Run | |

## ASSEMBLY FLOWCHART
## Generic CMOS or Bipolar Process

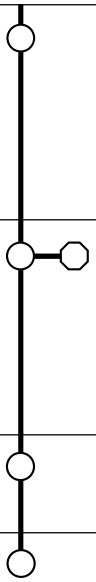
**Vendor:** Linear Technology Corporation
**Package:** Plastic SOIC
**Location of Wafer Fab:** Linear Technology Corporation, Milpitas, CA
**Assembly:** Carsem/Unisem/Penang-Malaysia, ASAT-Hong Kong
**Final Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Q.C. Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Source Accept Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Quality Contact:** QA Manager, LTC, Milpitas, CA
(408) 432-1900

▽ INCOMING
◯ QUALITY INSPECTION AND GATE
○ MANUFACTURING PROCESS
⯃ QUALITY MONITOR/SURVEILLANCE
□ REWORK

| FLOWCHART INCOMING ASSY REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
| ▽ | Incoming Raw Material Inspection | Wafers | Visual; Scratches Pits, Haze, Craters Dimples, Contamination | 1X Inspection | 1.0% AQL to 2.5% AQL Level I | % LAR Trend Chart and % Defective Trend Chart |
| | | | Oxygen/Carbon Measurement | Infrared Spectrometer | S/S = 2, ACC = 0 | |
| | | | Resistivity/ Conductivity | Magnetron V/I Meter | S/S = 2, ACC = 0 | |
| | | | Dimentional Thickness and Taper/Bow Orientation C of C Verification Against "MPS" | Calipers Dial Thickness Gauge Break Test | 2.5% AQL, Level S1 S/S = 1, ACC = 0 Each Bach | |
| | | Chemicals | Requirements Plus yearly | | Each Bath | |
| | | Gases | Gas Analysis | | | |
| ⯃ | Wafer Sort | 100% Die Level Electrical Test Rejects Are Red Inked | | Wafer Prober | | |
| | Wafer Sort Monitor | Monitor Probing and 2nd Optical Quality | Probe Defects 2nd Optical Defects | 3X to 75X Microscope | Minimum of 3 Times/Shift S/S = 1, ACC = 0 | % Defective Trend Chart |
| ○ | Kit for Overseas Assembly | Wafers Are Kitted with LTC Bonding Diagram and LTC Assembly Traveler | | | | |

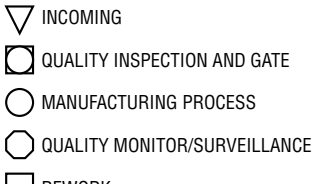
| FLOWCHART INCOMING ASSY REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | Incoming Piece Parts Inspection | Lead Frame | Visual | 10X to 30X Microscope | 1% AQL, Level 2 | % LAR Trend Chart |
| | | | Mechanical | Optical Comparator, Calipers, X-Ray Fluorescence | | |
| | | | Functional (Assembly Process Simulation): Bond Pull Test Die Shear Test | | | |
| | Wafer Mount | Preparation for Die Separation | Visual Inspection | Unaided Eye | 3 Wafers/Shift 0 PPM Target | Go/No Go Inspection |
| | Waver Mount Monitor | | | | | |
| | Wafer Saw | Die Separation | Alignment Accuracy | TV Alignment Micro Automation on Disco Saw 10X to 30X Microscope | Every Wafer/ Machine, 6 Cuts/ Wafer 0 PPM Target | nP Chart |
| | Wafer Saw Monitor | Saw KERF | Saw Quality Saw Accuracy | TM Microscope or Equivalent | Once/Shift 4 Cuts/Machine CPK 1.5 Target | $\overline{X}$ R Chart |
| | Die Attach | Die Bonded to Lead Frame with Epoxy | Visual Inspection | Auto Die Bonder | 2 Strips/Mag 0 PPM | nP Chart |
| | Die Attach Monitor | | Visual Quality Die Shear Test | 10X to 30X Microscope Die Shear Tester | 4 Units 1X/Machine/ Shift (or Per Customer Request) | Go/No Go |
| | Epoxy Cure | | Epoxy Cure | Pyrometer/TC | 1X/Machine/Shift CPK 1.5 Target | $\overline{X}$ R |
| | Wire Bond | Ball Bonds Gold 1.00 Mil Wire | Defects | Auto Thermosonic Ball Bonder | | |
| | Wire Bond Monitor | | Visual | Microscope | 4 Strip/Mag 0 PPM | nP Chart |
| | | | Bond Pull Strength | Bond Pull Tester | 10 Wires 1X/Machine/Shift CPK 1.5 | $\overline{X}$ R Chart |
| | | | Ball Shear | Ball Shear Tester | 10 Balls 1X/Machine/Shift CPK 1.5 | $\overline{X}$ R Chart |
| | | | Cratering Test | Visual | 4 Units/Day/Shift 0 PPM | Go/No Go |
| | | | Peel Test | Visual | 10 Wires 1X/Machine/Shift 0 PPM | Go/No Go |
| | QA 3rd Optical Inspection | Check for Workmanship Quality Prior to Molding | Die, Die Bond, Wire Bond Visual Quality | 30X to 60X Microscope | Every Lot AQL = 0.04% 0 PPM | |

| FLOWCHART INCOMING ASSY REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
| | Mold | Encapsulation with Epoxy Novalac | | Transfer Mold | | nP Chart |
| | Mold Monitor | Molding Quality | Visual: Chip, Void and Cracks, Misalignment, etc. | Unaided Eye 0 PPM | 7X/Shift/Machine 0 PPM | nP Chart |
| | | | Mold Temperature | Pyrometer | 1X/Shift/Machine CPK 1.5 | $\overline{X}$ R Chart |
| | | | Transfer Press | Hydr Load Cell | 1X/Month/Machine 4 Strips (Min) | Go/No Go |
| | | | Voids/Wire Sweep Visual Quality | X-Ray | 1X/Machine/Shift Change of Device Change of Compnd 0 PPM | nP Chart |
| | Mechanical Deflash | Remove Mold Flash from Package | L/F and Heat Sink Must Be Free from Mold Flash | 3X to 10X Microscope | 4 Strips (Min) 1X/Sublot/Machine 0 PPM | nP Chart |
| | Slurry Deflash | Remove Mold Flash from Package | L/F and Heat Sink Must Be Free from Mold Flash | Unaided Eye | 10 Strips/4X/Shift/ Machine 0 PPM | nP Chart |
| | Marking | | | | | |
| | Marking Permanency Test | Visual Inspection | Visual | Unaided Eye | 100% Inspect 0 PPM | Go/No Go |
| | | | MPT | Unaided Eye | 10 Units/Sublot 0 PPM | Go/No Go |
| | Post Mold Cure | Mold Quality | Temperature | Pyrometer | 1X/Machine/Shift CPK 1.5 | $\overline{X}$ R Chart |
| | Solder Plate | Solder Plate Bath | Visual Inspection | Unaided Eye | 5 Strips/4X/Shift 0 PPM | nP Chart |
| | | | | Thermometer | 1 Reading 2X/Shift CPK 1.5 | |
| | | | Thickness and Composition | XRF | 5 Frames/Shift CPK 1.5 | $\overline{X}$ R Chart |
| | Solder Plate Inspection | Solder Plate Quality | Visual Inspection | Unaided Eye Solderability Tester | 5 Units/Sublot 0 PPM | Go/No Go |
| | | | Steam Aging | 3X to 10X Microscope | 5 Units/Day/ Different Type of Package 0 PPM | Go/No Go |
| | | | Thickness and Composition | XRF | 5 Readings/Sublot 0 PPM | Go/No Go |
| | Trim and Form Singulation | Visual Inspection | Visual | Unaided Eye | 2 Tubes/Sublot 0 PPM | nP Chart |
| | | | Lead Gap/ Microcrack | 3X to 10X Microscope | 10 Units 1X/ Machine/Shift 0 PPM | Go/No Go |
| | | | Coplanarity | Jig and Microscope | 6 Units/Machine Min 1X/Shift 0 PPM | $\overline{X}$ R Chart |

| FLOWCHART INCOMING ASSY REWORK | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
|  | Final Visual | Visual | Mark, Correct Mark, Marking Permanency Test (If Ink Marked) Visual: Bent Leads Mold Flash, Solder Quality, Etc. | Unaided Eye | 100% 0 PPM | Go/No Go |
| | Final Visual Inspection | Visual Quality | Mark, Correct Mark, Marking Permanency Test (If Ink Marked) Visual: Bent Leads Mold Flash, Solder Quality, Etc. | Unaided Eye | S/S = 15 ACC = 0 | Go/No Go |
| | Pack | Packing and Preparation for Delivery | | Antistatic Shipping Tube | Every Lot 100% Basis | |
| | Ship to LTC | | | | | |

## EOL (END-OF-LINE) FLOWCHART
## Generic CMOS or Bipolar Process

**Vendor:** Linear Technology Corporation
**Package:** Plastic SOIC
**Location of Wafer Fab:** Linear Technology Corporation, Milpitas, CA
**Assembly:** Carsem/Unisem/Penang-Malaysia, ASAT-Hong Kong
**Final Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Q.C. Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Source Accept Test:** Linear Technology Corporation, Milpitas, CA, or Singapore
**Quality Contact:** QA Manager, LTC, Milpitas, CA
(408) 432-1900




| FLOWCHART | PROCESS STEP | DESCRIPTION | INSPECTION/ TEST CRITERIA | METHOD AND EQUIPMENT | SAMPLING PLAN | SPC TECHNIQUE |
|---|---|---|---|---|---|---|
| | LTC Incoming Inspection | Check Quality of Incoming Assembled Material | Package Dimension | Optical Comparator and Calipers | S/S = 2, $A_{CC}$ = 0 | % LAR Trend Chart |
| | | | External Visual | 3X to 30X Microscope | S/S = 76, $A_{CC}$ = 0 | |
| | | | Mark Permanency (If Ink-Marked) | MIL-STD-883 Method 2015 | S/S = 4, $A_{CC}$ = 0 | |
| | | | Solderability | MIL-STD-883 Method 2003 | S/S = 3, $A_{CC}$ = 0 | |
| | | | Die Attach Quality | Pliers | S/S = 5, $A_{CC}$ = 0 | |
| | | | Lead Fatigue Test | Lead Fatigue Tester | S/S = 10, $A_{CC}$ = 0 | |
| | Class Test | Electrical Test | Test to Guard-Banded Data Sheet Test Limits | LTX Integrated Circuit Test System | 100% | |
| | QA Electrical Test at 25°C | Electrical Quality | Test to Guard-Banded Data Sheet Test Limits | LTX Integrated Circuit Test System | S/S = 125, $A_{CC}$ = 0 | PPM Chart |
| | QA Electrical Test at 70°C and at 0°C | Electrical Quality | Test to Guard-Banded Data Sheet Test Limits | LTX Integrated Circuit Test System | S/S = 125, $A_{CC}$ = 3 | PPM Chart |
| | External Visual Inspection | Check for Package Quality | Visual: Bent Leads, Lead Form Criteria, Mold Voids/Cracks, etc. | 3X Eyepiece | 100% | Yield Chart |
| | QA Post Pack Inspection | Package/ Pack Quality Inspection | Verify Correct Top Mark, Correct Pack Method, Correct Labeling, External Visual Inspection | 3X to 10X Microscope Inspection | S/S = 125, $A_{CC}$ = 0 | % LAR and PPM P.A. Chart |
| | QA Shipbench Inspection | Plant Clearance Inspection | Paperwork Check, Verify Correct Part Number and Correct PAR Count | Unaided Eye Inspection | LTPD = 2%<br>S/S = 116, $A_{CC}$ = 0 | |
| | Ship to Customer | | | | | |