INTRODUCTION

Linear Technology Corporation (LTC) offers a wide variety of precision linear ICs in die form. It is our intent to offer dice electrically tested to levels which can be expected to yield the best possible performance in hybrid circuits. Complicating this task is the fact that many specifications given for our standard packaged products cannot be tested at the wafer level. Further, parameters which are 100% tested at wafer probe testing may shift during the die attach/assembly process.

Data sheets are available that contain ordering information for obtaining dice products. They are available from your local LTC Sales Rep, or from LTC Marketing.

GENERAL INFORMATION

Electrical Testing

Dice are 100% tested in wafer form at 25°C to the DC limits shown on the dice data sheet for a given device type. Many LTC packaged products have multiple electrical grades associated with a basic die type. A cross reference appears on each dice data sheet indicating which die product grade should be ordered to optimize candidates to meet the specifications of the desired finished product grade. This information should be used as a guideline only since LTC does not guarantee electrical specifications after assembly. Since electrical testing is done only at 25°C, no absolute guarantee can be made regarding performance at other temperatures. Some LTC products require post-package trimming to overcome certain assembly-related parameter shifts. Details on this trimming may be obtained by contacting the factory.

Visual Inspection

Dice are 100% visually inspected in accordance with MIL-STD-883, Method 2010 Condition B.

Chip Dimensions

Chip dimensions are as indicated on individual dice data sheets. Tolerance is ±1 mil. Chip thickness ranges from 12 mils to 20 mils, depending on product type. Bond pad dimensions are 4.5 mils × 4.5 mils minimum.

Topside Passivation

LTC products are passivated with a 2- layer system: a proprietary deposited oxide gives a crack-free conformal coverage of metal and oxide steps. A plasma nitride overcoat protects the die from ionic contamination and scratches during handling, testing and assembly. Note that LTC uses fuse link, laser and zener zap trimming techniques which may require windows in the passivation over the trim points. This passivation system is a major contributor to the extremely high reliability demonstrated throughout millions of device hours of accelerated testing of LTC devices in plastic and hermetic packages.

Topside Metallization

The metallization is a minimum of 11,000 Å thick unless otherwise specified. The quality of the metallization step coverage is monitored via a weekly SEM inspection per MIL-STD-883, Method 2018.

Backside Metal

Dice products are normally provided without backside metallization. Contact LTC for details about availability of LTC products with a particular backside metallization.

Backside Potential

LTC products are junction isolated. For proper operation the backside must be electrically connected to either the most negative potential seen by the IC or the most positive potential. This information is given in the individual dice data sheets.

Packaging

Dice are packaged in compartmentalized waffle packs for ease of handling and storage. Each waffle pack contains 100 dice. Special packaging methods are also available by contacting the factory.

Quality Levels of Dice Shipped

Each dice lot is guaranteed to meet the following requirements:

- Internal visual per MIL-STD-883, Method 2010, Condition B: 1.0% AQL Level II.
- Electrical: Due to variations in assembly methods and packaging techniques LTC does not guarantee electrical specifications after assembly. When a determination as to the finished products assembly yield is needed, the lot acceptance testing available at extra cost should be pursued.

Reliability Assurance

In addition to the more conventional reliability audits performed on finished products, LTC has innovated a unique periodic wafer fab reliability audit using a specially designed reliability structure that is stepped into all wafers. The test structure is optimized to accelerate the two primary failure mechanisms in linear circuits: mobile positive ions and surface charge-induced inversions. This provides a continuous monitor on the reliability performance of LTC's wafer fab processes and provides immediate feedback to wafer fab typically within one week.

Electrostatic Discharge (ESD) Precautions

Precision linear devices, especially those with very low (pA) input bias current levels and low (< 50µV) input offset voltages are susceptible to shifts in electrical performance and ESD damage as a result of improper handling. LTC recommends that ESD precautions, such as grounded conductive work stations, grounded conductive wrist straps and grounded equipment, be taken to prevent ESD damage.

ORDERING INFORMATION

Dice may be ordered by the part number defined in the dice data sheet. Minimum direct dice order per *delivery* is 1,000 pieces or $5,000, whichever is greater. Other minimums and conditions may also apply. Smaller quantities are available from authorized dice processing companies. In some cases, tighter parameter selections than indicated on the dice data sheets can be obtained by special order. Please contact the factory for details.

Lot Acceptance Testing

Lot acceptance testing (LAT) based on sample assembly and testing is available at extra cost. Sample sizes and acceptable electrical test limits vary from device to device and must be negotiated at the time of quoting. Contact the factory for details.