4-Channel, 3V Micropower Sampling 12-Bit Serial I/O A/D Converter

December 1995

FEATURES

- **12-Bit Resolution**
- **Auto Shutdown to 1nA**
- Low Supply Current: 160µA
- **Guaranteed ±3/4LSB Max DNL**
- Single Supply 3V Operation
- 4-Channel Multiplexer
- Separate MUX Output and ADC Input Pins
- MUX and ADC May Be Controlled Separately
- Sampling Rate: 10.5ksps
- I/O Compatible with SPI, MICROWIRE™, etc.
- 16-Pin SO Package

APPLICATIONS

- Pen Screen Digitizing
- Battery-Operated Systems
- Remote Data Acquisition
- Isolated Data Acquisition
- Battery Monitoring
- Temperature Measurement

DESCRIPTION

The LTC®1594L is a 4-channel, 3V micropower, 12-bit sampling A/D converter. It typically draws only 160µA of supply current when converting and automatically powers down to a typical supply current of 1nA between conversions. The LTC1594L is available in a 16-pin SO narrow package and operates on a 3V supply. The 12-bit, switched-capacitor, successive approximation ADC includes a 4-channel MUX and a sample-and-hold.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

The circuit can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

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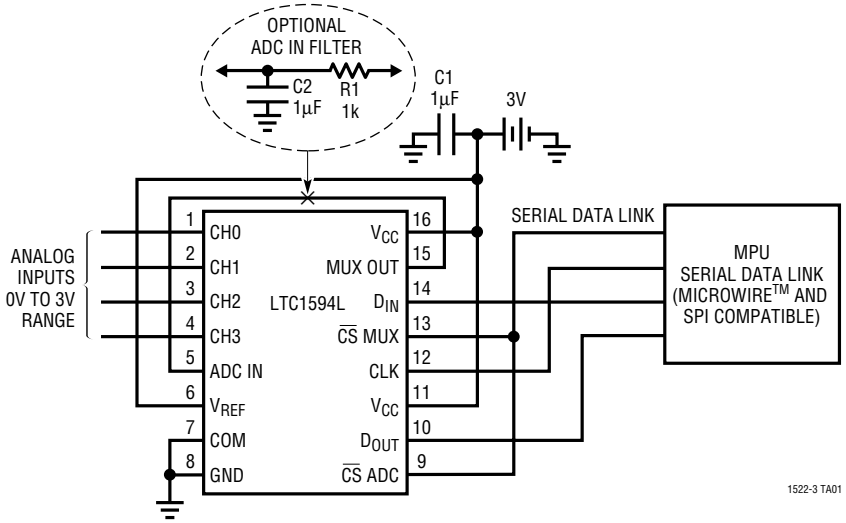
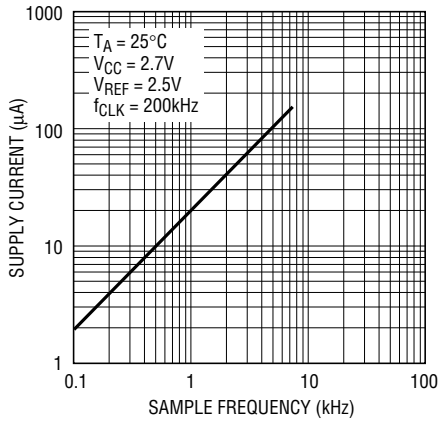
MICROWIRE is a trademark of National Semiconductor Corporation.

TYPICAL APPLICATION

12µW, 4-Channel, 12-Bit ADC Samples at 200Hz and Runs Off a 3V Battery



Supply Current vs Sample Rate



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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND 12V

Voltage

- Analog Reference ..... −0.3V to (V_{CC} + 0.3V)
- Analog Inputs ..... −0.3V to (V_{CC} + 0.3V)
- Digital Inputs .....−0.3V to 12V
- Digital Output ..... −0.3V to (V_{CC} +0.3V)

Power Dissipation 500mW

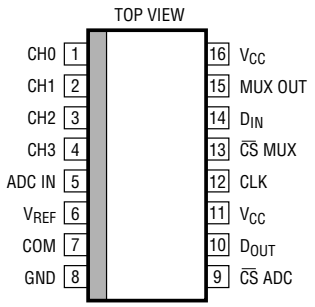
Operating Temperature Range

- LTC1594LCS ..... 0°C to 70°C
- LTC1594LIS ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO NARROW

T_{JMAX} = 125°C, θ_{JA} = 120°C/ W

ORDER PART NUMBER
LTC1594LCS LTC1594LIS

Consult factory for Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)		2.7		3.6	V
f_{CLK}	Clock Frequency	V_{CC} = 2.7V	(Note 4)		200	kHz
t_{CYC}	Total Cycle Time	f_{CLK} = 200kHz	95			µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 2.7V	2			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V	600			ns
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V	1.5			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V	1.5			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	f_{CLK} = 200kHz	25			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	f_{CLK} = 200kHz	70			µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1594LCS MIN	LTC1594LCS TYP	LTC1594LCS MAX	LTC1594LIS MIN	LTC1594LIS TYP	LTC1594LIS MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 6)	●			±3			±3	LSB
Differential Linearity Error		●			±3/4			±1	LSB
Offset Error		●			±3			±3	LSB
Gain Error		●			±8			±8	LSB
REF Input Range	(Notes 7, 8)			1.5V to V_{CC} + 0.05V					V
Analog Input Range	(Notes 7, 8)			−0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Note 9)	●			±1			±1	µA

DYNAMIC ACCURACY (Note 5) f_{SMPL} = 10.5kHz

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		68		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		−78		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		80		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		−80		dB

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.40 2.10	2.64 2.30		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			15		mA
R_{REF}	Reference Input Resistance	$\overline{CS} = V_{IH}$ $\overline{CS} = V_{IL}$			2700 60		MΩ kΩ
I_{REF}	Reference Current	$\overline{CS} = V_{CC}$ $t_{CYC} \geq 760\mu s$, $f_{CLK} \leq 25kHz$ $t_{CYC} \geq 95\mu s$, $f_{CLK} \leq 200kHz$	● ●		0.001 50 50	2.5 70	µA µA µA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$, CLK = V_{CC}, $D_{IN} = V_{CC}$ $t_{CYC} \geq 760\mu s$, $f_{CLK} \leq 25kHz$ $t_{CYC} \geq 95\mu s$, $f_{CLK} \leq 200kHz$	● ●		0.001 160 160	±3 320	µA µA µA

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence 1			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	See Operating Sequence 1		10.5			kHz
t_{CONV}	Conversion Time	See Operating Sequence 1			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		600	1500	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	600	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		180	500	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			520		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		60	180	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	180	ns
t_{ON}	Enable Turn-On Time	See Operating Sequence 1	●		540	1200	ns
t_{OFF}	Enable Turn-Off Time	See Operating Sequence 2	●		190	500	ns
t_{OPEN}	Break-Before-Make Interval			125	350		ns
C_{IN}	Input Capacitance	Analog Inputs On-Channel Off-Channel Digital Input			20 5 5		pF pF pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: This device is specified at 2.7V. Consult factory for 5V specified devices.

Note 4: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that f_{CLK} = 200kHz at 85°C, $f_{CLK} \geq$ 120kHz at 70°C and $f_{CLK} \geq$ 1kHz at 25°C.

Note 5: V_{CC} = 2.7V, V_{REF} = 2.5V and CLK = 200kHz unless otherwise specified.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for 2.7V ≤ V_{CC} ≤ 3.6V. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 3V input voltage range will therefore require a minimum supply voltage of 2.950V over initial tolerance, temperature variations and loading.

Note 8: Recommended operating condition.

Note 9: Channel leakage current is measured after the channel selection.

PIN FUNCTIONS

CH0 (Pin 1): Analog Multiplexer Input.

CH1 (Pin 2): Analog Multiplexer Input.

CH2 (Pin 3): Analog Multiplexer Input.

CH3 (Pin 4): Analog Multiplexer Input.

ADC IN (Pin 5): ADC Input. This input is the positive analog input to the ADC. Connect this pin to MUX OUT for normal operation.

V_{REF} (Pin 6): Reference Input. The reference input defines the span of the ADC.

COM (Pin 7): Negative Analog Input. This input is the negative analog input to the ADC and must be free of noise with respect to GND.

GND (Pin 8): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$ ADC (Pin 9): ADC Chip Select Input. A logic high on this input deselects and powers down the ADC and three-states D_{OUT}. A logic low on this input enables the ADC to sample the selected channel and start the conversion. For normal operation drive this pin in parallel with $\overline{CS}$ MUX.

D_{OUT} (Pin 10): Digital Data Output. The A/D conversion result is shifted out of this output.

V_{CC} (Pin 11): Power Supply Voltage. This pin provides power to the ADC. It must be bypassed directly to the analog ground plane.

CLK (Pin 12): Shift Clock. This clock synchronizes the serial data transfer to both MUX and ADC.

$\overline{CS}$ MUX (Pin 13): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUX OUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{CS}$ ADC.

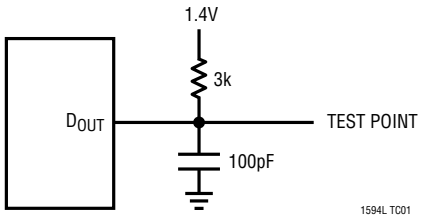
D_{IN} (Pin 14): Digital Data Input. The multiplexer address is shifted into this input.

MUX OUT (Pin 15): MUX Output. This pin is the output of the multiplexer. Tie to ADC IN for normal operation.

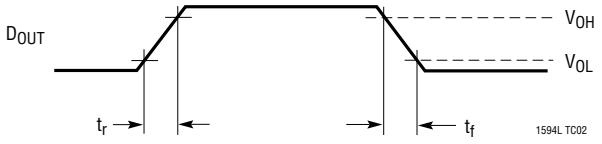
V_{CC} (Pin 16): Power Supply Voltage. This pin should be tied to Pin 11.

TEST CIRCUITS

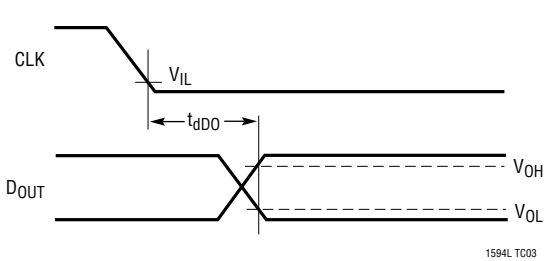
Load Circuit for t_{dDO}, t_r and t_f



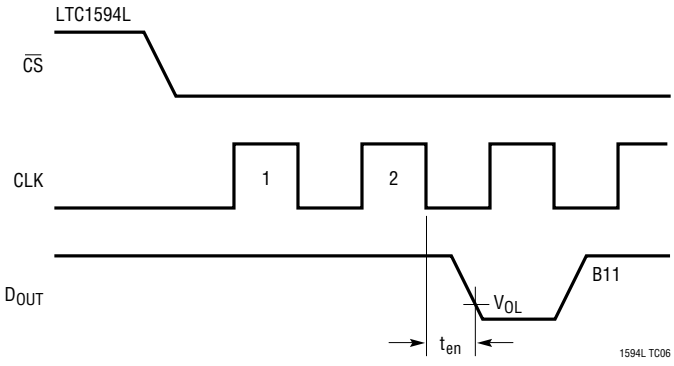
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}

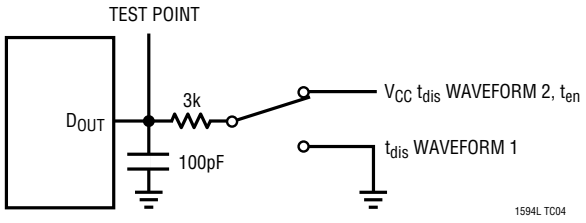


Voltage Waveforms for t_{en}

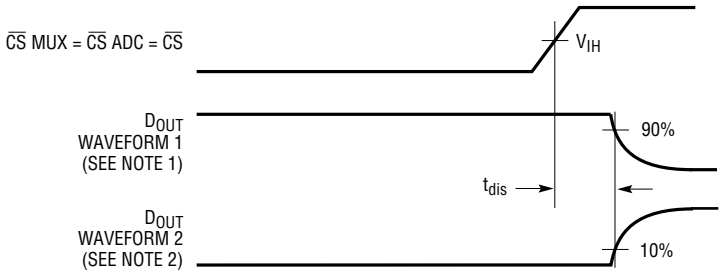


TEST CIRCUITS

Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

1594L TC05

APPLICATIONS INFORMATION

INPUT DATA WORD

The LTC1594L uses its Chip Select pins and D_{IN} to select one of its four channels as shown in the operating sequence figures and Table 1. For this discussion we will assume that $\overline{CS}$ MUX and $\overline{CS}$ ADC are tied togther and will refer to them as simply $\overline{CS}$.

When $\overline{CS}$ is high, the input data on the D_{IN} pin is latched into the 4-bit shift register on the rising edge of the clock. The input data word consists of an "EN" bit and a string of three bits for channel selection. If the "EN" bit is logic high as illustrated in Operating Sequence 1, it enables the selected channel. To ensure correct operation, the $\overline{CS}$ must be pulled low before the next rising edge of the clock. More than four input bits can be sent to the ADC without problems. The channel will be determined by the last four bits clocked in before $\overline{CS}$ falls.

Once the $\overline{CS}$ is pulled low, all channels are simultaneously switched off to ensure a break-before-make interval. After a delay of t_{ON}, the selected channel is switched on allowing signal transmission. The selected channel remains on until the next falling edge of $\overline{CS}$; and after a delay of t_{OFF}, it turns off and subsequently allows the selection of the next channel. If the "EN" bit is logic low, as illustrated in Operating Sequence 2, it disables all channels. Table 1 shows the various bit combinations for channel selection.

Table 1. Logic Table for Channel Selection

Channel Status	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1

ANALOG CONSIDERATIONS

Grounding

The LTC1594L should be used with an analog ground plane and single-point grounding techniques. Do not use wire-wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a printed circuit board. The Ground pin (Pin 8) should be tied directly to the ground plane with minimum lead length.

Bypassing

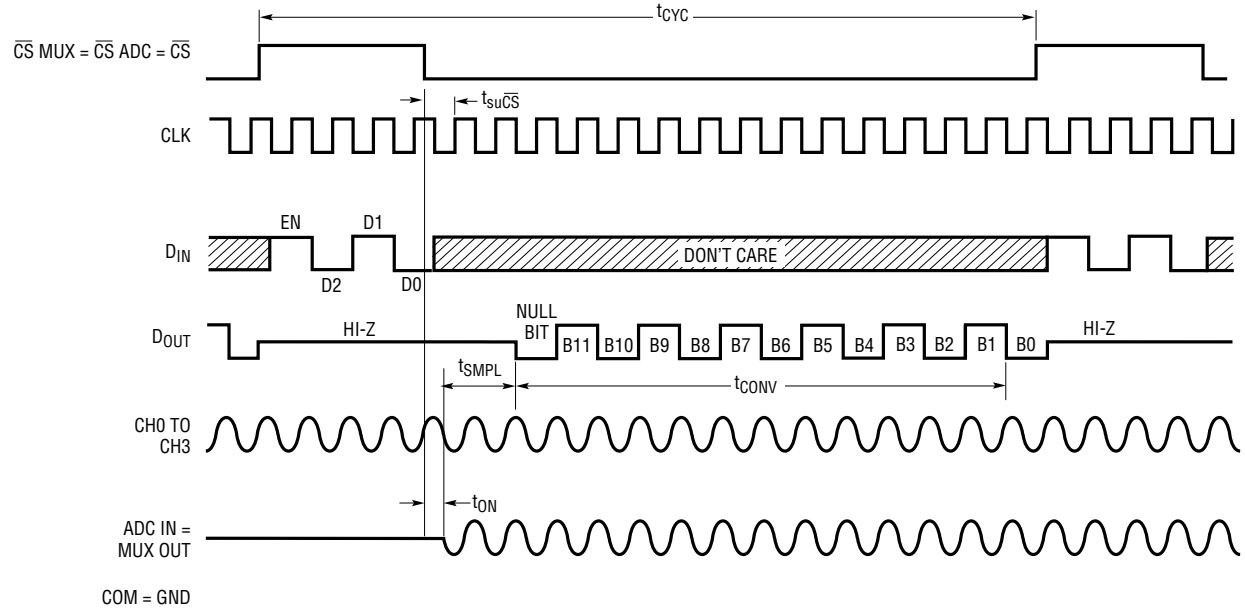
For good performance, the LTC1594L V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC}/V_{REF} pin directly to the analog ground plane with a minimum of a 0.1μF capacitor and leads as short as possible.

APPLICATIONS INFORMATION

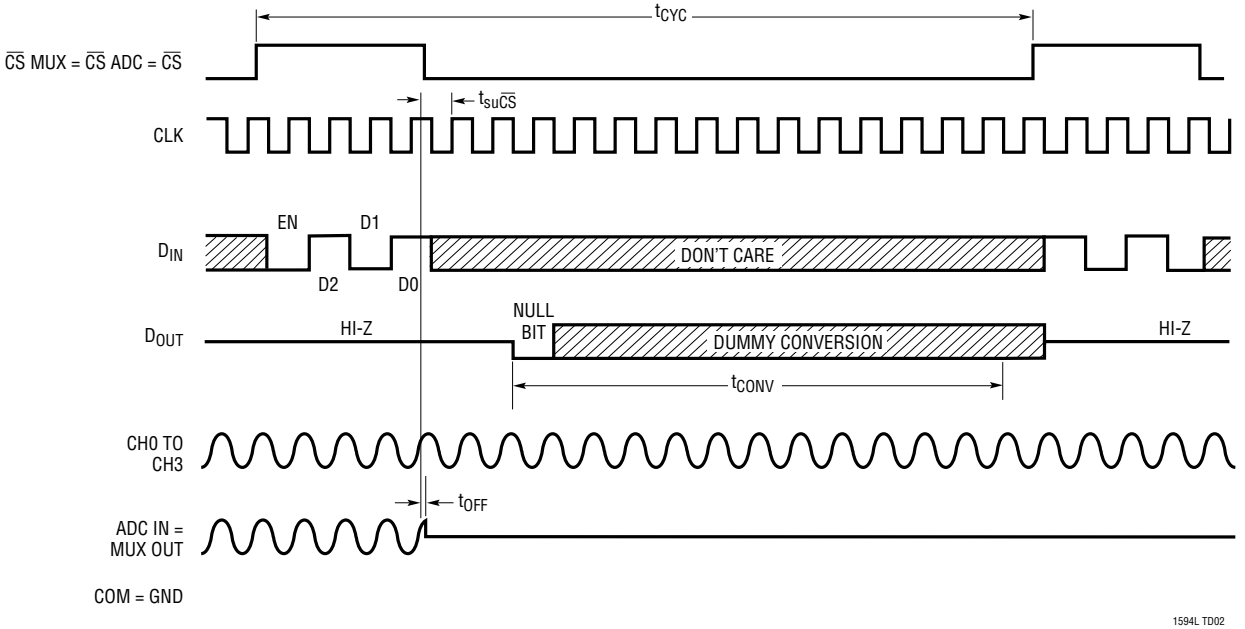
Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1594L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. But if large source resistances are used or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

Operating Sequence 1
Example: (CH2, GND)



Operating Sequence 2
Example: (ALL Channels Off)



TYPICAL APPLICATIONS

Microprocessor Interfaces

The LTC1594L can interface directly (without external hardware) to most popular microprocessors' (MPU) synchronous serial formats (see Table 2). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1594L. Included here is one serial interface example.

Table 2. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1594L**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE
COP800 Family	MICROWIRE/PLUS™
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

* Requires external hardware.

** Contact factory for interface information for processors not on this list.

MICROWIRE/PLUS is a trademark of National Semiconductor Corp.

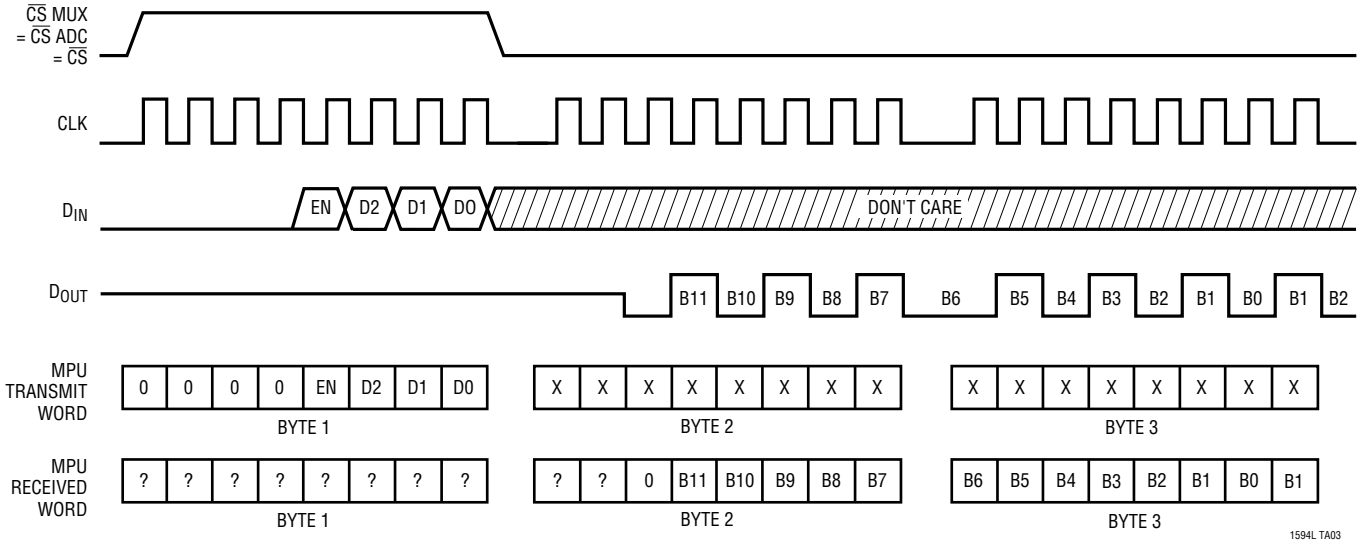
Motorola SPI (MC68HC05)

The MC68HC05 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B7 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits B6 through B0 into the MPU. ANDing the second byte with $1F_{HEX}$ clears the three most significant bits and ANDing the third byte with FE_{HEX} clears the least significant bit.

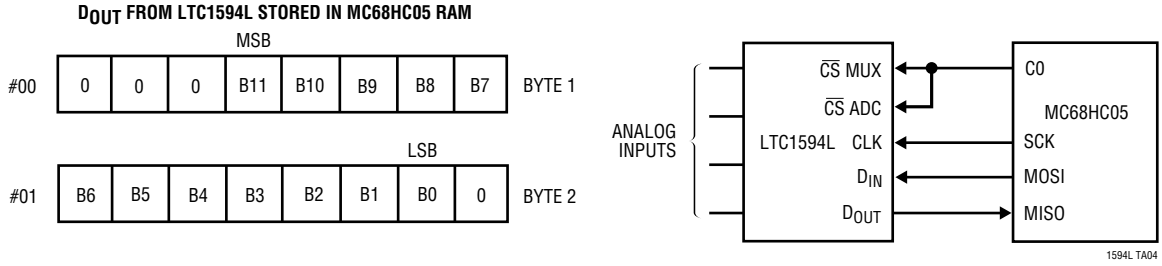
MC68HC05 CODE			
	LDA	#$52	Configuration data for serial peripheral control register (Interrupts disabled, output enabled, master, Norm = 0, Ph = 0, Clk/16)
	STA	$0A	Load configuration data into location $0A (SPCR)
	LDA	#$FF	Configuration data for I/O ports (all bits are set as outputs)
	STA	$04	Load configuration data into Port A DDR ($04)
	STA	$05	Load configuration data into Port B DDR ($05)
	STA	$06	Load configuration data into Port C DDR ($06)
	LDA	#$08	Put D_{IN} word for LTC1594L into Accumulator (CH0 with respect to GND)
	STA	$50	Load D_{IN} word into memory location $50
START	BSET	0,$02	Bit 0 Port C ($02) goes high ($\overline{CS}$ goes high)
	LDA	$50	Load D_{IN} word at $50 into Accumulator
	STA	$0C	Load D_{IN} word into SPI data register ($0C) and start clocking data
LOOP1	TST	$0B	Test status of SPIF bit in SPI status register ($0B)
	BPL	LOOP1	Loop if not done with transfer to previous instruction
	BCLR	0,$02	Bit 0 Port C ($02) goes low ($\overline{CS}$ goes low)
	LDA	$0C	Load contents of SPI data register into Accumulator
	STA	$0C	Start next SPI cycle
LOOP2	TST	$0B	Test status of SPIF
	BPL	LOOP2	Loop if not done
	LDA	$0C	Load contents of SPI data register into Accumulator
	STA	$0C	Start next SPI cycle
	AND	#$IF	Clear 3 MSBs of first D_{OUT} word
	STA	$00	Load Port A ($00) with MSBs
LOOP3	TST	$0B	Test status of SPIF
	BPL	LOOP3	Loop if not done
	LDA	$0C	Load contents of SPI data register into Accumulator
	AND	#$FE	Clear LSB of second D_{OUT} word
	STA	$01	Load Port B ($01) with LSBs
	JMP	START	Go back to start and repeat program

TYPICAL APPLICATIONS

Data Exchange Between LTC1594L and MC68HC05



Hardware and Software Interface to Motorola MC68HC05



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1096/LTC1098	8-Pin SO, Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1096L/LTC1098L	8-Pin SO, 2.65V Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1196/LTC1198	8-Pin SO, 1Msps 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1282	3V High Speed Parallel 12-Bit ADC	140ksps, Complete with V_{REF}, CLK, Sample-and-Hold
LTC1285/LTC1288	8-Pin SO, 3V Micropower 12-Bit ADC	12-Bit ADC in SO-8
LTC1289	Mutiplexed 3V, 12-Bit ADC	8-Channel 12-Bit Serial I/O

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