8-Channel Analog Multiplexer with Cascadable Serial Interface

FEATURES

- **Low R_{ON}: 45Ω**
- **Single 2.7V to ±5V Supply Operation**
- Analog Inputs May Extend to Supply Rails
- **Low Charge Injection**
- **Serial Digital Interface**
- Low Leakage: ±5nA Max
- Guaranteed Break-Before-Make
- TTL/CMOS Compatible for All Digital Inputs
- Cascadable to Allow Additional Channels
- Can Be Used as a Demultiplexer

APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing

DESCRIPTION

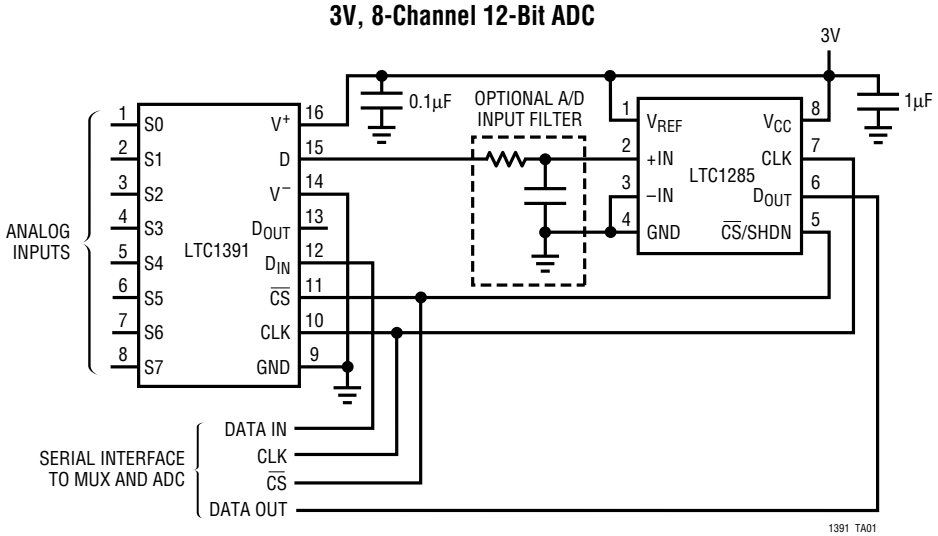
The LTC®1391 is a high performance CMOS 8-to-1 analog multiplexer. It features a serial digital interface that allows several LTC1391s to be daisy-chained together, increasing the number of MUX channels available using a single digital port.

The LTC1391 features a typical R_{ON} of 45Ω, a typical switch leakage of 50pA and guaranteed break-before-make operation. Charge injection is ±10pC maximum. All digital inputs are TTL and CMOS compatible when operated from single or dual supplies. The inputs can withstand 100mA fault current.

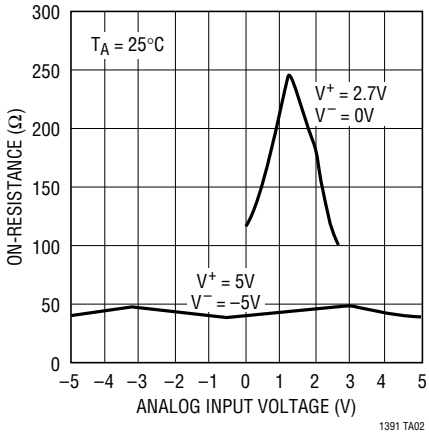
The LTC1391 is available in 16-pin PDIP and narrow SO packages. For applications requiring 2-way serial data transmission, see the LTC1390 data sheet.

TYPICAL APPLICATION

3V, 8-Channel 12-Bit ADC



On-Resistance vs Analog Input Voltage

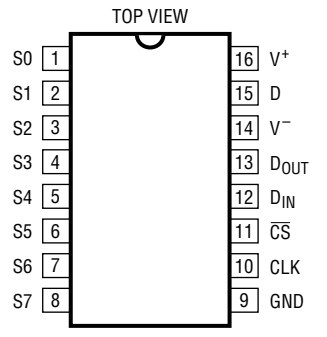


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage
  Analog Inputs ..... (V^- – 0.3V) to (V^+ + 0.3V)
  Digital Inputs .....–0.3V to 15V
  Digital Outputs.....–0.3V to (V^+ + 0.3V)
Power Dissipation..... 500mW
Operating Temperature Range
  LTC1391C..... 0°C to 70°C
  LTC1391I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PDIP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER
LTC1391CN
LTC1391CS
LTC1391IN
LTC1391IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = –5V, GND = 0V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch								
V_{ANALOG}	Analog Signal Range	(Note 2)		●	–5		5	V
R_{ON}	On-Resistance	V_S = ±3.5V	T_{MIN}				75	Ω
		I_D = 1mA	25°C			45	75	Ω
			T_{MAX}				120	Ω
	ΔR_{ON} vs V_S					20		%
	ΔR_{ON} vs Temperature					0.5		%/°C
$I_{S(OFF)}$	Off Input Leakage	V_S = 4V, V_D = –4V, V_S = –4V, V_D = 4V				±0.05	±5	nA
		Channel Off		●			±20	nA
$I_{D(OFF)}$	Off Output Leakage	V_S = 4V, V_D = –4V, V_S = –4V, V_D = 4V				±0.05	±5	nA
		Channel Off		●			±20	nA
$I_{D(ON)}$	On Channel Leakage	V_S = V_D = ±4V				±0.05	±5	nA
		Channel On		●			±20	nA
Digital								
V_{INH}	High Level Input Voltage	V^+ = 5.25V		●	2.4			V
V_{INL}	Low Level Input Voltage	V^+ = 4.75V		●			0.8	V
I_{INL}, I_{INH}	Input Current	V_{IN} = 5V, 0V		●			±5	µA
V_{OH}	High Level Output Voltage	V^+ = 4.75V, I_O = –10µA				4.74		V
		I_O = –360µA		●	2.4	4.50		V
V_{OL}	Low Level Output Voltage	V^+ = 4.75V, I_O = 1.6mA		●		0.5	0.8	V
Dynamic								
f_{CLK}	Clock Frequency	(Note 2)					5	MHz
t_{ON}	Enable Turn-On Time	V_S = 2.5V, R_L = 1k, C_L = 35pF				260	400	ns
t_{OFF}	Enable Turn-Off Time	V_S = 2.5V, R_L = 1k, C_L = 35pF				100	200	ns
t_{OPEN}	Break-Before-Make Interval				35	155		ns
OIRR	Off Isolation	V_S = $2V_{P-P}$, R_L = 1k, f = 100kHz				70		dB
Q_{INJ}	Charge Injection	R_S = 0, C_L = 1000pF, V_S = 1V (Note 2)				±2	±10	pC

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = -5V$, GND = 0V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Dynamic								
$C_{S(OFF)}$	Input Off Capacitance					5		pF
$C_{D(OFF)}$	Output Off Capacitance					10		pF
Supply								
I^+	Positive Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or 5V		●		15	40	µA
I^-	Negative Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or 5V		●		–15	–40	µA

$V^+ = 2.7V$, $V^- =$ GND = 0V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch								
V_{ANALOG}	Analog Signal Range	(Note 2)		●	0		2.7	V
R_{ON}	On-Resistance	V_S = 1.2V, I_O = 1mA	T_{MIN}				300	Ω
			25°C			250	300	Ω
			T_{MAX}				350	Ω
	ΔR_{ON} vs V_S					20		%
	ΔR_{ON} vs Temperature					0.5		%/°C
$I_{S(OFF)}$	Off Input Leakage	V_S = 2.5V, V_D = 0.5V; V_S = 0.5V, V_D = 2.5V (Note 3)				±0.05	±5	nA
		Channel Off		●			±20	nA
$I_{D(OFF)}$	Off Output Leakage	V_S = 2.5V, V_D = 0.5V; V_S = 0.5V, V_D = 2.5V (Note 3)				±0.05	±5	nA
		Channel Off		●			±20	nA
$I_{D(ON)}$	On Channel Leakage	V_S = V_D = 0.5V, 2.5V (Note 3)				±0.05	±5	nA
		Channel On		●			±20	nA
Digital								
V_{INH}	High Level Input Voltage	V^+ = 3.0V		●	2.0			V
V_{INL}	Low Level Input Voltage	V^+ = 2.4V		●			0.8	V
I_{INL}, I_{INH}	Input Current	V_{IN} = 2.7V, 0V		●			±5	µA
V_{OH}	High Level Output Voltage	V^+ = 2.7V, I_O = –20µA				2.68		V
		I_O = –400µA		●	2.0	2.30		V
V_{OL}	Low Level Output Voltage	V^+ = 2.7V, I_O = 20µA				0.01		V
		I_O = 400µA		●		0.20	0.8	V
Dynamic								
f_{CLK}	Clock Frequency	(Note 2)					5	MHz
t_{ON}	Enable Turn-On Time	V_S = 1.5V, R_L = 1k, C_L = 35pF (Note 4)				490	800	ns
t_{OFF}	Enable Turn-Off Time	V_S = 1.5V, R_L = 1k, C_L = 35pF (Note 4)				190	400	ns
t_{OPEN}	Break-Before-Make Interval	(Note 4)			125	290		ns
QIRR	Off Isolation	V_S = $2V_{P-P}$, R_L = 1k, f = 100kHz				70		dB
Q_{INJ}	Charge Injection	R_S = 0, C_L = 1000pF, V_S = 1V (Note 2)				±1	±5	pC
$C_{S(OFF)}$	Input Off Capacitance					5		pF
$C_{D(OFF)}$	Output Off Capacitance					10		pF
Supply								
I^+	Positive Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or 2.7V		●		0.2	2	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

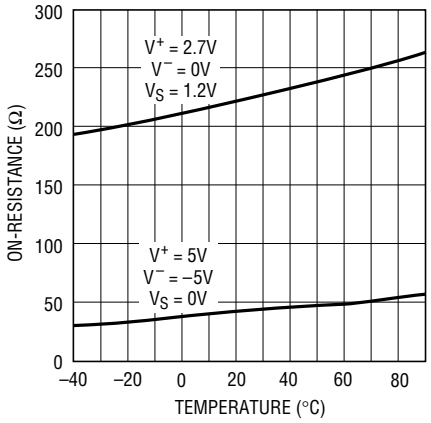
Note 2: Guaranteed by Design.

Note 3: Leakage current with a single 2.7V supply is guaranteed by correlation with the ±5V leakage current specifications.

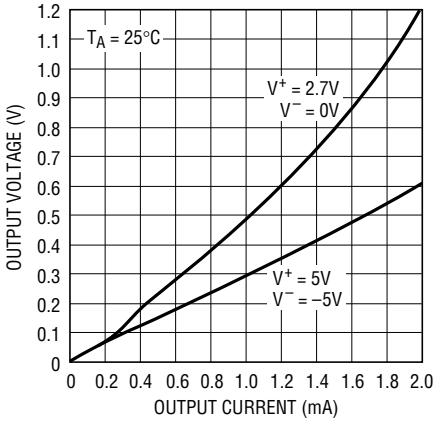
Note 4: Timing specifications with a single 2.7V supply are guaranteed by correlation with the ±5V timing specifications.

TYPICAL PERFORMANCE CHARACTERISTICS

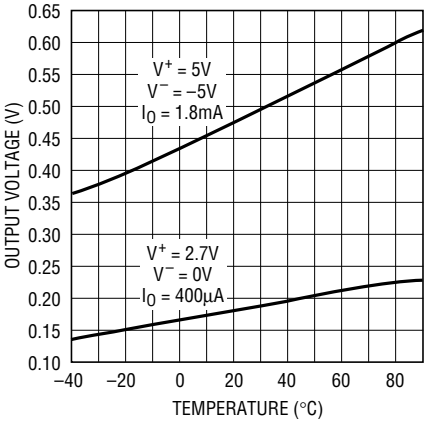
On-Resistance vs Temperature



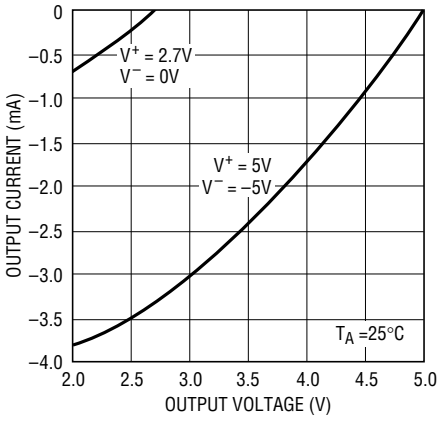
Driver Output Low Voltage vs Output Current



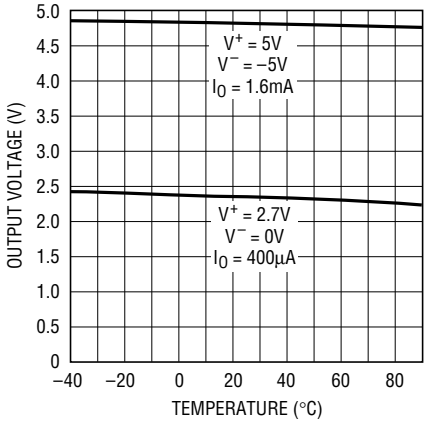
Driver Output Low Voltage vs Temperature



Driver Output High Voltage vs Output Current



Driver Output High Voltage vs Temperature



PIN FUNCTIONS

S0, S1, S2, S3, S4, S5, S6, S7 (Pins 1, 2, 3, 4, 5, 6, 7, 8): Analog Multiplexer Inputs.

GND (Pin 9): Digital Ground. Connect to system ground.

CLK (Pin 10): System Clock (TTL/CMOS Compatible). The clock synchronizes the channel selection bits and the serial data transfer from D_{IN} to D_{OUT}.

$\overline{CS}$ (Pin 11): Channel Select Input (TTL/CMOS Compatible). A logic high on this input enables the LTC1391 to read in the channel selection bits and allows digital data transfer from D_{IN} to D_{OUT}. A logic low on this input puts D_{OUT} into three-state and enables the selected channel for analog signal transmission.

D_{IN} (Pin 12): Digital Input (TTL/CMOS Compatible). Input for the channel selection bits.

D_{OUT} (Pin 13): Digital Output (TTL/CMOS Compatible). Output from the internal shift register.

V^- (Pin 14): Negative Supply.

D (Pin 15): Analog Multiplexer Output.

V^+ (Pin 16): Positive Supply.

APPLICATIONS INFORMATION

Multiplexer Operation

Figure 1 shows the block diagram of the components within the LTC1391 required for MUX operation. The LTC1391 uses D_{IN} to select the active channel and the chip select input, $\overline{CS}$, to switch on the selected channel as shown in Figure 2.

When $\overline{CS}$ is high, the input data on the D_{IN} pin is latched into the 4-bit shift register on the rising clock edge. The input data consists of the "EN" bit and a string of three bits for channel selection. If "EN" bit is logic high as illustrated in the first input data sequence, it enables the selected channel. After the clocking in of the last channel selection bit B0, the $\overline{CS}$ pin must be pulled low before the next rising clock edge to ensure correct operation. Once $\overline{CS}$ is pulled low, the previously selected channel is switched off to ensure a break-before-make interval. After a delay of t_{ON}, the selected channel is switched on allowing signal transmission. The selected channel remains on until the next falling edge of $\overline{CS}$. After a delay of t_{OFF}, the LTC1391 terminates the analog signal transmission and allows the selection of next channel. If the "EN" bit is logic low, as illustrated in the second data sequence, it disables all channels and there will be no analog signal transmission. Table 1 shows the various bit combinations for channel selection.

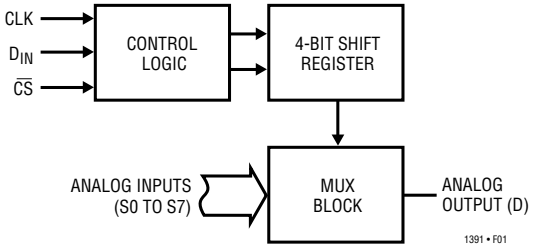


Figure 1. Simplified Block Diagram of the MUX Operation

Table 1. Logic Table for Channel Selection

ACTIVE CHANNEL	EN	B2	B1	B0
All Off	0	X	X	X
S0	1	0	0	0
S1	1	0	0	1
S2	1	0	1	0
S3	1	0	1	1
S4	1	1	0	0
S5	1	1	0	1
S6	1	1	1	0
S7	1	1	1	1

Digital Data Transfer Operation

The block diagram of Figure 3 shows the components within the LTC1391 required for serial data transfer. When $\overline{CS}$ is held high, data is fed into the 4-bit shift register and then shifted to D_{OUT}. Data appears at D_{OUT} after the fourth rising edge of the clock as shown in Figure 4. The last four

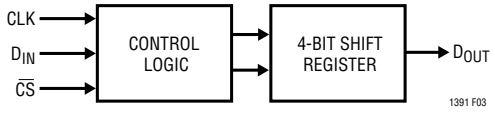


Figure 3. Simplified Block Diagram of the Digital Data Transfer Operation

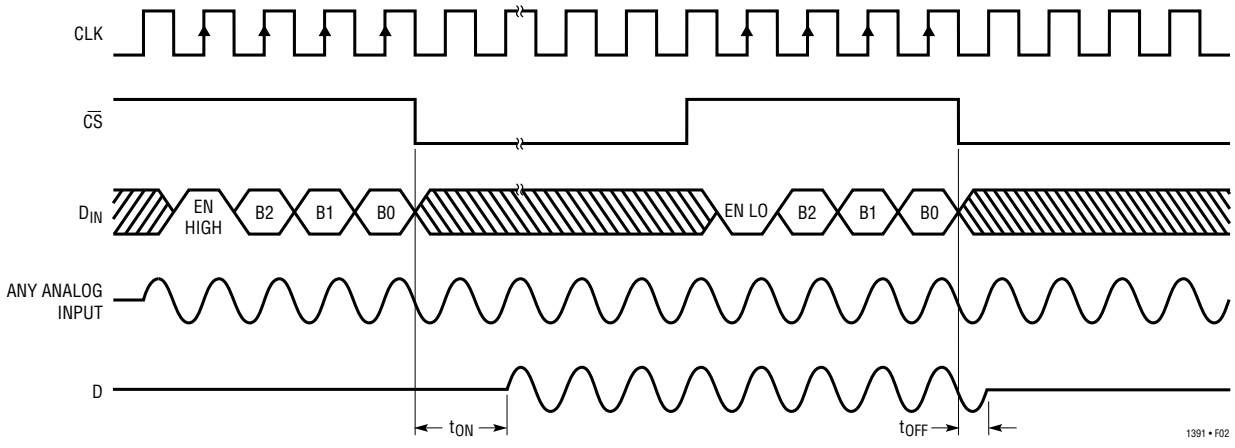


Figure 2. Multiplexer Operation

APPLICATIONS INFORMATION

bits clocked into the LTC1391 shift register before $\overline{CS}$ is taken low select the MUX channel that is turned on. This allows a series of devices, with the D_{OUT} of one device connected to the D_{IN} of the next device, to be programmed with a single data stream.

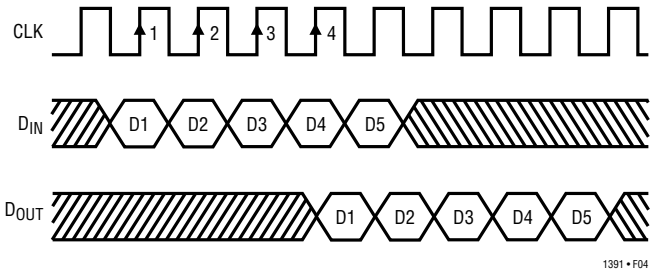


Figure 4. Digital Data Transfer Operation

Multiplexer Expansion

Several LTC1391s can be daisy-chained to expand the number of multiplexer inputs. No additional interface ports are required for the expansion. Figure 5 shows two LTC1391s connected at their analog outputs to form a 16-to-1 multiplexer at the input to an LTC1400 A/D converter.

To ensure that only one channel is switched on at any one time, two sets of channel selection bits are needed for DATA as shown in Figure 6. The first data sequence is used to switch off one MUX and the second data sequence is used to select one channel from the other MUX or vice versa. In other words, if bit "ENA" is high and bit "ENB" is low, one channel of MUX A is switched on and all channels of MUX B are switched off. If bit "ENA" is low and bit "ENB" is high, all channels at MUX A are switched off and one channel of MUX B is switched on. Care should be taken to ensure that only one LTC1391 is enabled at any one time to prevent two channels from being enabled simultaneously.

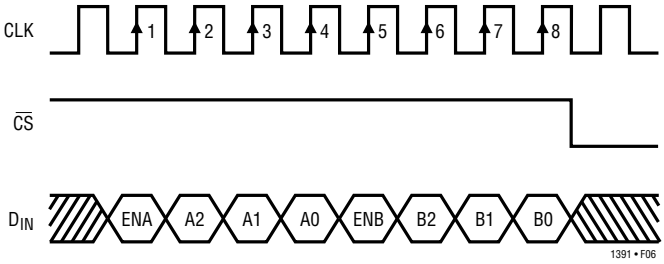


Figure 6. Data Sequence for MUX Expansion

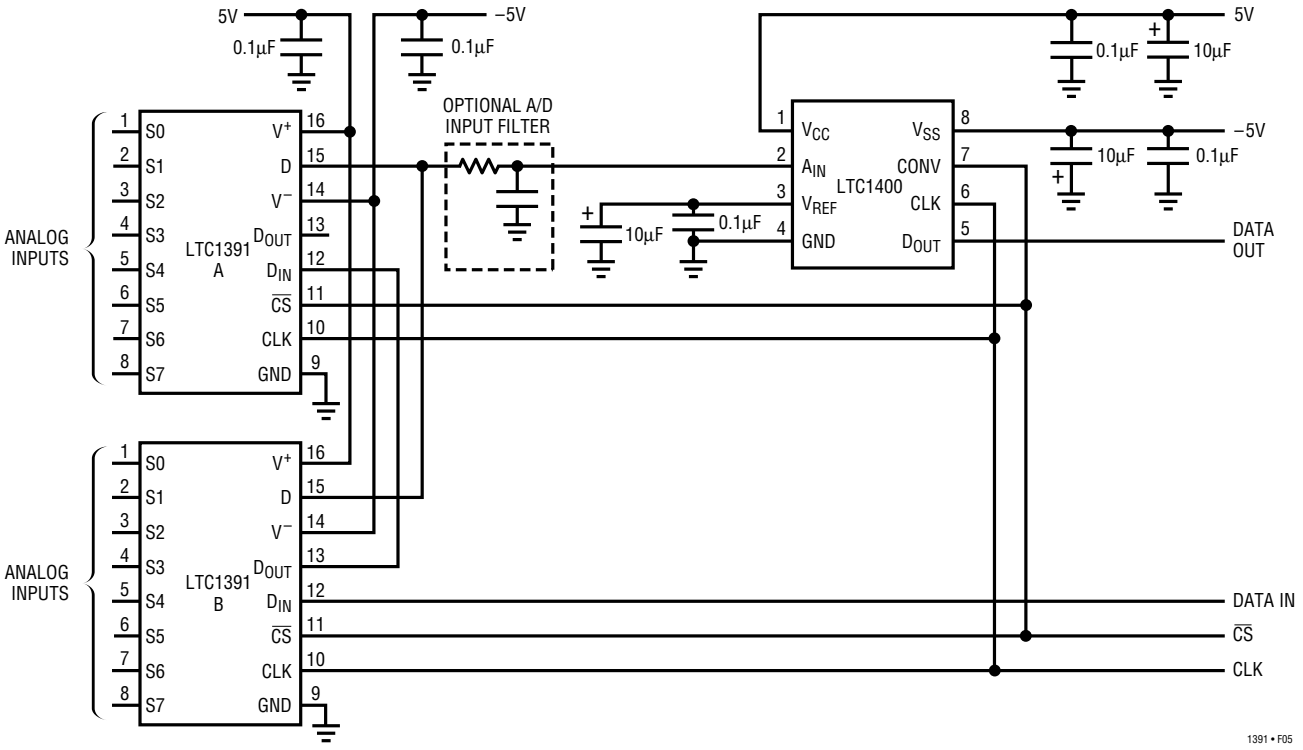
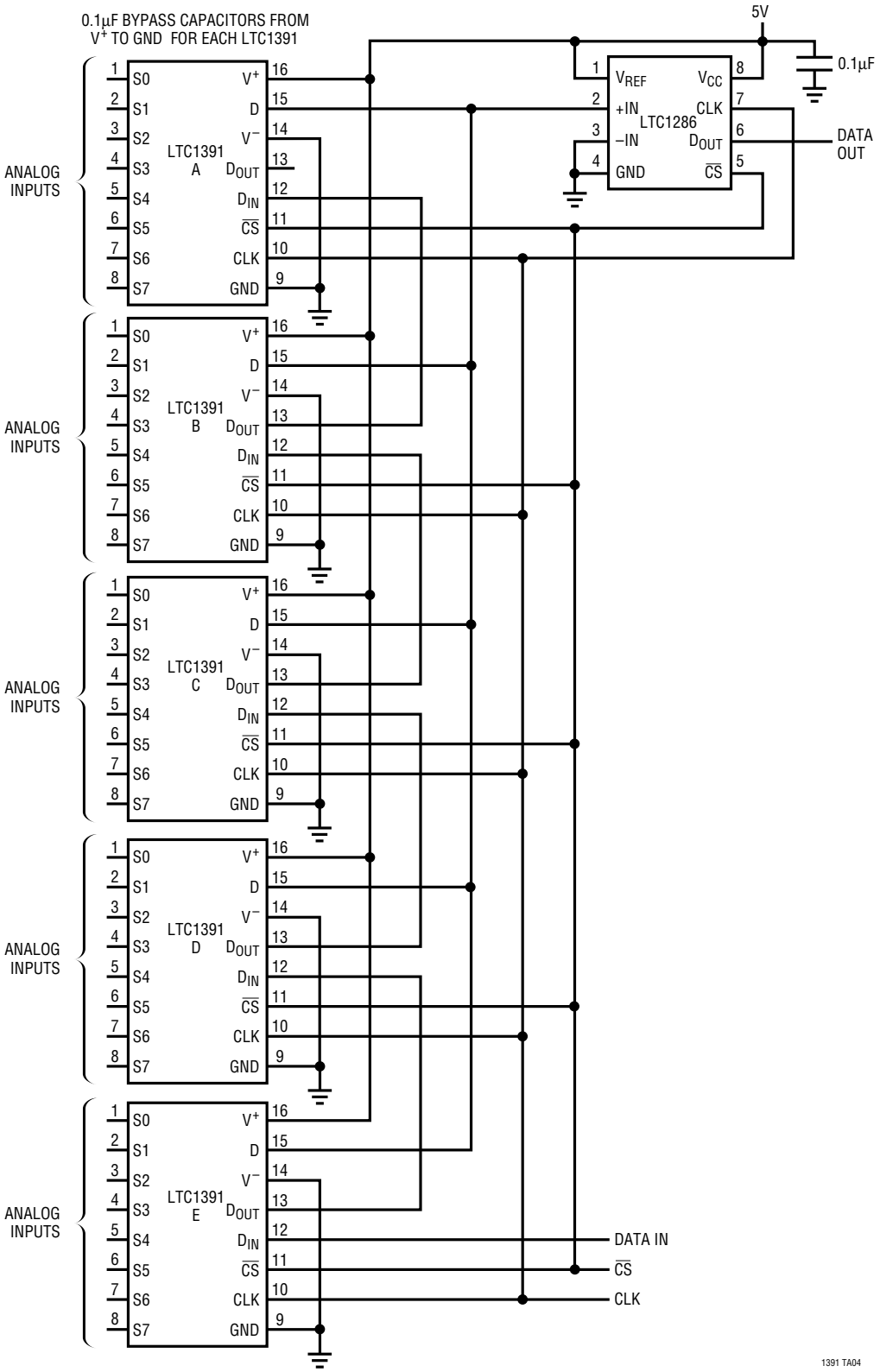


Figure 5. Daisy-Chaining Two LTC1391s for Expansion

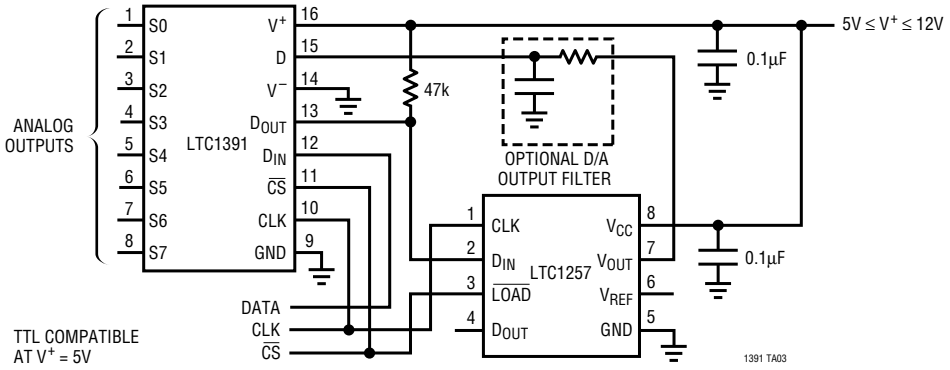
TYPICAL APPLICATIONS

Daisy-Chaining Five LTC1391s



TYPICAL APPLICATION

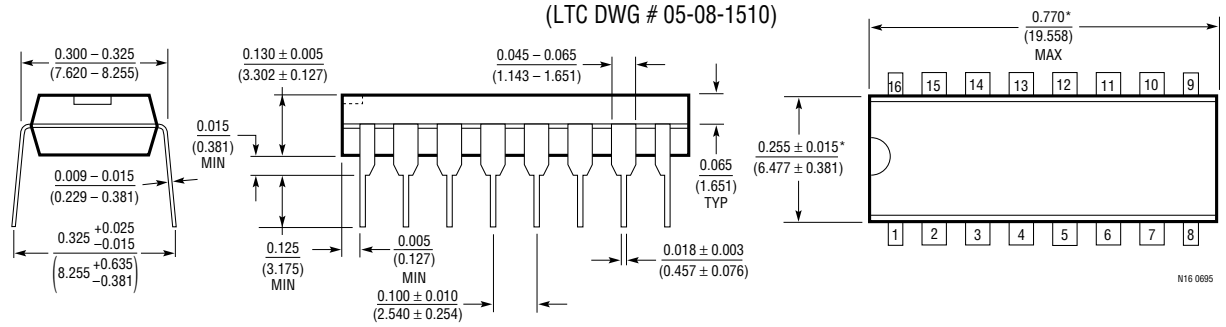
Interfacing LTC1391 with LTC1257 for Demultiplex Operation



PACKAGE DESCRIPTION

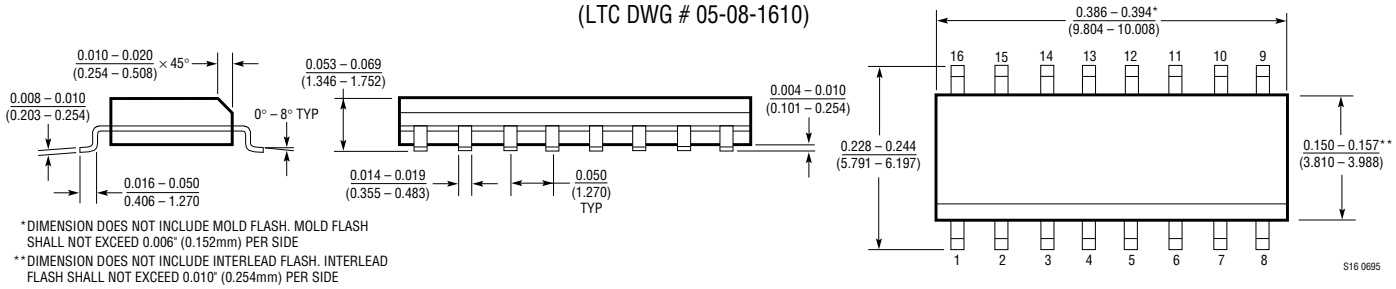
Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1285	3V 12-Bit ADC	Micropower, Auto Shutdown, SO-8 Package, SPI, QSPI + MICROWIRE™ Compatible
LTC1286	5V 12-Bit ADC	Micropower, Auto Shutdown, SO-8 Package, SPI, QSPI + MICROWIRE Compatible
LTC1390	Serial-Controlled 8-to-1 Analog Multiplexer	Low R_{ON}, Bidirectional Serial Interface, Low Power, 16-Pin SO
LTC1451	5V 12-Bit DAC	Complete V_{OUT} DAC, SO-8 Package, Daisy-Chainable, Low Power
LTC1452	5V and 3V 12-Bit DAC	Multiplying V_{OUT} DAC, SO-8 Package, Rail-to-Rail Output, Low Power
LTC1453	3V 12-Bit DAC	Complete V_{OUT} DAC, SO-8 Package, Daisy-Chainable, Low Power

MICROWIRE is a trademark of National Semiconductor.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977
LT/GP 0896 7K • PRINTED IN USA