LTC1068

Very Low Noise, High Accuracy, Quad Universal Filter Building Block

May 1996

FEATURES

- Four Identical 2nd Order Filters in an SSOP Package
- Center Frequency Error: ≤±0.3%
- Low Noise: ≤40μV_{RMS} per 2nd Order Section, Q ≤ 5
- High Dynamic Range: THD + Noise ≤0.01%
- Low DC Offsets: ≤10mV per 2nd Order Section
- Clock-to-Center Frequency Ratio: 100:1
- No Aliasing for Input Frequencies up to 200 × f_{CUTOFF}
- Maximum Center Frequency up to 56kHz (V_S = ±5V)
- Operates from ±1.57V to ±5V Power Supplies

APPLICATIONS

- High Performance Data Acquisition Filters
- Data Communication Filters
- Precision High Selectivity Bandpass Filters
- Precision Phase Matching Filters
- Audio Equalizer Filters
- Noise Cancellation Filters

DESCRIPTION

The LTC®1068 consists of four identical, low noise and high accuracy 2nd order switched-capacitor filter building blocks. Each building block, together with three to five resistors, can provide 2nd order filter functions like low-pass, bandpass, highpass and notch. High precision, high performance, quad 2nd order, dual 4th order or 8th order filters can be designed with an LTC1068. The center frequency of each 2nd order section is tuned by an external clock. The clock-to-center frequency ratio is internally set to 100:1 and can be modified by external resistors.

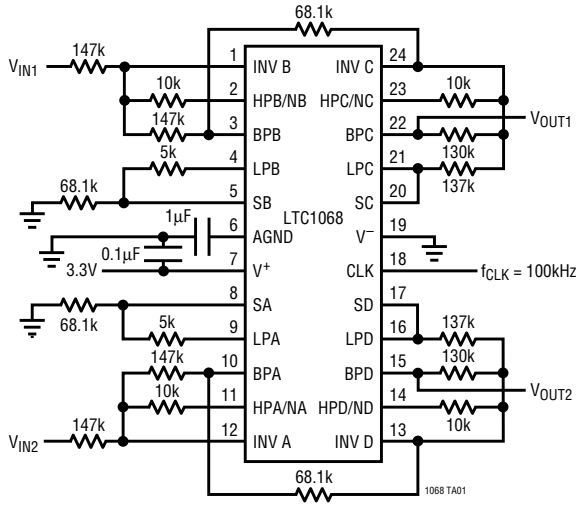
The sampling rate of the LTC1068 is twice the clock frequency. The maximum input frequency can approach twice the clock frequency before aliasing occurs.

Mask programmable versions of the LTC1068 with thin film resistors can be designed to realize customized active filters in monolithic form. Clock-to-center frequency ratios higher or lower than 100:1 can also be obtained. Please contact LTC marketing for details.

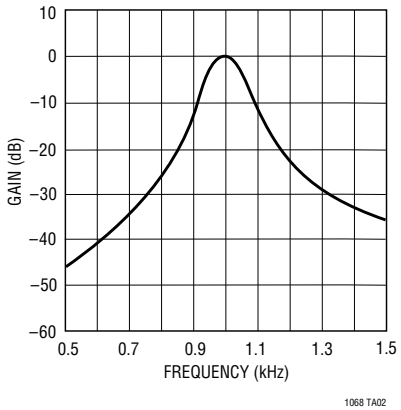
The LTC1068 is available in a 24-pin PDIP and 28-pin SSOP surface mounted package.

TYPICAL APPLICATION

Single 3.3V Supply Dual Butterworth Bandpass Filter



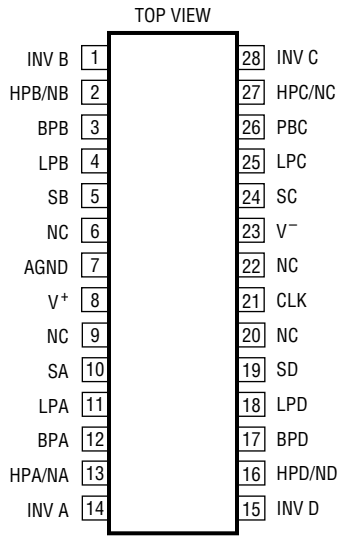
Frequency Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 12V
Power Dissipation 500mW
Operating Temperature Range
LTC1068C ..... 0°C to 70°C
LTC1068I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

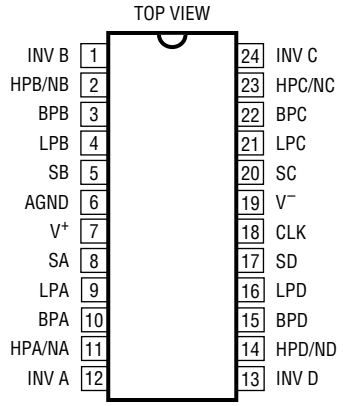


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 110°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1068CG
LTC1068IG



N PACKAGE
24-LEAD PDIP

T_{JMAX} = 110°C, θ_{JA} = 65°C/W

ORDER PART NUMBER

LTC1068CN
LTC1068IN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

(Internal Op Amps) V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			±1.57		±5.5	V
Voltage Swings	V_S = ±1.57V, R_L = 5k	●	±0.65	±0.9		V
	V_S = ±2.375V, R_L = 5k	●	±1.50	±1.7		V
	V_S = ±5V, R_L = 5k	●	±3.60	±4.3		V
Output Short-Circuit Current (Source/Sink)	V_S = ±2.375V			3		mA
	V_S = ±5V			3		mA
DC Open-Loop Gain	R_L = 5k			85		dB
GBW Product				6		MHz
Slew Rate				10		V/µs

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_O (Note 1)				0.1 to 50		kHz
Input Frequency Range				0 to 1		MHz
Clock-to-Center Frequency, f_{CLK}/f_O	$V_S = \pm 2.375V$, $f_{CLK} = 1MHz$, Mode 1, $f_O = 10kHz$, Q = 5, R1 = R3 = 49.9k, R2 = 10k	 ● 		100 ±0.3	100 ±0.8 100 ±0.9	% %
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$, Mode 1, $f_O = 10kHz$, Q = 5, R1 = R3 = 49.9k, R2 = 10K	 ● 		100 ±0.3	100 ±0.8 100 ±0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 2)	$V_S = \pm 2.375V$, $f_{CLK} = 1MHz$, Q = 5 $V_S = \pm 5V$, $f_{CLK} = 1MHz$, Q = 5	● ●		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 2)	$V_S = \pm 2.375V$, $f_{CLK} = 1MHz$, Q = 5 $V_S = \pm 5V$, $f_{CLK} = 1MHz$, Q = 5	● ●		±1 ±1	±3 ±3	% %
f_O Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 2) (See Table 1)	V_{OS1} (DC Offset of Input Inverter) V_{OS2} (DC Offset of First Integrator) V_{OS3} (DC Offset of Second Integrator)	● ● ●		0 –2 –5	±15 ±25 ±40	mV mV mV
Clock Feedthrough				0.1		mV_{RMS}
Max Clock Frequency	$V_S = \pm 5V$, $Q \leq 2.5$			5.6		MHz
Power Supply Current	$V_S = \pm 1.57V$ $V_S = \pm 2.375V$ $V_S = \pm 5V$			2.0 5.0 7.5	3.75 7.50 11.0	mA mA mA
	$V_S = \pm 1.57V$ $V_S = \pm 2.375V$ $V_S = \pm 5V$	● ● ●		2.5 5.5 8.0	4.5 8.5 12.0	mA mA mA

The ● denotes specificatons which apply over the full operating temperature range.

Note 1: See performance characteristics.

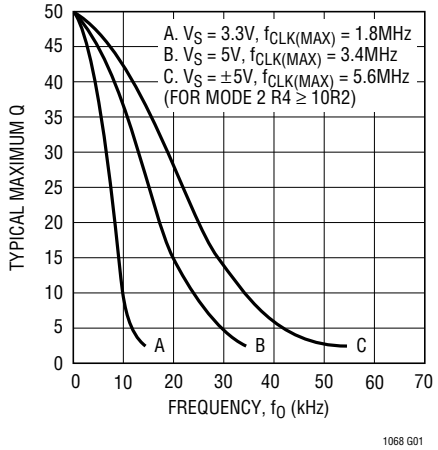
Note 2: Side D is guaranteed by design.

Table 1. Output DC Offsets One 2nd Order Section

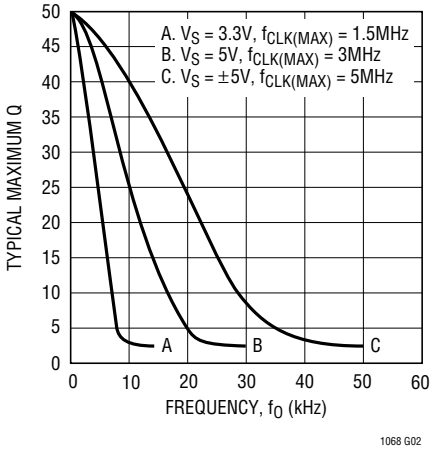
MODE	V_{OSN}	V_{OSBP}	V_{OSLP}
1	$V_{OS1}[(1/Q) + 1 + \|\|HOLP\|\|] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)X$ $[R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	$V_{OS2} = V_{OS(HP)}$	V_{OS3}	$V_{OS1}[1 + R4/R1 + R4/R2 + R4/R3] - V_{OS2}(R4/R2) - V_{OS3}(R4/R3)$

TYPICAL PERFORMANCE CHARACTERISTICS

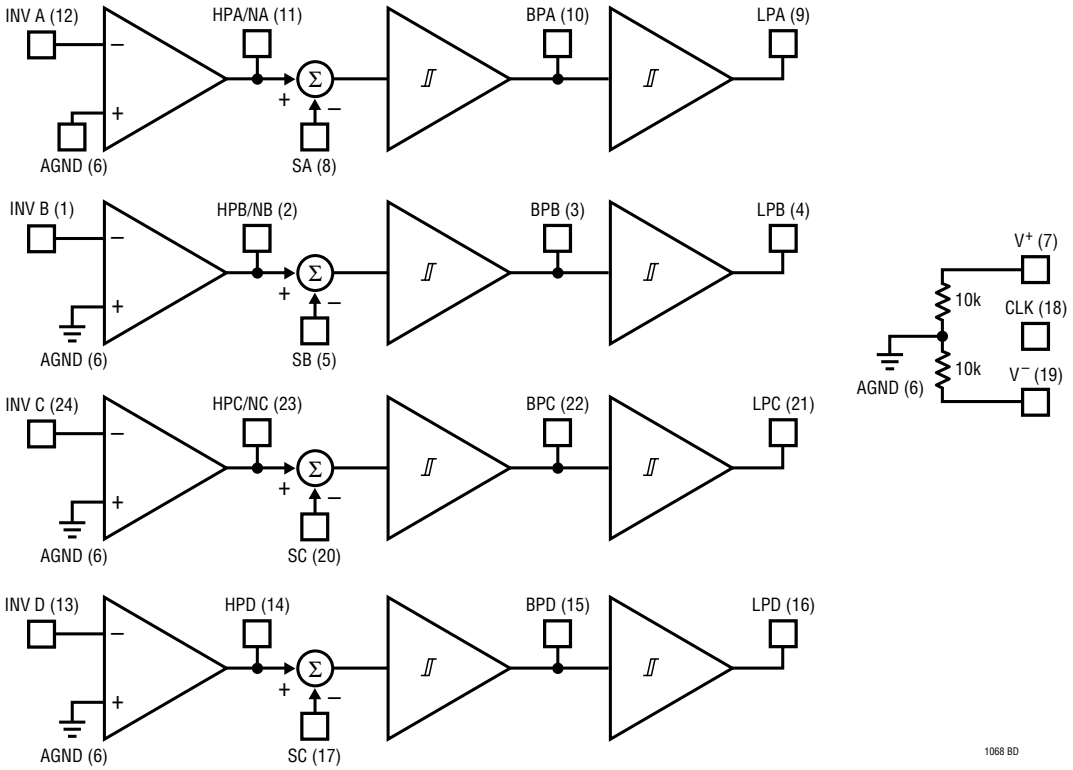
Maximum Q vs Frequency (Modes 1, 1B, 2)



Maximum Q vs Frequency (Modes 1, 1B, 2)



BLOCK DIAGRAM



RELATED PARTS

PART NUMBER	DESCRIPTON	COMMENTS
LTC1064	Universal Filter	50:1 and 100:1 Clock-to-f_0 Ratios
LTC1164	Low Power Universal Filter	50:1 and 100:1 Clock-to-f_0 Ratios
LTC1264	High Speed Universal Filter	25:1 Clock-to-f_0 Ratio

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