LTC1410

12-Bit, 1.25Msps Sampling A/D Converter with Shutdown

April 1995

FEATURES

- **Complete 1.25Msps ADC**
- **Power Dissipation: 160mW (Typ)**
- **Nap (7mW) and Sleep (10μW) Shutdown Modes**
- Operates with Internal 25ppm/°C Reference or External Reference
- True Differential Inputs Reject Common-Mode Noise
- 71dB S/(N + D) and 82dB THD at Nyquist
- 20MHz Full Power Bandwidth
- ±2.5V Bipolar Input Range
- Internal Synchronized Clock
- 28-Pin SO Wide Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

DESCRIPTION

The LTC®1410 is a 650ns, 1.25Msps, sampling 12-bit A/D converter which draws only 160mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold, a precision reference and a trimmed internal clock. Two digitally selectable power shutdown modes provide flexibility for low power systems.

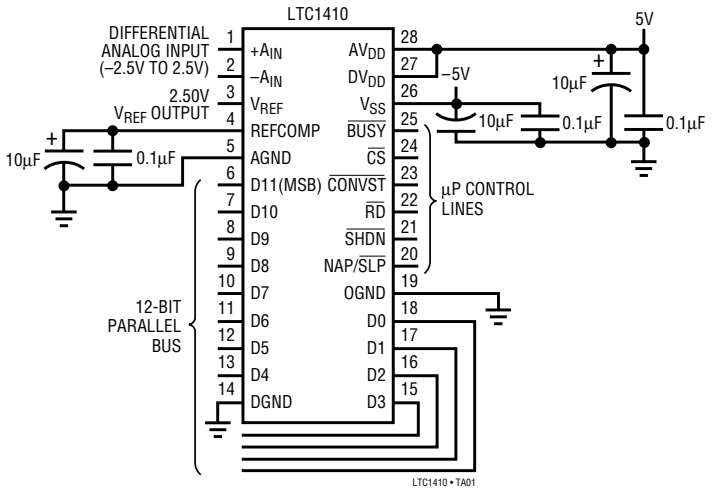
The LTC1410's full-scale input range is ±2.5V. Maximum DC specs include ±1LSB INL and ±1LSB DNL over temperature. Outstanding AC performance includes 71dB S/(N + D) and 82dB THD at the Nyquist input frequency of 625kHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common-mode rejection allows users to eliminate ground loops and common-mode noise by measuring signals differentially from the source.

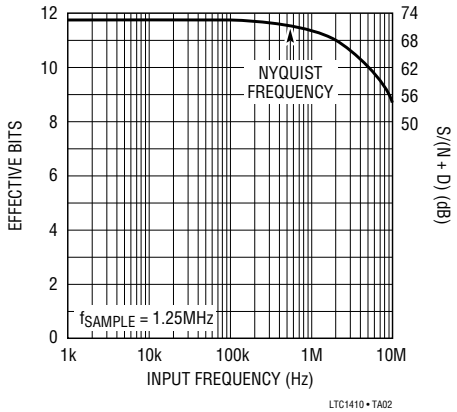
The internal clock is trimmed for 750ns maximum conversion time. The clock automatically synchronizes to each sample command. A separate convert start input and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Complete 1.25MHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

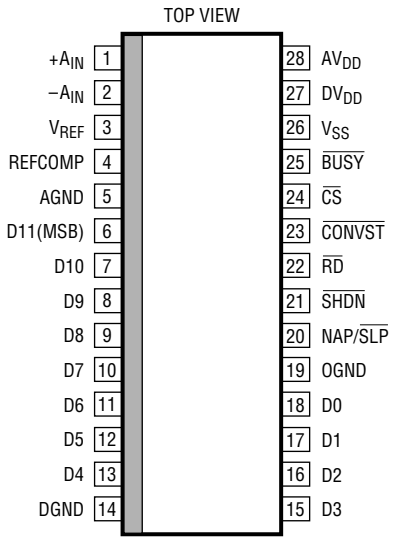


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = DV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... V_{SS} – 0.3V to 10V
Digital Output Voltage ..... – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1410C ..... 0°C to 70°C
LTC1410I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1410CSW LTC1410ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Offset Error	(Note 8)	 ●			±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±15		ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			17 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		50	100	ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Acquisition Delay Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common-Mode Rejection Ratio	–2.5V < V_{CM} < 2.5V, DC to 1MHz			60		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal (Note 12) 600kHz Input Signal (Note 12)	● ●	70 68			dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First Five Harmonics 600kHz Input Signal, First Five Harmonics	 ●		–85 –82	 –74	dB dB
	Peak Harmonic or Spurious Noise	600kHz Input Signal	●		–84	–74	dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–84		dB
	Full Power Bandwidth				20		MHz
	Full Linear Bandwidth	(S/(N + D) ≥ 68dB)			2.5		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	0.1V ≤ $\lvert I_{OUT} \rvert$ ≤ 0.1mA			2		kΩ
REFCOMP Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V I_O = –10µA I_O = –200µA	 ●	 4.0	 4.5 	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●	 	 0.05 0.10	 0.4	 V V
I_{OZ}	High-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 10, 11)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	●		12 1.5 1.0	16 2.3 	mA mA µA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SS}	Negative Supply Current Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	● 		20 10 1	30 200 	mA µA µA
P_{DISS}	Power Dissipation Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	 		160 7.5 0.01	230 12 	mW mW mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	1.25			MHz
$t_{SAMPLE(MIN)}$	Conversion and Acquisition Time		●			800	ns
t_{CONV}	Conversion Time		●			750	ns
t_{ACQ}	Acquisition Time		●			100	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	NAP/$\overline{SLP}\uparrow$ to $\overline{SHDN}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	Nap Mode (Note 10) Sleep Mode, $C_{REFCOMP}$ = 10µF	 		200 10		ns ms
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF	 ●		10	 50	ns ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$		 ●	20 15	35		ns ns
t_8	Delay Between Conversions	(Note 10)	●	50			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$		●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF C_L = 100pF 	 ● ●		15 20 	25 35 35 50	ns ns ns ns
t_{11}	Bus Relinquish Time Commercial Industrial		 ● ●		8 	20 25 30	ns ns ns ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	40			ns
t_{14}	Aperture Delay of Sample-and-Hold				–1.5		ns

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latch-up. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SAMPLE} = 1.25MHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended $+A_{IN}$ input with $-A_{IN}$ grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

TIMING CHARACTERISTICS

Note 11: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a critical point during the conversion it can create small errors. For best performance ensure that $\overline{\text{CONVST}}$ returns high either within 425ns after conversion start or after $\overline{\text{BUSY}}$ rises.

Note 12: Signal-to-noise ratio (SNR) is measured at 100kHz and distortion is measured at 600kHz. These results are used to calculate signal-to-noise plus distortion (SINAD).

PIN FUNCTIONS

$+A_{IN}$ (Pin 1): Analog Input, ±2.5V. The ADC converts the difference voltage between $+A_{IN}$ and $-A_{IN}$ with a differential range of ±2.5V.

$-A_{IN}$ (Pin 2): Negative Analog Input, ±2.5V.

V_{REF} (Pin 3): 2.500V Reference Output.

REFCOMP (Pin 4): 4.06V Reference Compensation Pin. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 5): Analog Ground.

D11 to D4 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground for Internal Logic.

D3 to D0 (Pins 15 to 18): Three-State Data Outputs.

OGND (Pin 19): Digital Ground for Output Drivers.

NAP/$\overline{\text{SLP}}$ (Pin 20): Power Shutdown Mode. Defines power down mode when $\overline{\text{SHDN}}$ goes low. High for quick wake-up Nap mode. Low for Sleep.

$\overline{\text{SHDN}}$ (Pin 21): Power Shutdown.

$\overline{\text{RD}}$ (Pin 22): Read Input. This enables the output drivers when $\overline{\text{CS}}$ is low.

$\overline{\text{CONVST}}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge when $\overline{\text{CS}}$ is low.

$\overline{\text{CS}}$ (Pin 24): The Chip Select input must be low for the ADC to recognize $\overline{\text{CONVST}}$ and $\overline{\text{RD}}$ inputs.

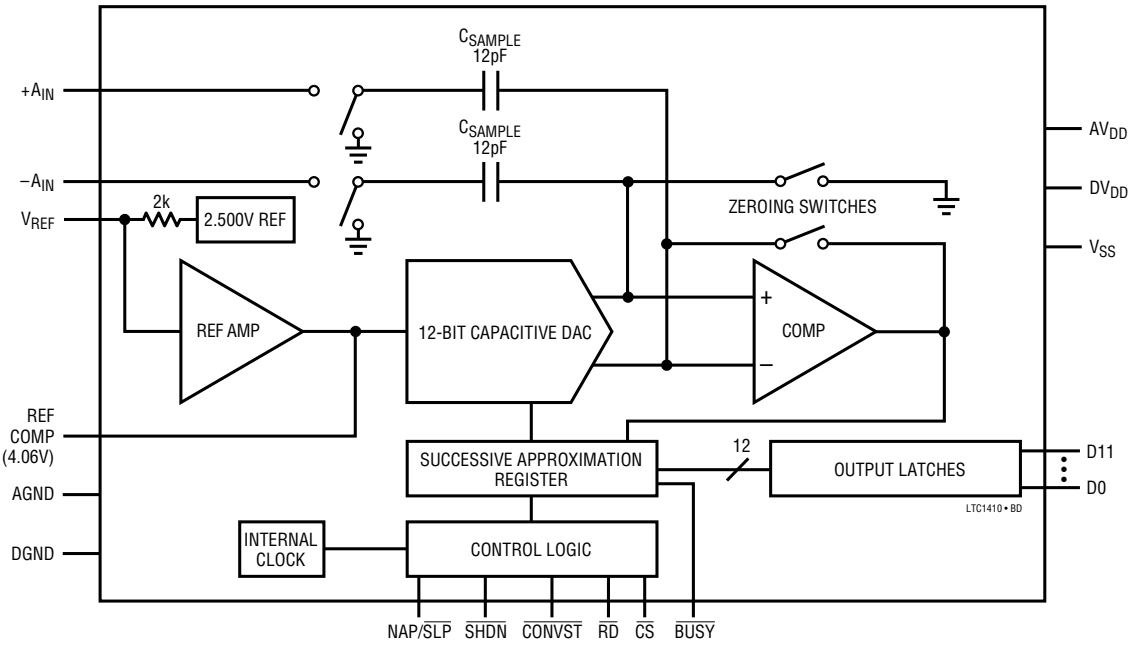
$\overline{\text{BUSY}}$ (Pin 25): The $\overline{\text{BUSY}}$ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{\text{BUSY}}$.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel 0.1µF ceramic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to pin 28.

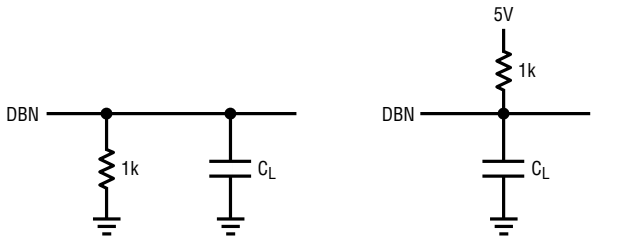
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

Load Circuits for Access Timing



A) Hi-Z to V_{OH} AND V_{OL} TO V_{OH} B) Hi-Z to V_{OL} AND V_{OH} TO V_{OL}

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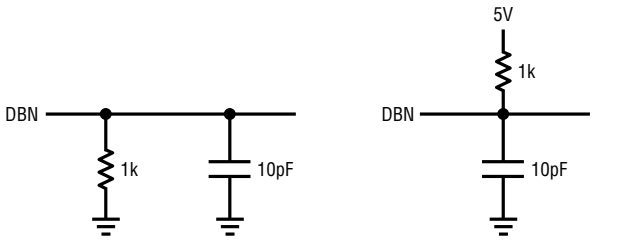
Load Circuits for Output Float Delay



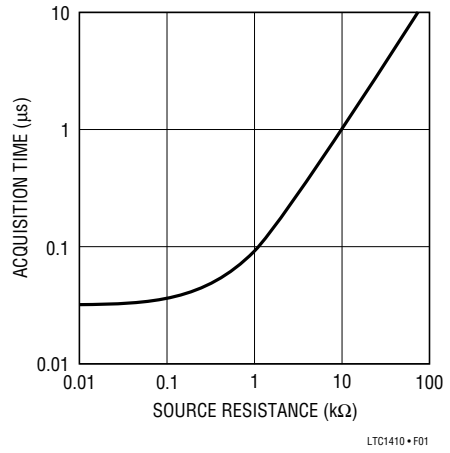
A) V_{OH} TO Hi-Z B) V_{OL} TO Hi-Z

LTC1410 • TC02

APPLICATIONS INFORMATION

Driving the Analog Input

The differential analog inputs of the LTC1410 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $-A_{IN}$ input is grounded). The $+A_{IN}$ and $-A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common-mode to both inputs will be reduced by the 60dB common-mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1410 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 1). For minimum acquisition time, with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 100ns for full throughput rate).



LTC1410 • F01

Figure 1 Acquisition Time vs Source Resistance

Choosing an input amplifier is easy if a few requirements are taken into consideration, First, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a closed-loop bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's inputs include the LT®1360, LT1220, LT1223 and LT1224 op amps.

The noise and the distortion of the input amplifier must also be considered since they will add to the LTC1410 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise that is present at the analog inputs will be summed over this entire bandwidth. Noisy input signals should be filtered prior to the analog inputs to minimize noise. A simple one-pole RC filter is usually sufficient. For example, a 1000pF capacitor from $+A_{IN}$ to ground and a 100Ω source resistor will limit the input bandwidth to 1.6MHz. Simple RC filters work well for AC applications, but they will limit the transient response. Raising the bandwidth of the RC filter will improve the transient response. For full speed operation, fast settling, low noise amplifiers should be chosen.

APPLICATIONS INFORMATION

Internal Reference

The LTC1410 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.50V. It is connected internally to a reference amplifier and is available at pin 3. A 2k resistor is in series with the output so that it can be easily overdriven in applications where an external reference is required. The reference buffer compensation pin, REFCOMP (pin 4), must be bypassed with a capacitor to ground. The reference is stable with capacitors of 1µF or greater. For the best noise performance, Linear Technology recommends 10µF in parallel with 0.1µF ceramic (see Figure 2).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The reference should be kept in the range of 2.25V to 2.75V for specified linearity.

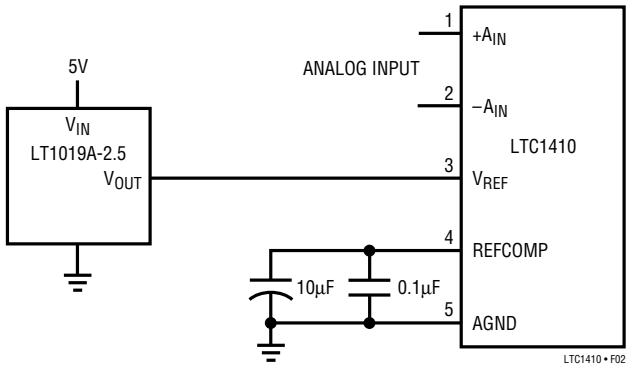


Figure 2. Using the LT1019-2.5 as an External Reference

Full-Scale and Offset Adjustment

Figure 3 shows the ideal input/output characteristics for the LTC1410. The code transitions occur midway between successive integer LSB values (i.e., –FS/2 + 0.5LSB, –FS/2 + 1.5LSB, –FS/2 + 2.5LSB,... FS/2 – 1.5LSB, FS/2 – 2.5LSB. The output is two's complement binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 4 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the $–A_{IN}$ input. For zero offset error apply –0.61mV (i.e., –0.5LSB at $+A_{IN}$ and adjust the voltage at the $–A_{IN}$ input until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.49817V (FS/2 – 1.5LSBs) is applied to A_{IN} and R2 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

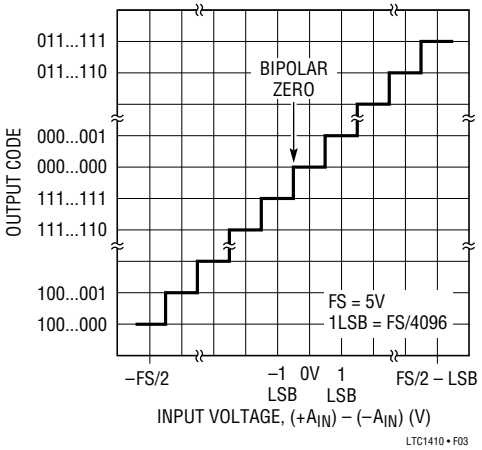


Figure 3. LTC1410 Transfer Characteristics

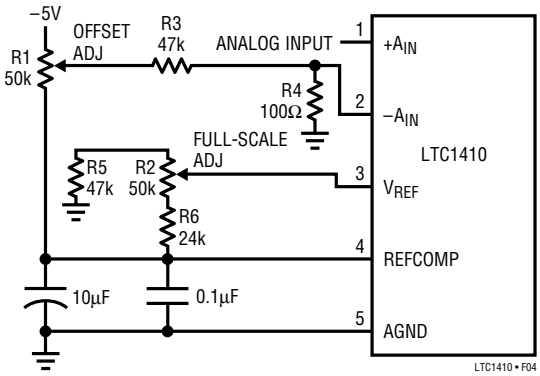


Figure 4. Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1410, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

APPLICATIONS INFORMATION

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD}, V_{SS} and REFCOMP pins as shown in the Typical Application on the first page of this data sheet. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1410 has differential inputs to minimize noise coupling. Common-mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the LTC1410 will hold and convert the voltage difference between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (pin 1) and $-A_{IN}$ (pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side by side to equalize coupling.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at pin 5 (AGND) or as close as possible to the ADC. Pin 14 and pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. No other digital ground should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.65µs and a maximum conversion time over the full operating temperature range of 0.75µs. No external adjustments are required. The guaranteed maximum acquisition time is 100ns. In addition, throughput performance is also guaranteed at 800ns so that 1.25Msps is assured.

Power Shutdown

The LTC1410 provides two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from NAP to active is 200ns. Follow the setup time shown in Figure 5a to avoid inadvertently invoking sleep mode. In Sleep mode all bias currents are shut down and only leakage current remains, about 1µA. Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle to 0.01% for full 12-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (pin 4). The wake-up time is 10ms with the recommended 10µF capacitor. (See Figure 5b).

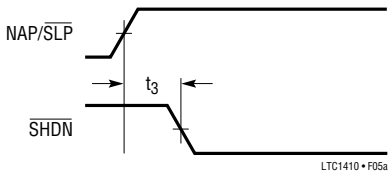


Figure 5a. NAP/$\overline{SLP}$ to $\overline{SHDN}$ Timing to Ensure Nap Mode

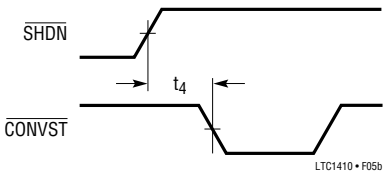


Figure 5b. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

APPLICATIONS INFORMATION

Shutdown is controlled by pin 21 (SHDN), the ADC is in shutdown when it is low. The shutdown mode is selected with pin 20 (NAP/SLP); high selects NAP.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. (See Figure 6.) A falling edge applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

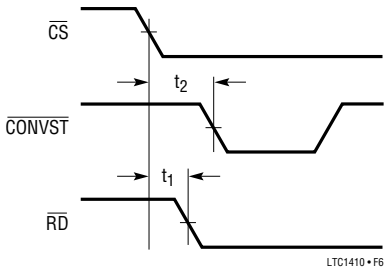


Figure 6. $\overline{CS}$ to $\overline{CONVST}$ Setup Timing

Figures 7 through 11 show several different modes of operation. In modes 1a and 1b (Figures 7 and 8) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 9) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 10 and 11) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$) starting the conversion. $\overline{BUSY}$ goes low forcing the processor into a wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor, and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

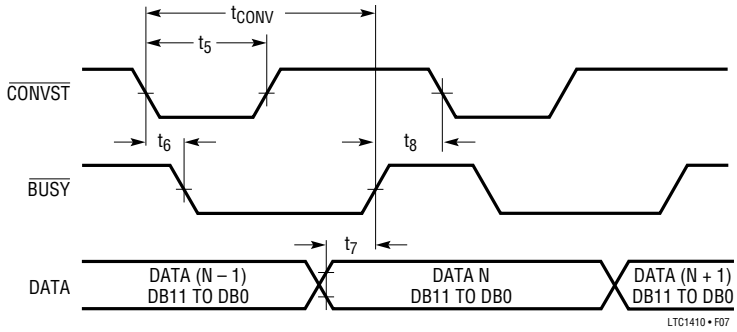


Figure 7. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⊓⊓⊓)

APPLICATIONS INFORMATION

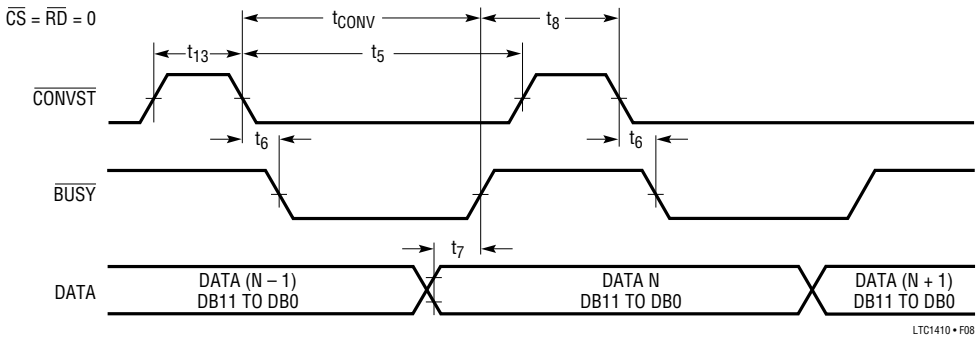


Figure 8. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⎍⎍⎍)

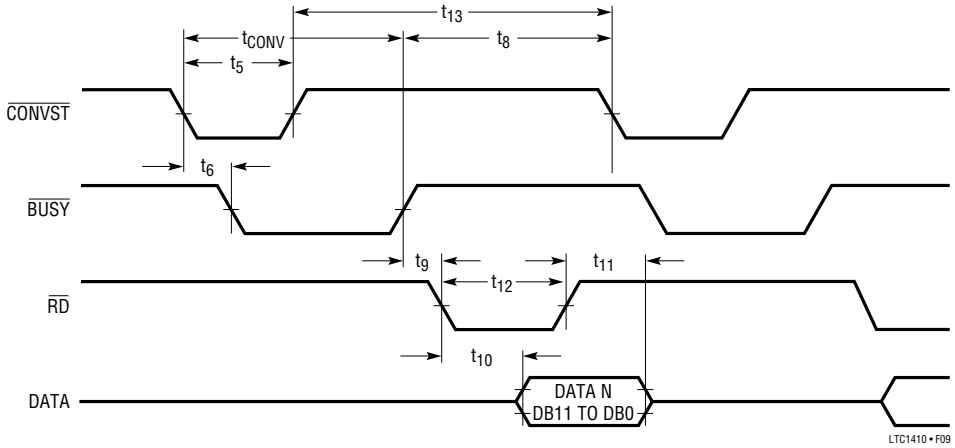


Figure 9. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

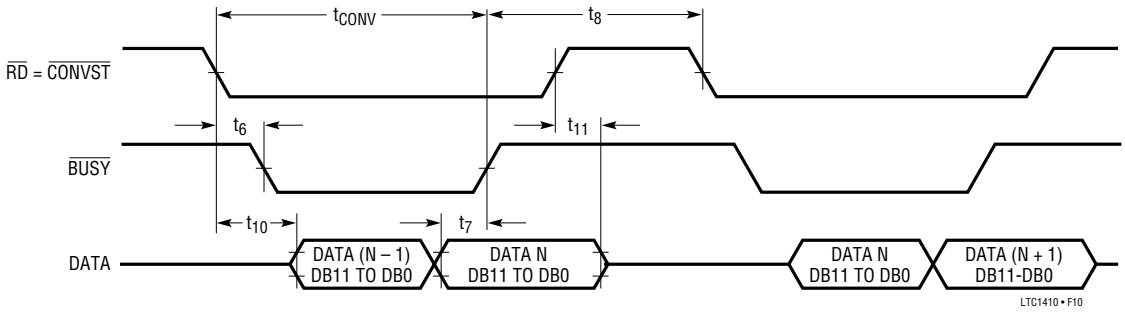


Figure 10. Slow Memory Mode Timing

APPLICATIONS INFORMATION

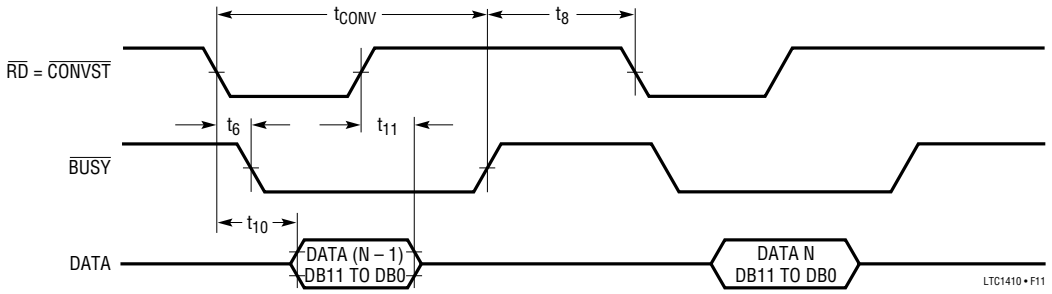


Figure 11. ROM Mode Timing

RELATED PRODUCTS

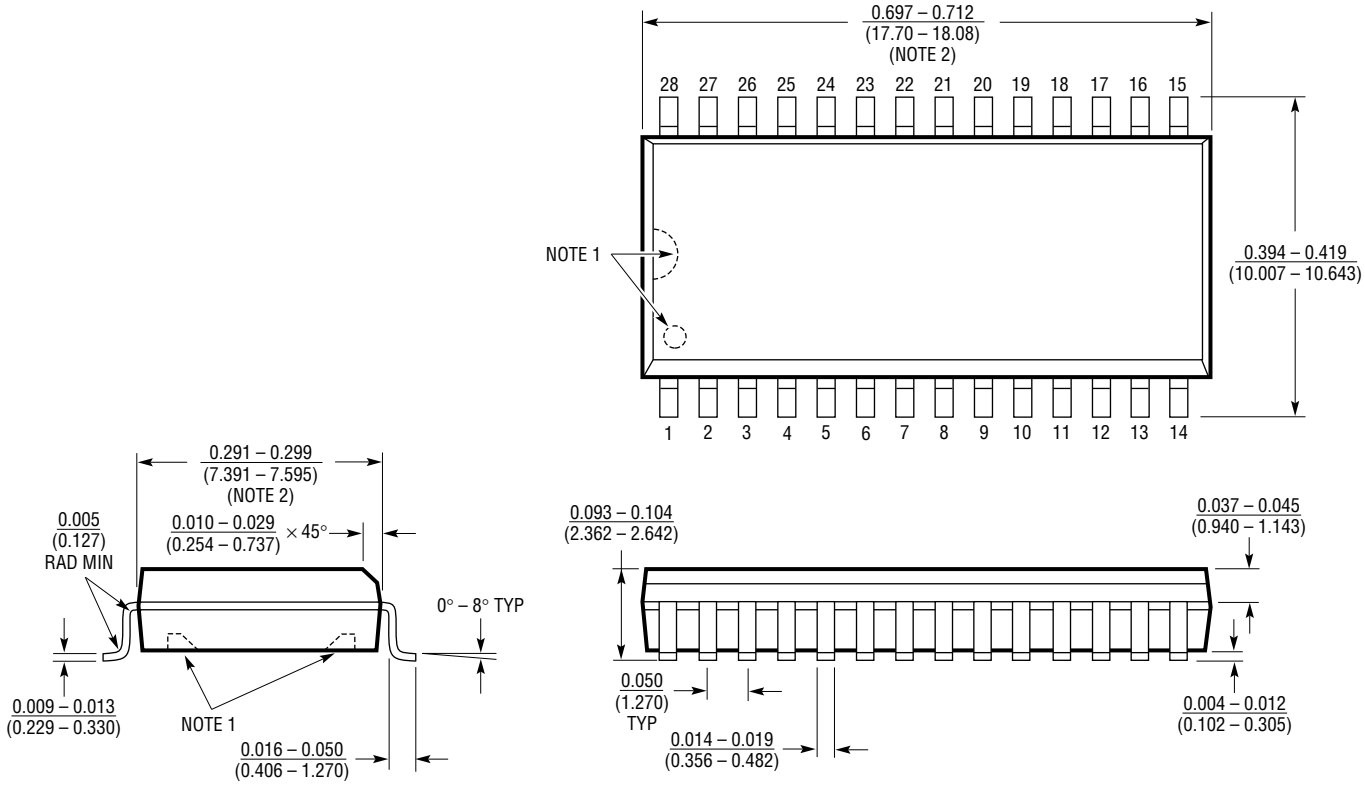
12-Bit Sampling A/D Converters

PART NUMBER	SAMPLE RATE	DESCRIPTION	COMMENTS
LTC1273/75/76	300ksps	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Nyquist	Lower Power and Cost Effective for $f_{SAMPLE} \leq 300$ksps
LTC1274/77	100ksps	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	Lowest Power for $f_{SAMPLE} \leq 100$ksps
LTC1278/79	500/600ksps	High Speed Sampling 12-Bit ADCs with Shutdown	Cost Effective 12-Bit ADCs — Best for 2-Pair HDSL
LTC1282	140ksps	Complete 3V 12-Bit ADCs with 12mW Power Dissipation	Fully Specified for 3V-Powered Applications

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
28-Lead Plastic SOL



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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