LTC1400

Complete SO-8, 12-Bit, 400ksps ADC with Shutdown

May 1996

FEATURES

- **Complete 12-Bit ADC in SO-8**
- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 400ksps**
- Power Dissipation: 75mW (Typ)
- 70dB S/(N + D) and 74dB THD at Nyquist
- No Missing Codes over Temperature
- NAP Mode with Instant Wake-Up: 6mW
- SLEEP Mode: 30µW
- High Impendance Analog Input
- Input Range (1mV/LSB): 0V to 4.096 or ±2.048V
- Internal Reference Can Be Overdriven Externally
- 3-Wire Interface to DSPs and Processors

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Digital Radio
- Spectrum Analysis
- Low Power and Battery-Operated Systems
- Handheld or Portable Instruments

DESCRIPTION

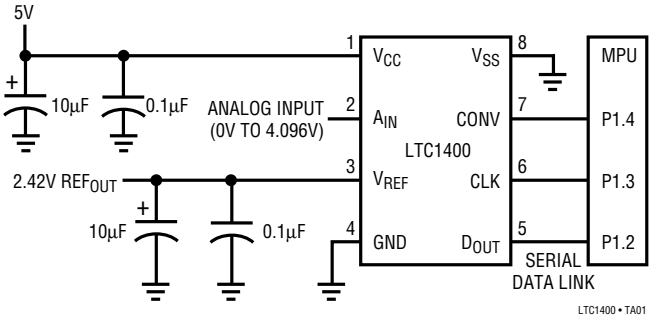
The LTC®1400 is a complete 400ksps, 12-bit A/D converter which draws only 75mW from a 5V or ± 5V supplies. This easy-to-use device comes complete with a 200ns sample-and-hold and a precision reference. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The LTC1400 is capable of going into two power saving modes: NAP and SLEEP. In NAP mode, it consumes only 6mW of power and can wake up and convert immediately. In the SLEEP mode, it consumes 30µW of power typically. Upon power-up from SLEEP mode, a reference ready (REFRDY) signal is available in the serial data word to indicate that the reference has settled and the chip is ready to convert.

The LTC1400 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL, ±1LSB DNL and 45ppm/°C drift over temperature. Guaranteed AC performance includes 70dB S/(N + D) and 76dB THD at an input frequency of 100kHz, over temperature.

The 3-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers and DSPs.

TYPICAL APPLICATION

Single 5V Supply, 400kHz, 12-Bit Sampling A/D Converter



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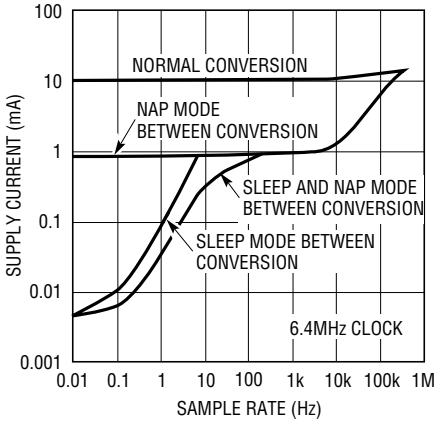
Power Consumption vs Sample Rate



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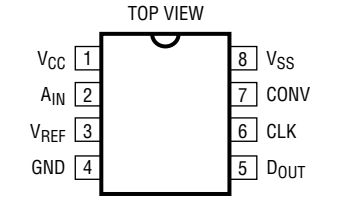
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Negative Supply Voltage (V_{SS}) ..... –6V to GND
Total Supply Voltage (V_{CC} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... –0.3V to (V_{CC} + 0.3V)
  Bipolar Operation ..... (V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Digital Input Voltage (Note 4)
  Unipolar Operation ..... –0.3V to 12V
  Bipolar Operation ..... (V_{SS} – 0.3V) to 12V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to (V_{CC} + 0.3V)
  Bipolar Operation ..... (V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 500mW
Operation Temperature Range
  LTC1400C ..... 0°C to 70°C
  LTC1400I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S8)

ORDER PART NUMBER
LTC1400CN8 LTC1400CS8 LTC1400IN8 LTC1400IS8
S8 PART MARKING
1400 1400I

Consult factory for Military grade parts.

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage (Note 6)	Unipolar Bipolar		4.75 4.75		5.25 5.25	V V
V_{SS}	Negative Supply Voltage (Note 6)	Bipolar Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 400ksps NAP Mode SLEEP Mode	● ● ●		15 1.0 5.0	30 3.0 20.0	mA mA µA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 400ksps, V_{SS} = –5V NAP Mode SLEEP Mode	● ● ●		0.3 0.2 1	0.6 0.5 5	mA mA µA
P_D	Power Dissipation	f_{SAMPLE} = 400ksps NAP Mode SLEEP Mode	● ● ●		75 6 30	160 20 125	mW mW µW

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 7)	4.75V ≤ V_{CC} ≤ 5.25V (Unipolar) 4.75V ≤ V_{CC} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –2.45V (Bipolar)	● ●		0 to 4.096 ±2.048		V V
I_{IN}	Analog Input Leakage Current	During Conversions (Hold Mode)	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			45 5		pF pF

CONVERTER CHARACTERISTICS With internal reference (Notes 5, 8)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 9)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Offset Error	(Note 10)	 ●			±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal Commercial Industrial	● ●	70 69	72		dB dB
		200kHz Input Signal			70		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	100kHz Input Signal 200kHz Input Signal	●		–80 –74	–76	dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal 200kHz Input Signal	●		–84 –74	–76	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 99.3kHz, f_{IN2} = 102.4kHz f_{IN1} = 199.37kHz, f_{IN2} = 202.4kHz			–82 –70		dB dB
	Full Power Bandwidth				4		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				350		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{CC} ≤ 5.25V –5.25V ≤ V_{SS} ≤ 0V			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	0 ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			2		LSB/mA

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10µA V_{CC} = 4.75V, I_O = –200µA	 ●	 4.0	4.7		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.25V, I_O = 160µA V_{CC} = 5.25V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{CC}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT} (Note 7)		●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			10		mA

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	400			kHz
t_{CONV}	Minimum Conversion Time		●			2.1	µs
t_{ACQ}	Acquisition Time (Unipolar Mode) (Bipolar Mode V_{SS} = –5V)	(Note 7)	● ●		230 200	300 270	ns ns
t_{CLK}	CLK Frequency	(Note 6)	●	0.1		6.4	MHz
$t_{WK(NAP)}$	Time to Wake Up from NAP Mode				350		ns
t_1	Minimum CLK Pulse Width to Return to Active Mode		●		20	50	ns
t_2	Minimum CONV↑ to CLK↑ Setup Time		●		40	80	ns
t_3	Maximum CONV↑ After Leading CLK↑		●		–20	0	ns
t_4	Minimum CONV Pulse Width	(Note 11)	●		20	50	ns
t_5	Time from CLK↑ to Sample Mode		●		80		ns
t_6	Aperture Delay of Sample-and-Hold (Note 7)	Jitter < 50ps	●		45	65	ns
t_7	Minimum Delay Between Conversion (Unipolar Mode) (Bipolar Mode V_{SS} = –5V)		● ●		265 235	385 355	ns ns
t_8	Delay Time, CLK↑ to D_{OUT} Valid	C_{LOAD} = 20pF	●		40	80	ns
t_9	Delay Time, CLK↑ to D_{OUT} Hi-Z	C_{LOAD} = 20pF	●		40	80	ns
t_{10}	Time from Previous Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	14	25		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{CC}, they will be clamped by internal diodes. This product can handle input currents greater than 40mA below V_{SS} (ground for unipolar mode) or above V_{CC} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 40mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{CC}.

Note 5: V_{CC} = 5V, f_{SAMPLE} = 400kHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Recommended operating conditions.

Note 7: Guaranteed by design, not subject to test.

Note 8: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

Note 9: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 10: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 11: The rising edge of CONV starts a conversion. If CONV returns low at a bit decision point during the conversion, it can create small errors. For best performance ensure that CONV returns low either within 120ns after conversion starts (i.e., before the first bit decision) or after the 14 clock cycle. (Figure 9 Timing Diagram).

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply, 5V. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

A_{IN} (Pin 2): Analog Input. 0V to 4.096V (Unipolar), ±2.048V (Bipolar).

V_{REF} (Pin 3): 2.42V Reference Output. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 4): Ground. GND should be tied directly to an analog ground plane.

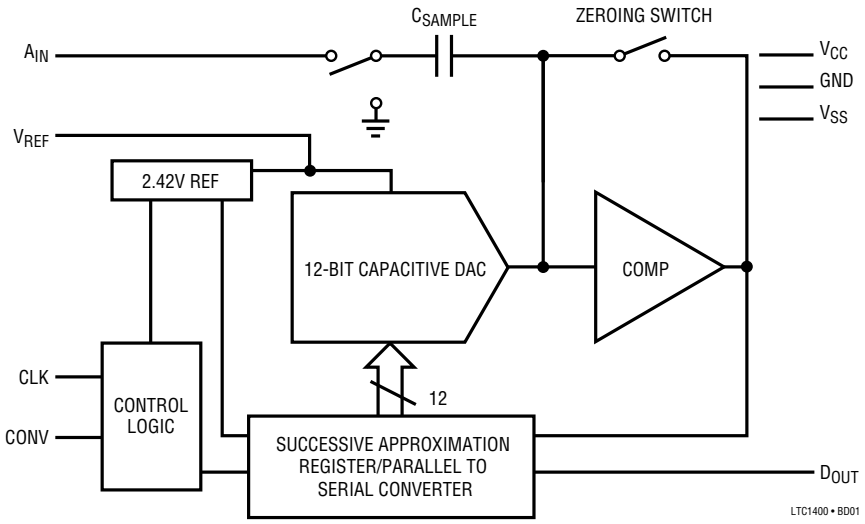
D_{OUT} (Pin 5): The A/D conversion result is shifted out from this pin.

CLK (Pin 6): Clock. This clock synchronizes the serial data transfer. A minimum CLK pulse of 50ns will cause the ADC to wake up from NAP or SLEEP mode.

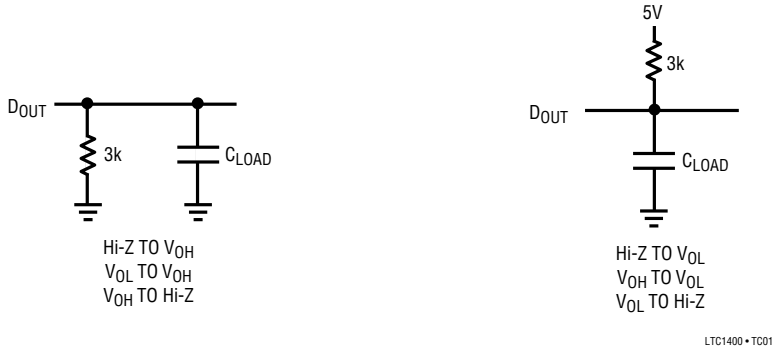
CONV (Pin 7): Conversion Start Signal. This active high signal starts a conversion on its rising edge. Keeping CLK low and pulsing CONV two/four times will put the ADC into NAP/SLEEP mode.

V_{SS} (Pin 8): Negative Supply. –5V for bipolar operation. Bypass to GND with 0.1µF ceramic. V_{SS} should short to GND for unipolar operation.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS



APPLICATIONS INFORMATION

Conversion Details

The LTC1400 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output based on a precision internal reference. The control logic provides easy interface to microprocessors and DSPs through 3-wire connections.

Start of conversion is controlled by the CONV input. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquired phase and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 200ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN}, are output through the serial pin D_{OUT}.

Driving the Analog Input

The analog input of the LTC1400 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion, the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 200ns to small current transients will allow maximum speed operation. If a slower op amp is used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include LT®1006, LT1007, LT1220, LT1223 and LT1224 op amps.

Internal Reference

The LTC1400 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at Pin 3 to provide up to 1mA of current to an external load. For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic). The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should not be driven to more than 5V. Figure 2 shows an LT1006 op amp driving the reference

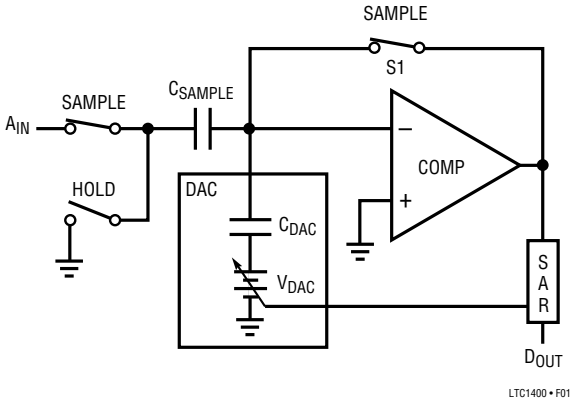


Figure 1. A_{IN} Input

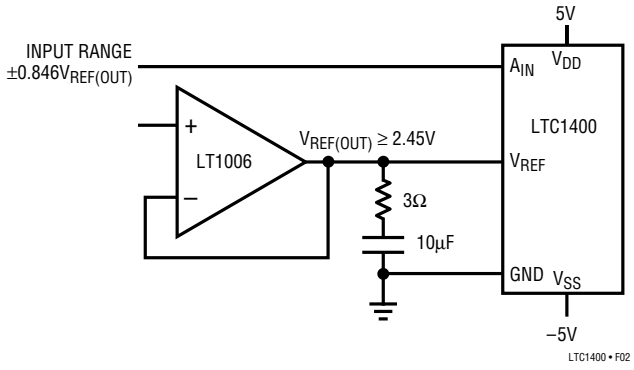


Figure 2. Driving the V_{REF} with the LT1006 Op Amp

APPLICATIONS INFORMATION

pin. Figure 3 shows a typical reference, the LT1019A-5 connected to the LTC1400. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-5) and a ±4.231V full scale.

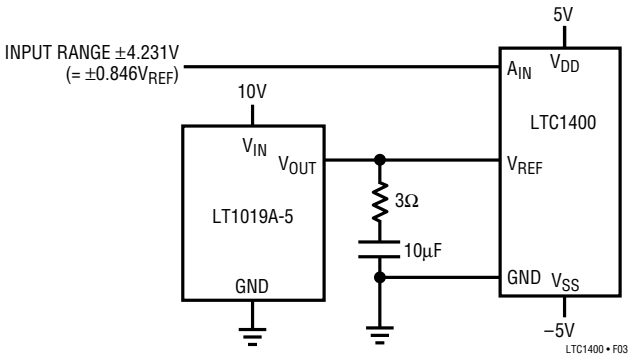


Figure 3. Supplying a 5V Reference Voltage to the LTC1400 with the LT1019A-5

UNIPOLAR / BIPOLAR OPERATION AND ADJUSTMENT

Figure 4 shows the ideal input/output characteristics for LTC1400. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, … FS – 1.5LSB). The output code is naturally binary with 1LSB = 4.096/4096 = 1mV. Figure 5 shows the input/output transfer characteristics for the bipolar mode in two's complement format.

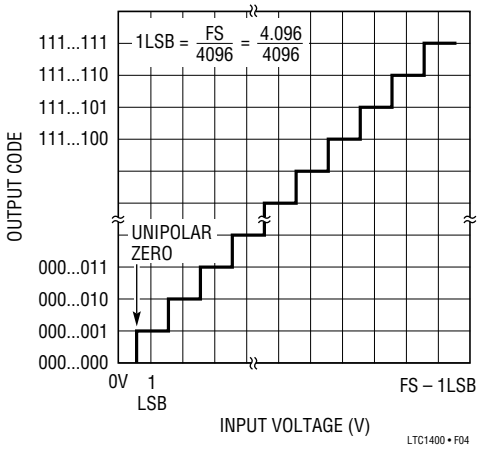


Figure 4. LTC1400 Unipolar Transfer Characteristics

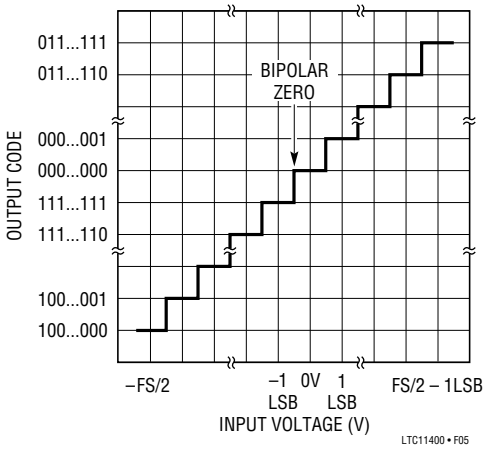


Figure 5. LTC1400 Bipolar Transfer Characteristics

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 6a shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving A_{IN} (i.e., A1 in Figure 6b). For zero offset error, apply 0.5mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1400 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 4.0945V (FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1400 output code flickers between 1111 1111 1110 and 1111 1111 1111.

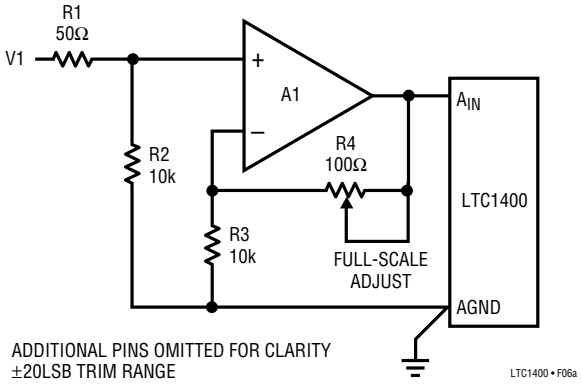


Figure 6a. Full-Scale Adjust Circuit

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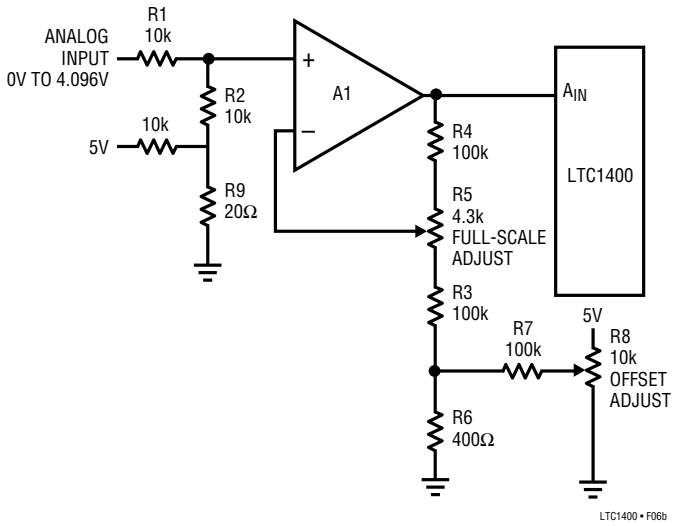


Figure 6b. LTC1400 Offset and Full-Scale Adjust Circuit

Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1400 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.5mV (–0.5LSB) to the input in Figure 6c and adjusting the op amp until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

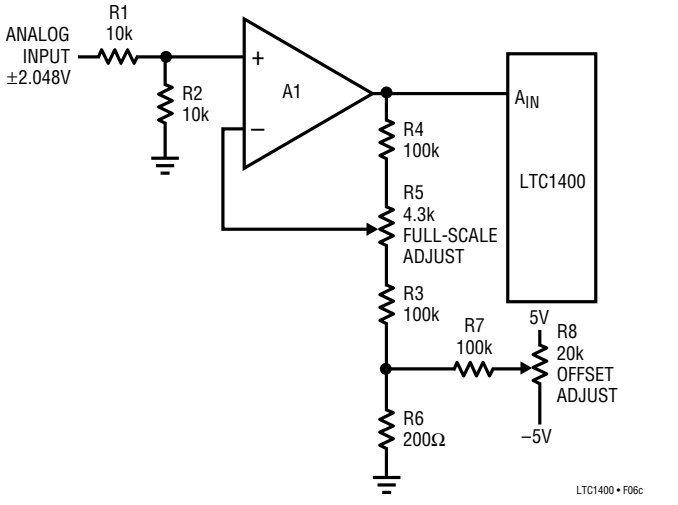


Figure 6c. LTC1400 Bipolar Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND BYPASSING

Wire-wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1400, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by GND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{CC} and V_{REF} pins as shown in the Typical Application on the first page of this data sheet. For the bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from GND (Pin 4) should be kept as short as possible to minimize noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible.

Figure 7 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC1400 GND pin. The ground return from the LTC1400

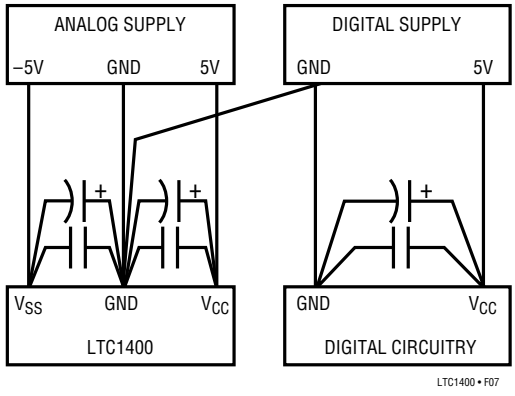


Figure 7. Power Supply Connection

APPLICATIONS INFORMATION

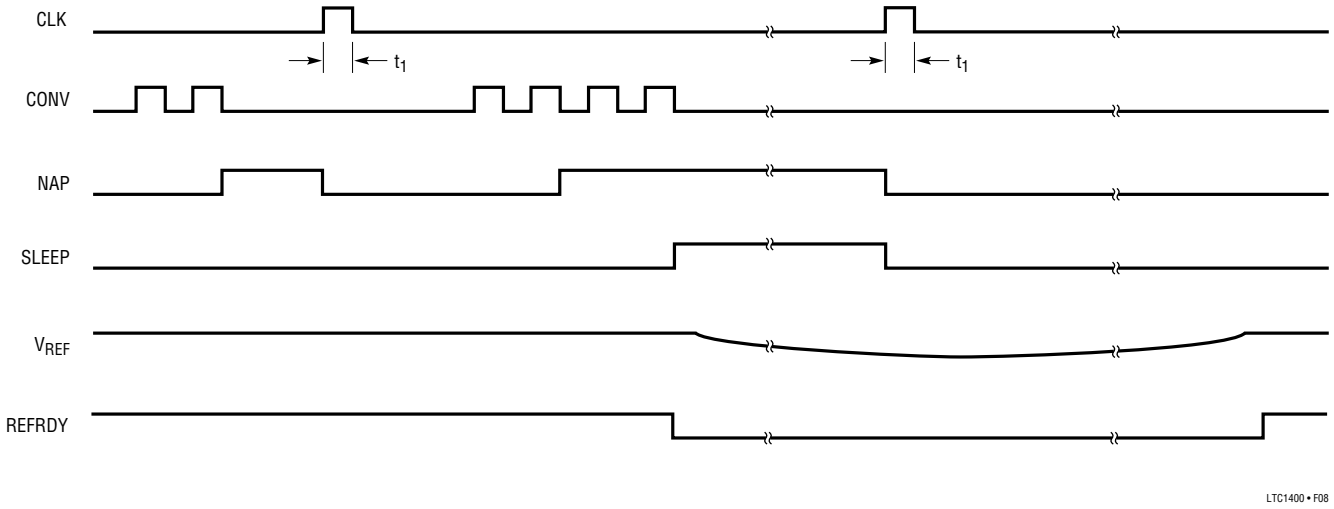
Pin 4 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

Power-Down Mode

Upon power-up, the LTC1400 is initialized to the active state and is ready for conversion. However, the chip can be easily placed into the NAP or SLEEP mode by exercising the right combination of CLK and CONV signal. In the NAP mode all power is off except the internal reference, which is still active and provides 2.42V output voltage to the other circuitry. In this mode, the ADC draws only 6mW of power instead of 75mW (for minimum power, the logic inputs must be within 500mV of the supply rails). The wake-up time from the NAP mode to the active mode is 350ns. In the SLEEP mode, the power consumption is reduced to minimum by cutting off the supply to all internal circuitry including the reference. Figure 8 shows the ways to power down LTC1400. The chip can enter the NAP mode by keeping the CLK signal low and pulsing the CONV signal twice. For SLEEP mode operation, CONV signal should be activated four times while CLK is kept low.

The LTC1400 can be returned to active mode easily. This can be achieved by pulsing the CLK signal. During the transition from SLEEP mode to active mode, the V_{REF} voltage ramp-up time is a function of the loading conditions. With a 10µF bypass capacitor, the wake-up time from SLEEP mode is typically 4ms. A REFRDY signal will be activated once the reference has settled and is ready for A/D conversion. This REFRDY bit is output to the D_{OUT} pin before the rest of the A/D converted code.



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS. REFRDY APPEARS AS A BIT IN THE D_{OUT} WORD.

Figure 8. NAP Mode and SLEEP Mode Waveforms

APPLICATIONS INFORMATION

DIGITAL INTERFACE

The digital interface requires only three digital lines. CLK and CONV are both inputs, and the D_{OUT} output provides the conversion result in serial form.

Figure 9 shows the digital timing diagram of the LTC1400 during the A/D conversion. The CONV rising edge starts the conversion. Once initiated, it can not be restarted until the conversion is completed. If the time from CONV signal to CLK rising edge is less than t_2, the digital output will be delayed by one clock cycle.

The digital output data is updated on the rising edge of the CLK line. D_{OUT} data should be captured by the receiving system on the rising CLK edge. Data remains valid for a minimum time of t_{10} after the rising CLK edge to allow capture to occur.

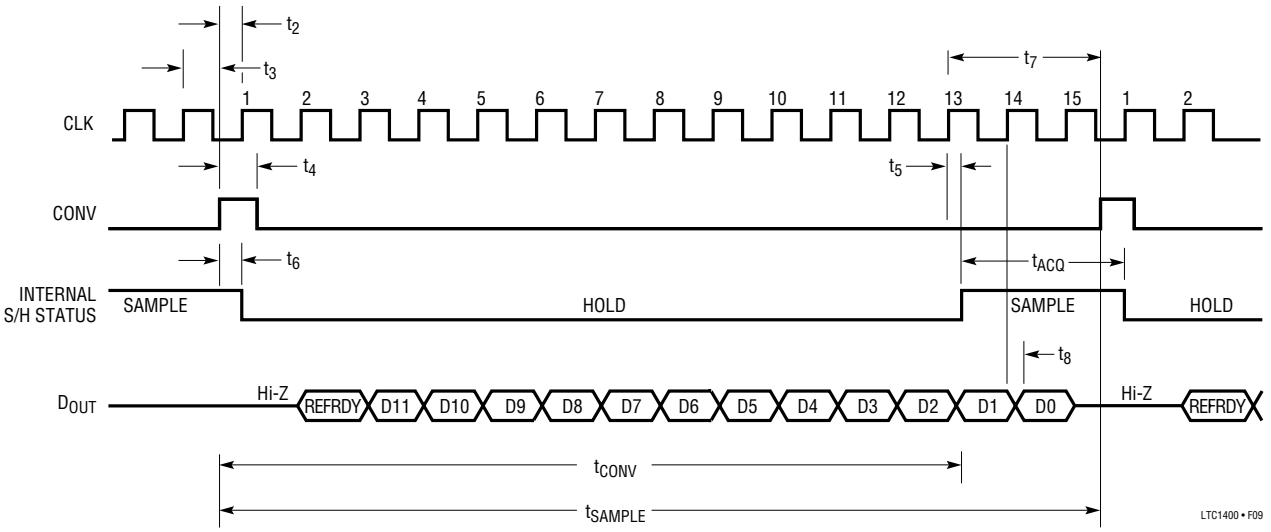


Figure 9. ADC Digital Timing Diagram

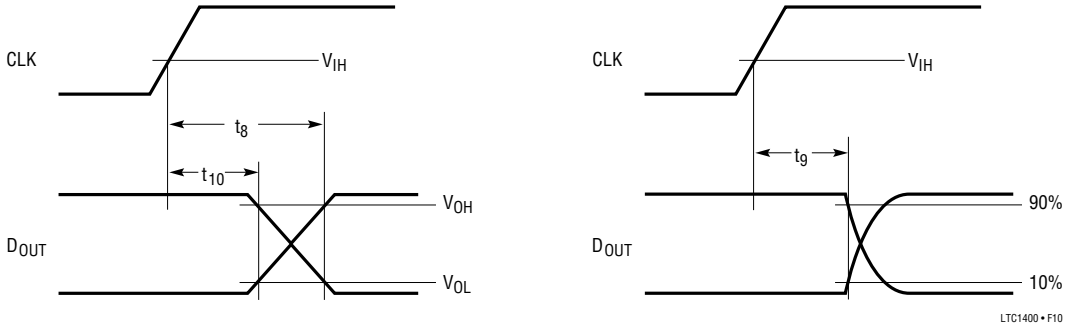
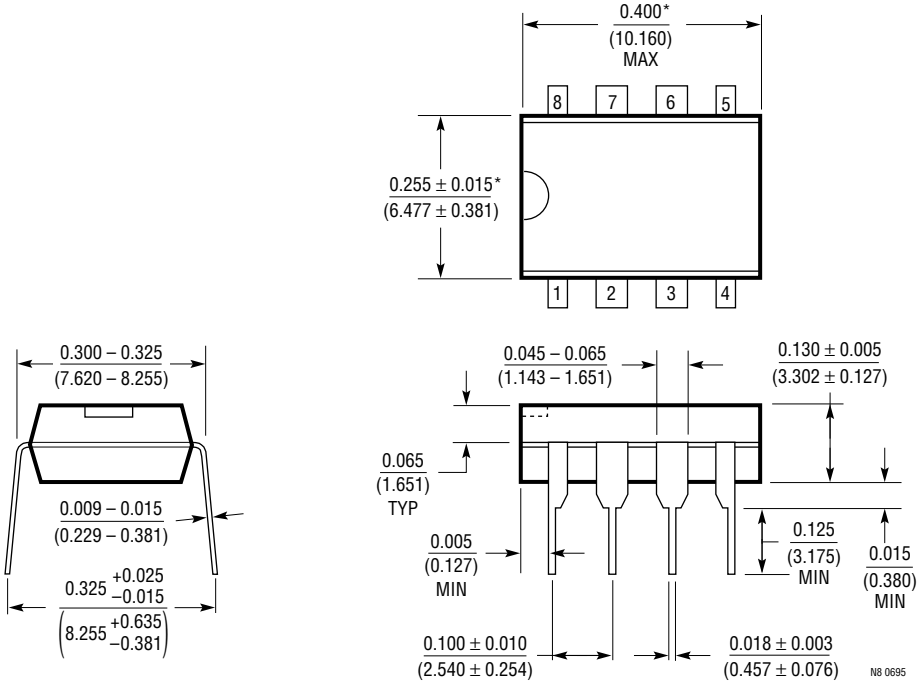


Figure 10. CLK to D_{OUT} Delay

PACKAGE DESCRIPTION

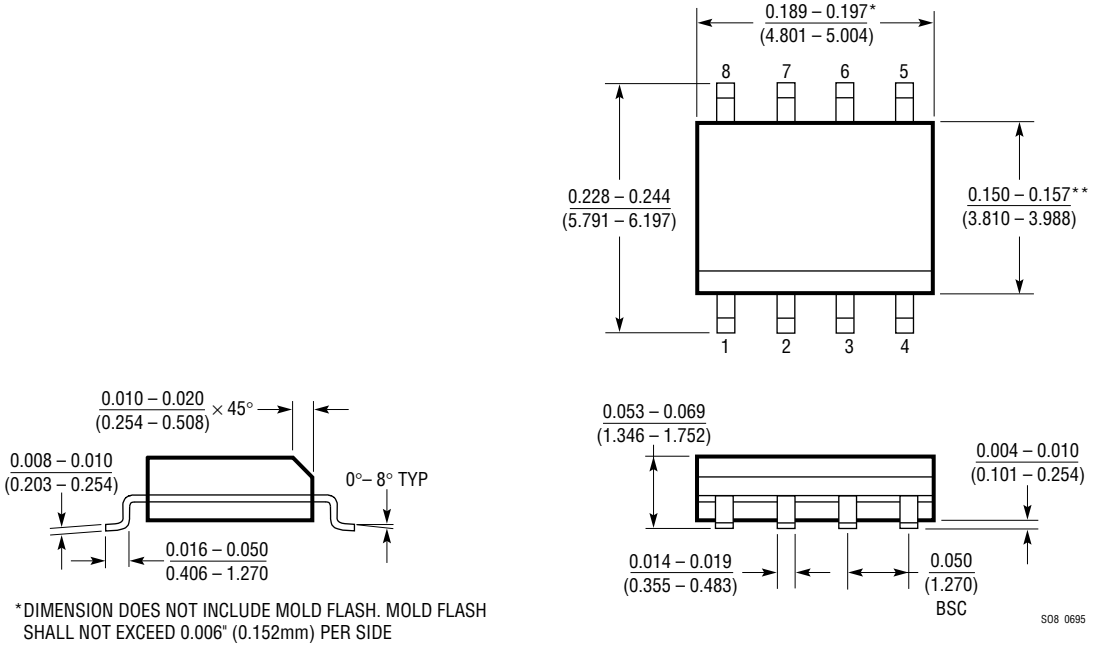
Dimension in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

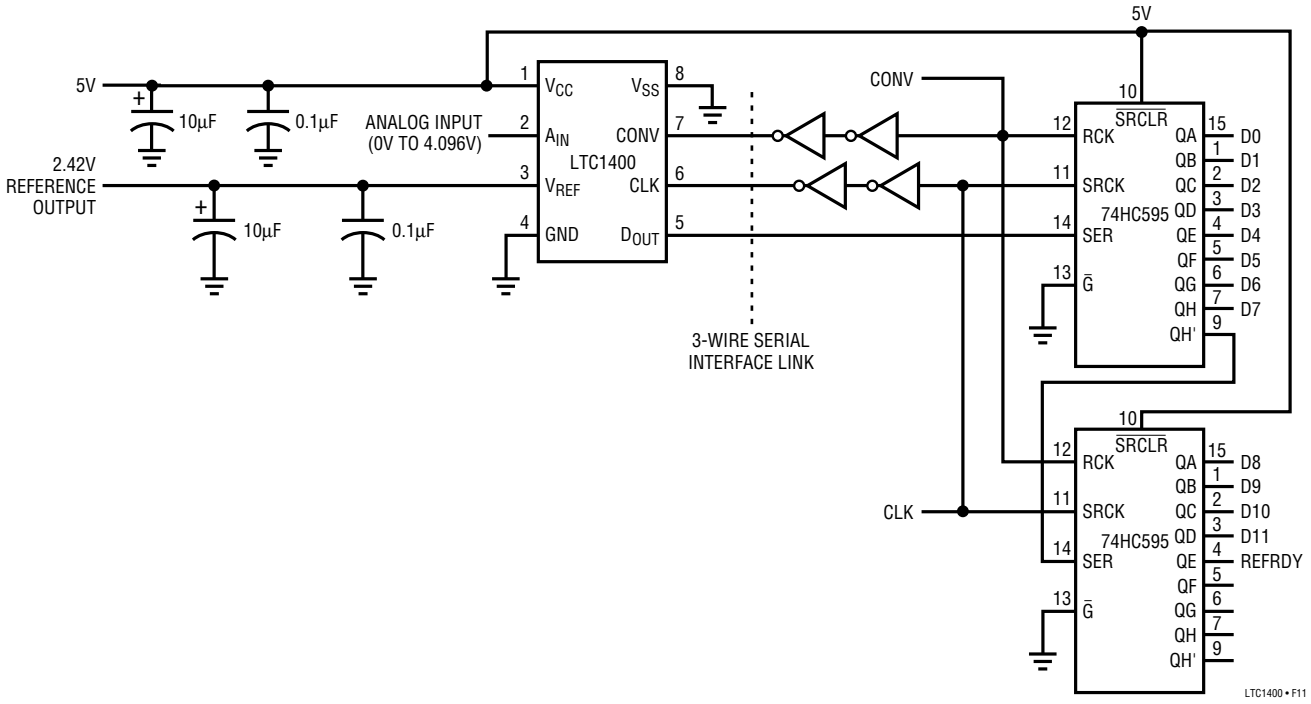
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION



RELATED PARTS

12-Bit Parallel Output ADCs

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
LTC1272	250ksps	75mW	Single 5V, 7572 Upgrade
LTC1273/LTC1275/LTC1276	300ksps	75mW	With Clock and Reference
LTC1274/LTC1277	100ksps	10mW	Low Power ADCs with 1µA Shutdown
LTC1278/LTC1279	500/600ksps	75mW	70dB at Nyquist, Low Power, Single 5V
LTC1282	140ksps	12mW	3V or ±3V ADC with Clock and Reference
LTC1410	1.25Msps	160mW	70dB at Nyquist, Differential Input

12-Bit Serial Output ADCs

PART NUMBER	VCC	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
LTC1285/LTC1288	3V	7.5/6.6ksps	0.48mW	3V, One or Two Input, Micropower, SO-8
LTC1286/LTC1298	5V	12.5/11.1ksps	1.25mV	One or Two Input, Micropower, SO-8
LTC1290	5/±5V	50ksps	30mW	8 Input, Full-Duplex Serial I/O
LTC1296	5/±5V	46.5ksps	30mW	8 Input, Half-Duplex Serial I/O, Power Shutdown Output

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