High Speed, Quad Universal Filter Building Block

FEATURES

- High Speed, Up to 250kHz Center Frequency
- Four Identical Filters in a 0.3" Wide Package
- Clock-to-Center Frequency Ratio of 20:1
- Double-Sampling, Improved Aliasing
- Operates from ±2.37V to ±8V Power Supplies
- Customized Version with Internal Resistors Available
- Low Noise
- Low Harmonic Distortion

APPLICATIONS

- Digital Communications
- Spread Spectrum Communications
- Spectral Analysis
- Loran Receivers
- Instrumentation

DESCRIPTION

The LTC1264 consists of four identical, high speed 2nd order switched-capacitor filter building blocks designed for center frequencies up to 250kHz. Each building block, together with three to five resistors, can provide 2nd order functions like lowpass, highpass, bandpass and notch. The center frequency of each 2nd order section is tuned via an external clock. The clock-to-center frequency ratio is internally set to 20:1, but it can be modified via external resistors.

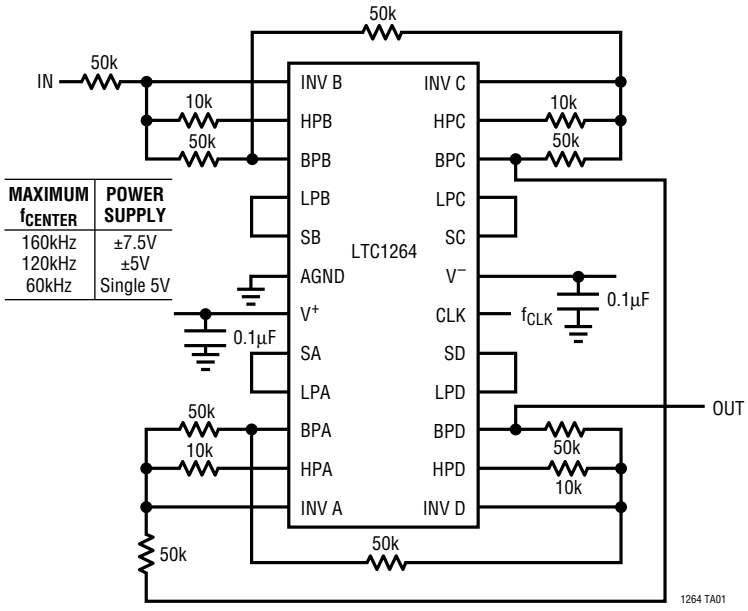
The aliasing performance of the LTC1264 is improved by double-sampling each 2nd order section. Input signal frequencies can reach up to twice the clock frequency before any alias products will be detectable.

For $Q \leq 5$ and for $T_A < 85°C$, the maximum center frequency is 160kHz. For $Q \leq 2$, the maximum center frequency is 250kHz. Up to 8th order filters can be realized by cascading all four 2nd order sections.

A customized monolithic version of the LTC1264 including internal thin film resistors can be obtained.

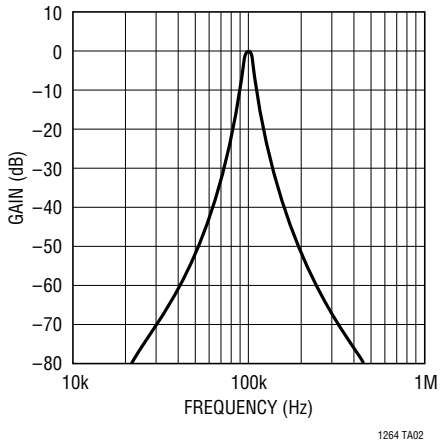
TYPICAL APPLICATION

Clock-Tunable 8th Order Bandpass Filter, $f_{CENTER} = f_{CLK}/20$



MAXIMUM f_{CENTER}	POWER SUPPLY
160kHz	±7.5V
120kHz	±5V
60kHz	Single 5V

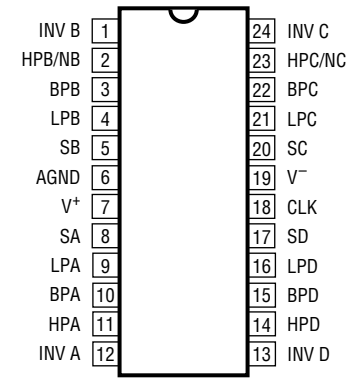
Gain vs Frequency
100kHz Bandpass, f_{-3dB} Bandwidth = $f_{CENTER}/10$



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
24-LEAD PLASTIC DIP

S PACKAGE
24-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)
T_{JMAX} = 110°C, θ_{JA} = 85°C/W (S)

ORDER PART NUMBER
LTC1264CN LTC1264CS

ELECTRICAL CHARACTERISTICS

(Internal Op Amps) T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range			±2.375		±8	V
Voltage Swings	V_S = ±2.375V, R_L = 5k			±1.5		V
	V_S = ±5V, R_L = 5k	 ●	±3.2 ±3.1	±3.7		V V
	V_S = ±7.5, R_L = 5k			±6		V
Output Short-Circuit Current (Source/Sink)				3		mA
DC Open-Loop Gain				80		dB
GBW Product				7		MHz
Slew Rate				10		V/µs

(Complete Filter) V_S = ±5V, f_{CLK} = 1MHz, all sides mode 1, f_0 = 50kHz, Q = 5, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_0 (Note 1)	V_S = ±7.5V, T_A < 85°C, Q < 2 V_S = ±5V, T_A < 85°C, Q < 2 V_S = ±2.5V, T_A < 85°C, Q < 2			0.1 - 250 0.1 - 200 0.1 - 100		kHz kHz kHz
Clock-to-Center Frequency Ratio, f_{CLK}/f_0				20:1		
Center Frequency Error (Note 3)	V_S = ±7.5V	 ●		±0.1	±0.7 ±0.8	% %
	V_S = ±5V	 ●		±0.2	±0.8 ±1.0	% %
	V_S = ±2.375V			–1.6		%
Clock-to-Center Frequency Ratio, Side-to-Side Matching	V_S ≥ ±5V	 ●		0.4	0.8 1.0	% %
Q Accuracy	V_S = ±5V	 ●		–2.7	 7.0	% %
f_0 Temperature Coefficient	f_{CLK} < 2MHz			±1		ppm/°C
Q Temperature Coefficient	f_{CLK} < 2MHz			5		ppm/°C

ELECTRICAL CHARACTERISTICS

(Complete Filter) V_S = ±5V, f_{CLK} = 1MHz, all sides mode 1, f_0 = 50kHz, Q = 5, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Offset Voltage (Note 2)	V_{OS1} (DC Offset of Input Inverter)	●			±20	mV
	V_{OS2} (DC Offset of First Integrator)	●			±45	mV
	V_{OS3} (DC Offset of Second Integrator)	●			±45	mV
Clock Feedthrough	V_S = ±7.5V (f_{CLK} is a Square Wave)			160		μV_{RMS}
	V_S = ±5V (f_{CLK} is a Square Wave)			120		μV_{RMS}
	V_S = ±2.375V (f_{CLK} is a Square Wave)			90		μV_{RMS}
Maximum Clock Frequency	V_S = ±7.5V, T_A = 25°C			6		MHz
Power Supply Current	V_S = ±5V		9	14	20	mA
		●			24	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Please refer to Typical Maximum Q vs Clock Frequency graphs.

Note 2: Calculations of output DC offsets of one 2nd order section. Also see Block Diagram.

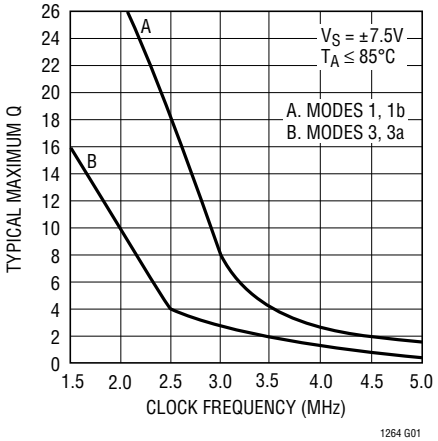
Note 3: The center frequency f_0, error is calculated as

$$\frac{f_0(\text{measured}) - f_0(\text{ideal})}{f_0\ (\text{ideal})} \times 100$$

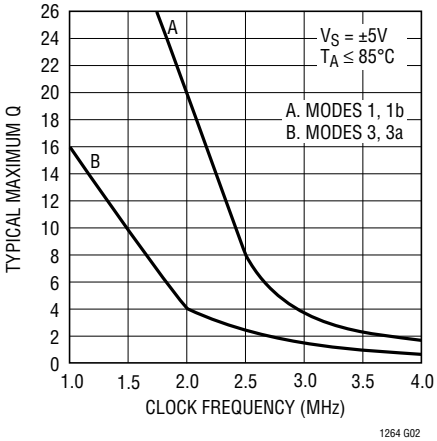
MODE	V_{OSN} PINS 2, 11, 14, 23	V_{OSBP} PINS 3, 10, 15, 22	V_{OSLP} PINS 4, 9, 16, 21
1	$V_{OS1}[(1Q) + 1 \lVert H_{OLP} \rVert] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$\approx(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}[1 + R4/R1 + R4/R2 + R4/R3] - V_{OS2}(R4/R2) - V_{OS3}(R4/R3)$

TYPICAL PERFORMANCE CHARACTERISTICS

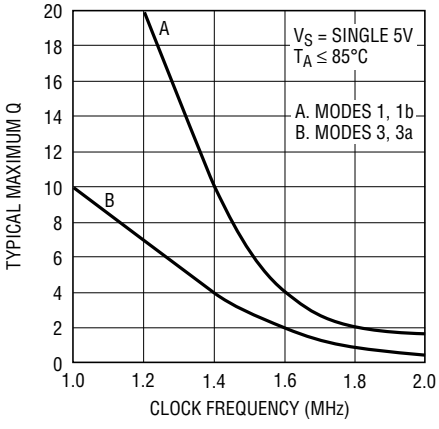
Typical Maximum Q vs Clock Frequency



Typical Maximum Q vs Clock Frequency

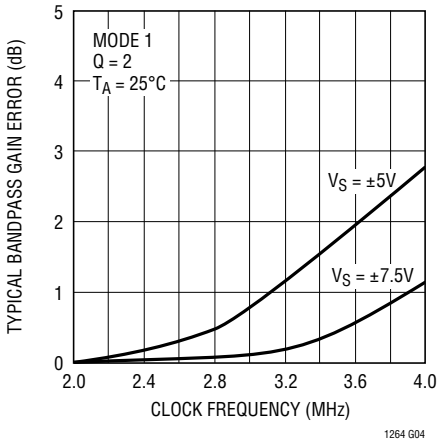


Typical Maximum Q vs Clock Frequency

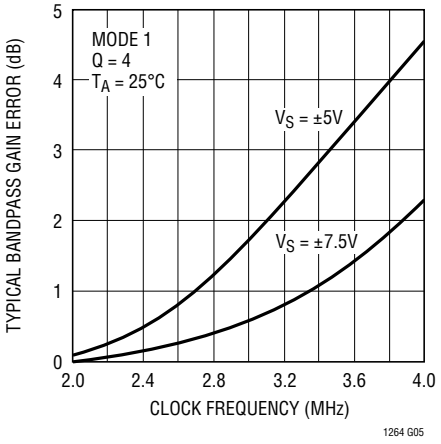


TYPICAL PERFORMANCE CHARACTERISTICS

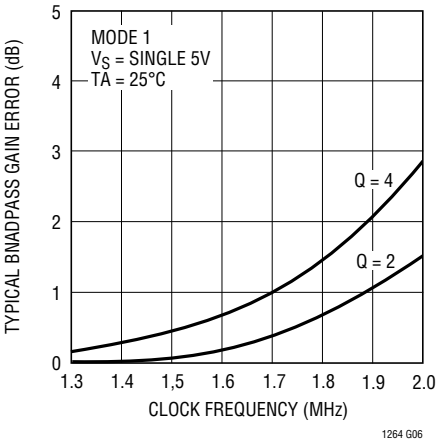
Typical Bandpass Gain Error vs Clock Frequency



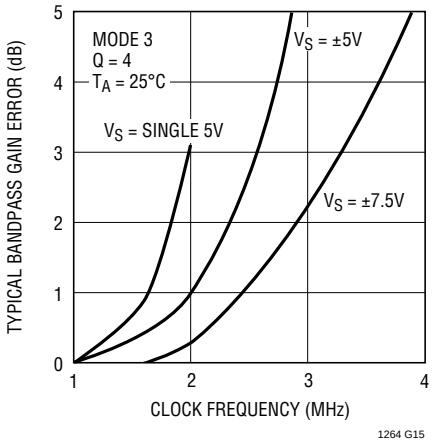
Typical Bandpass Gain Error vs Clock Frequency



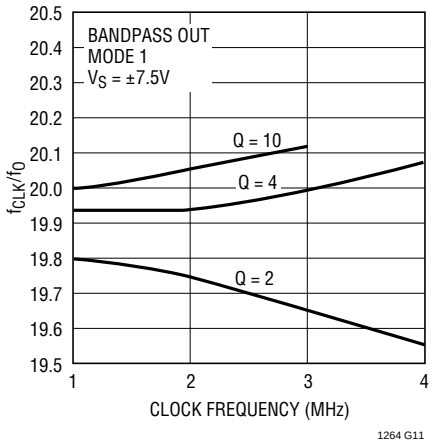
Typical Bandpass Gain Error vs Clock Frequency



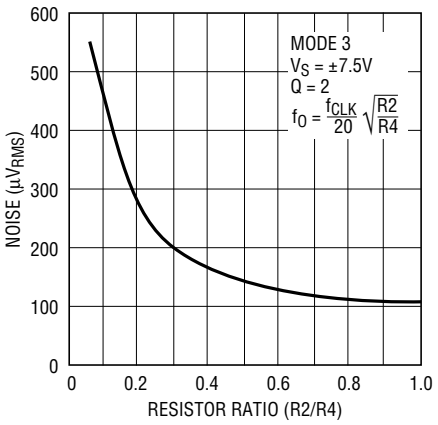
Typical Bandpass Gain Error vs Clock Frequency



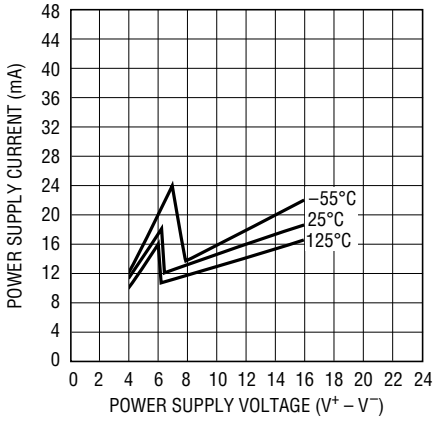
Ratio (f_{CLK}/f_O) vs Clock Frequency



Noise vs R2/R4 Ratio



Power Supply Current vs Supply Voltage



PIN FUNCTIONS

Power Supply Pins (7, 19)

The V^+ (pin 7) and the V^- (pin 19) should each be bypassed with a 0.1μF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/μs. When V^+ is applied before V^- and V^- is allowed to go above ground, a diode should clamp V^- to prevent latch-up. Figures 1 and 2 show typical connections for dual and single supply operation.

Analog Ground Pin (6)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 6 should be connected to the analog ground plane. For single supply operation, pin 6 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1μF capacitor (Figure 2). For single 5V operation and f_{CLK} greater than 1MHz, pin 6 should be biased at 2V. This minimizes passband gain and phase variations.

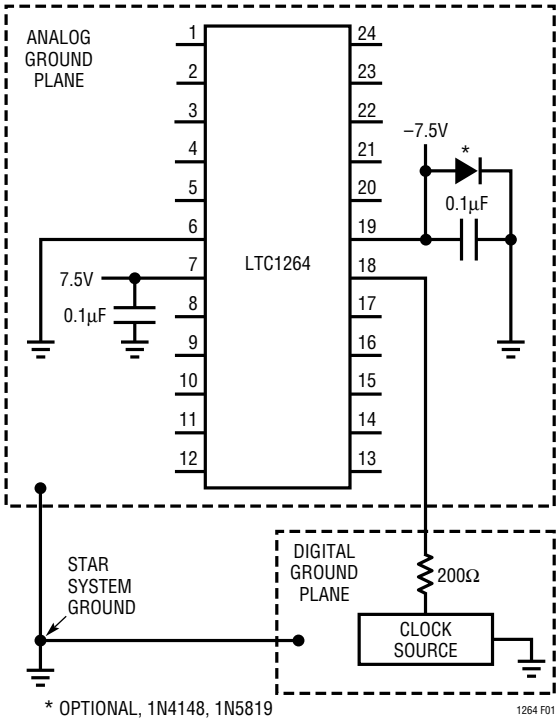


Figure 1. Dual Supply Ground Plane Connections

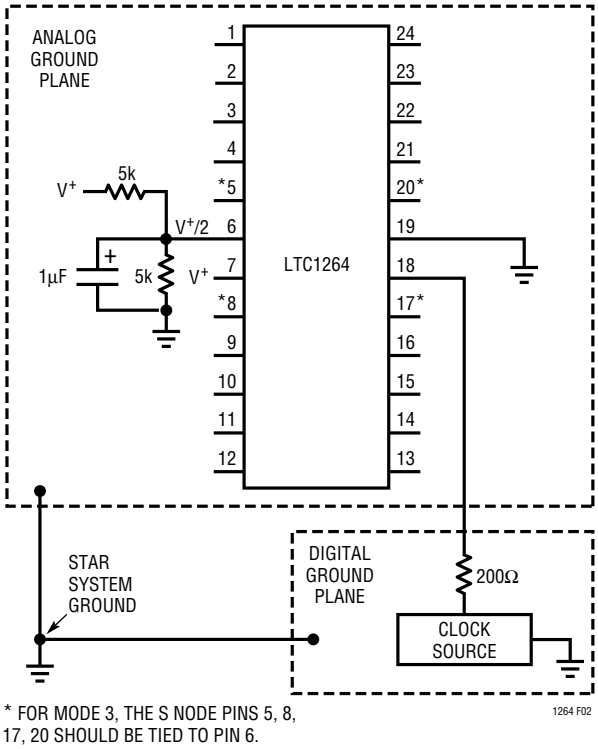


Figure 2. Single Supply Ground Plane Connections

PIN FUNCTIONS

Clock Input Pin (18)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high level threshold values for a dual or single supply operation.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

A pulse generator can be used as a clock source provided the high level ON-time is greater than 0.2µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 1 and 2).

Output Pins (2,3,4,9,10,11,14,15,16,21,22,23)

Each 2nd order section of the LTC1264 has three outputs which typically source 3mA and sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion performance of any filter design. When evaluating the distortion or noise performance of a particular filter design implemented with an LTC1264, the final output of the filter should be buffered with a wideband noninverting high slew rate amplifier (Figure 3).

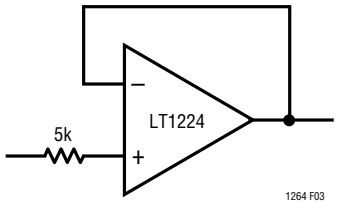


Figure 3. Wideband Buffer

Inverting Input Pins (1,12,13,24)

These pins are the high impedance inverting inputs of internal op amps and they are susceptible to stray capacitive connections to low impedance signal outputs and power supply lines.

Summing Input Pins (5,8,17,20)

The summing pins connections determine the circuit topology (mode) of each 2nd order section. Please refer to Modes of Operation.

MODES OF OPERATION

For the definition of filter functions please refer to the LTC1060 data sheet.

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 20:1. Figure 4 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency. Mode 1 is faster than Mode 3.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b (Figure 5) two additional resistors R5 and R6 are added to alternate the amount of voltage fed back from the lowpass output into the input of the SA (SB, SC or SD) switched-capacitor summer. This allows the filter's clock-to-center frequency ratio to be adjusted beyond 20:1. Mode 1b maintains the speed advantages of Mode 1 and should be considered an

MODES OF OPERATION

optimum mode for high Q designs with f_{CLK} to f_{CUTOFF} (or f_{CENTER}) ratios greater than 20:1.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

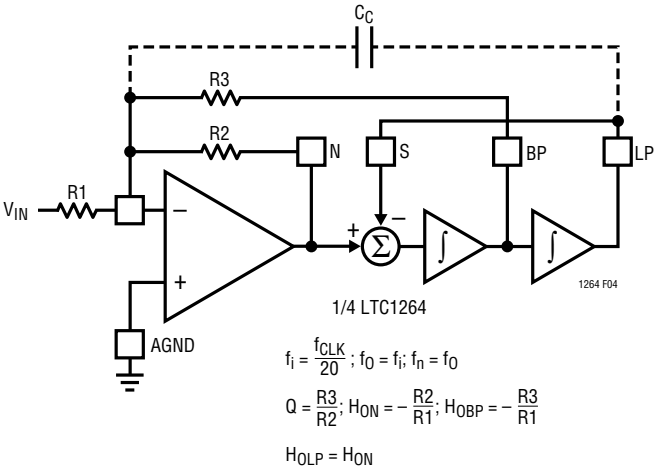


Figure 4. Mode 1, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

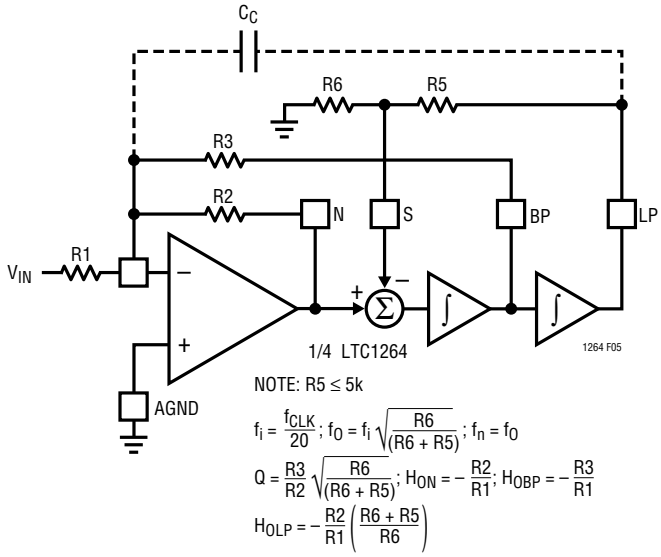


Figure 5. Mode 1b, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

Mode 3

In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below 20:1. Figure 6 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass, and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass, and highpass filters.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, shown in Figure 7. With Mode 2, the clock-to-center frequency ratio, f_{CLK}/f_O, is always less than 20:1. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. As in Mode 1, Mode 2 has a notch output which depends on the clock frequency, and the notch frequency is therefore less than the center frequency, f_O.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

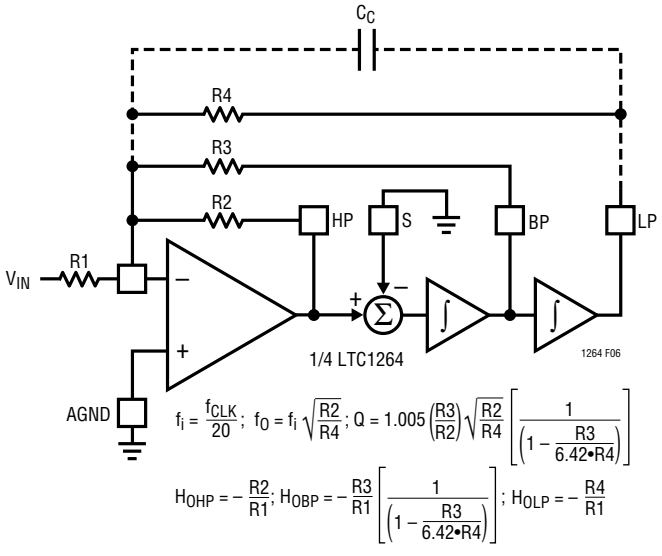
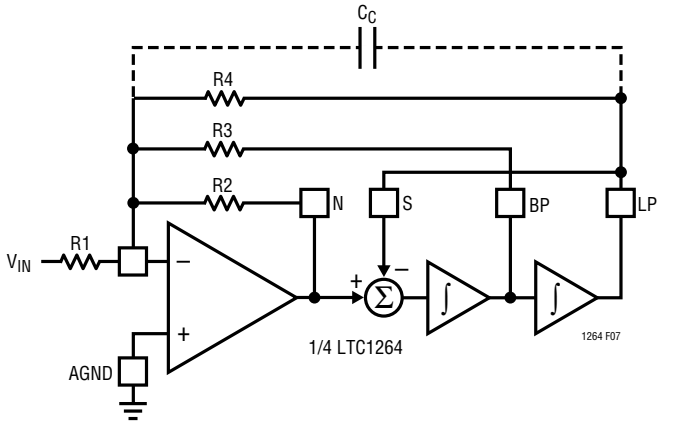


Figure 6. Mode 3, 2nd Order Section Providing Highpass, Bandpass and Lowpass Outputs

MODES OF OPERATION



$$f_i = \frac{f_{CLK}}{20};\ f_0 = f_i\sqrt{1+\frac{R2}{R4}};\ f_n = f_0$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{1+\frac{R2}{R4}}\left[\frac{1}{\left(1-\frac{R3}{6.42\bullet R4}\right)}\right]$$

$$H_{OHP} = -\frac{R2}{R1}\ (\text{AC GAIN, } f > f_n);\ H_{OHPn} = -\frac{R2}{R1}\left[\frac{1}{\left(1+\frac{R2}{R4}\right)}\right]\ (\text{DC GAIN, } f < f_n)$$

$$H_{OBP} = -\frac{R3}{R1}\left[\frac{1}{\left(1-\frac{R3}{6.42\bullet R4}\right)}\right];\ H_{OLP} = H_{OHPn}$$

Figure 7. Mode 2, 2nd Order Filter Providing Highpass Notch, Bandpass and Lowpass Outputs

Mode 3a

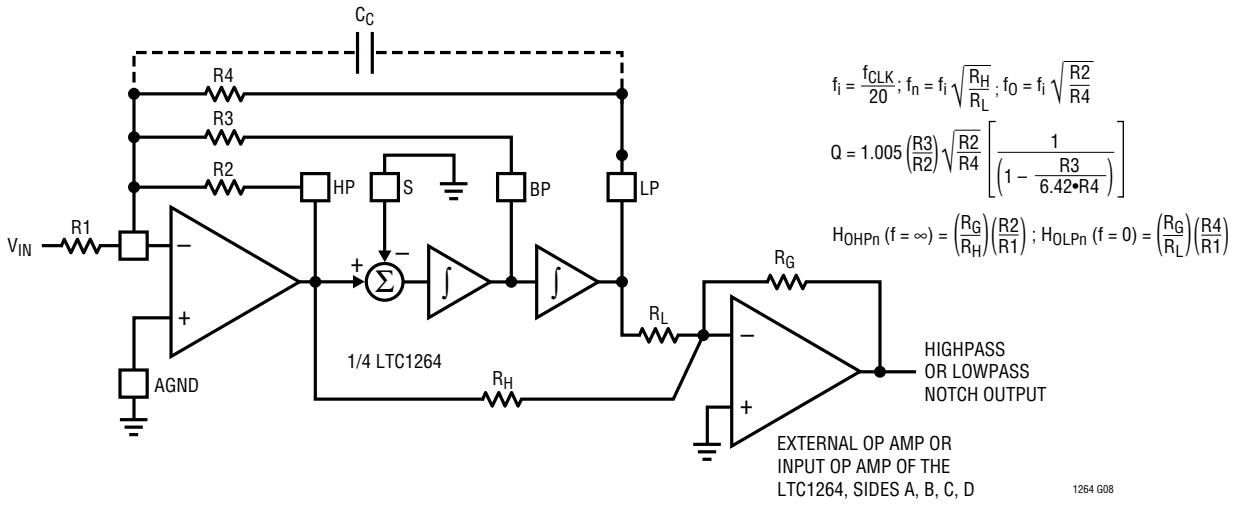
This is an extension of Mode 3 where the highpass and lowpass output are summed through two external resistors R_H and R_L to create a notch. This is shown in Figure 8. Mode 3a is more versatile than Mode 2 because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 8 is not always required. When cascading the sections of the LTC1264, the highpass and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2n

This mode extends the circuit topology of Mode 3a to Mode 2 (Figure 9) where the highpass notch and lowpass outputs are summed through two external resistors R_H and R_L to create a lowpass output with a notch higher in frequency than the notch in Mode 2. This mode, shown in Figure 8, is most useful in lowpass elliptic designs. When cascading the sections of the LTC1264, the highpass notch and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Maximum Frequency of Operation paragraph under Applications Information for a guide to the use of capacitor C_C.



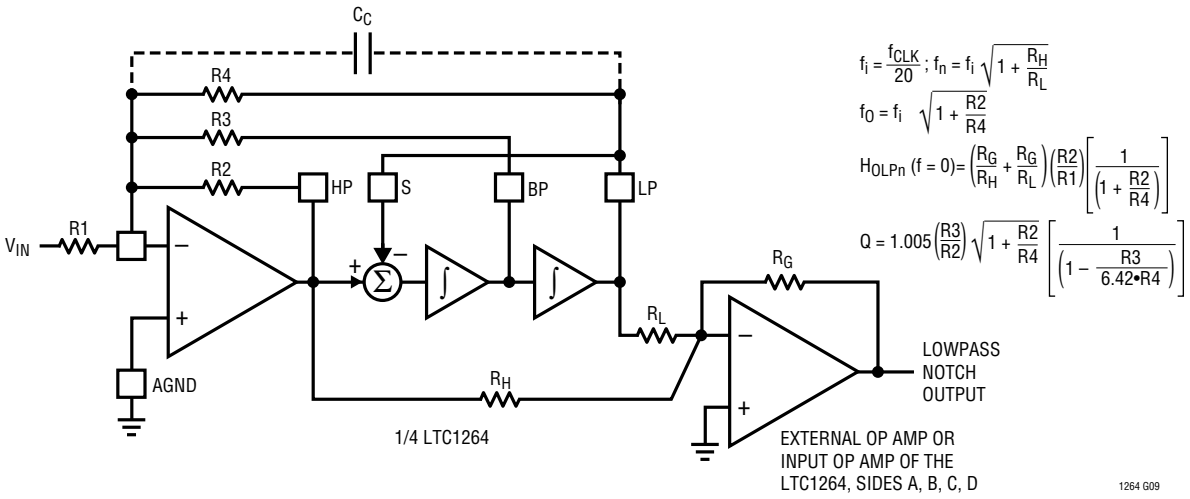
$$f_i = \frac{f_{CLK}}{20};\ f_n = f_i\sqrt{\frac{R_H}{R_L}};\ f_0 = f_i\sqrt{\frac{R2}{R4}}$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{\frac{R2}{R4}}\left[\frac{1}{\left(1-\frac{R3}{6.42\bullet R4}\right)}\right]$$

$$H_{OHPn}\ (f=\infty) = \left(\frac{R_G}{R_H}\right)\left(\frac{R2}{R1}\right);\ H_{OLPn}\ (f=0) = \left(\frac{R_G}{R_L}\right)\left(\frac{R4}{R1}\right)$$

Figure 8. Mode 3a, 2nd Order Filter Providing a Highpass Notch or Lowpass Notch Output

MODES OF OPERATION



$$f_i = \frac{f_{CLK}}{20};\ f_n = f_i\sqrt{1+\frac{R_H}{R_L}}$$

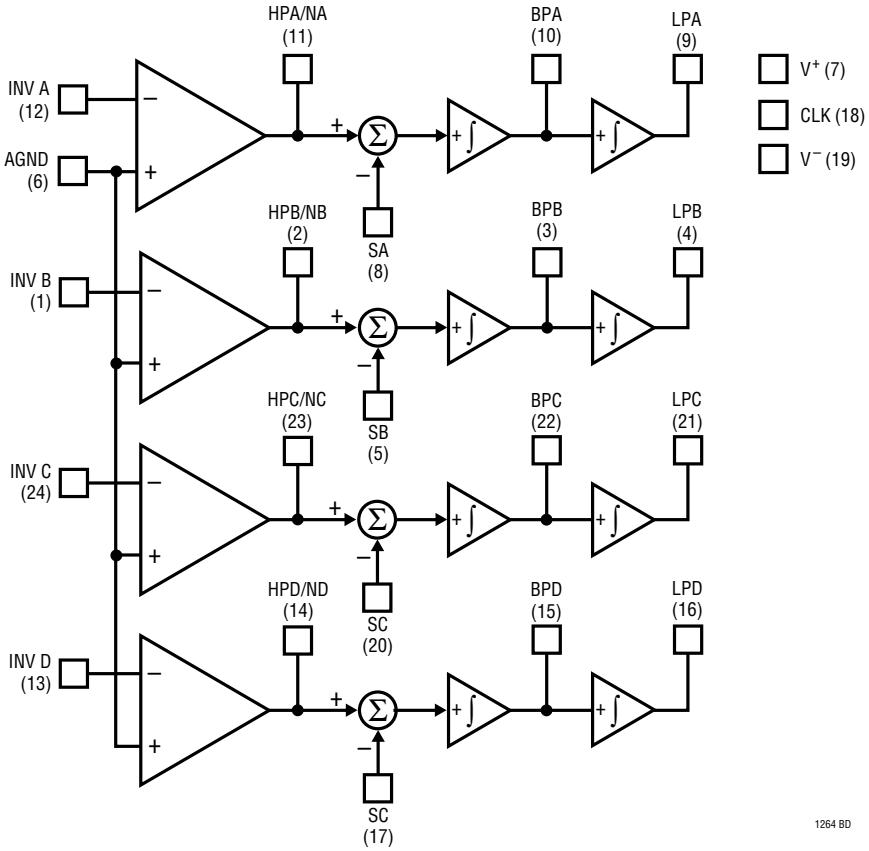
$$f_O = f_i\ \sqrt{1+\frac{R2}{R4}}$$

$$H_{OLPn}\,(f=0) = \left(\frac{R_G}{R_H}+\frac{R_G}{R_L}\right)\left(\frac{R2}{R1}\right)\left[\frac{1}{\left(1+\frac{R2}{R4}\right)}\right]$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{1+\frac{R2}{R4}}\left[\frac{1}{\left(1-\frac{R3}{6.42\bullet R4}\right)}\right]$$

Figure 9. Mode 2n, 2nd Order Filter Providing a Lowpass Notch Output

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Operating Limits

The Typical Maximum Q vs Clock Frequency and Bandpass Gain Error graphs, under Typical Performance Characteristics, define an upper limit of operating Q for each LTC1264 2nd order section. These graphs indicate the power supply, f_{CLK} and Q value conditions under which a filter implemented with an LTC1264 will remain stable when operated at temperatures of 85°C or less. For a 2nd order section, a bandpass gain error of 3dB or less is arbitrarily defined as a condition for stability.

When the passband gain error begins to exceed 1dB, the use of capacitor C_C will reduce the gain error (capacitor C_C is connected from the lowpass node to the inverting node of a 2nd order section). Please refer to Figures 4 through 9. The value of C_C can be best determined experimentally, and as a guide it should be about 5pF for each 1dB of gain error and not to exceed 15pF. When operating LTC1264 very near the limits defined by the Typical Performance Characteristics graphs, passband gain variations of 2dB or more should be expected.

Speed Limitations

To avoid op amp slew rate limiting, the signal amplitude should be kept below a specified level as shown in Table 2.

Table 2. Maximum V_{IN} vs V_S and Clock

V_S	MAXIMUM CLOCK	MAXIMUM V_{IN}
±7.5V	4MHz to 5MHz	$0.5V_{RMS}$ $f_{IN} \geq 400kHz$
±5V	3MHz to 4MHz	$0.5V_{RMS}$ $f_{IN} \geq 250kHz$
Single 5V	1MHz to 2MHz	$0.35V_{RMS}$ $f_{IN} \geq 160kHz$

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pins. The clock feedthrough is tested with the filter's input grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques, the typical values of clock feedthrough are listed under Electrical Characteristics.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple RC lowpass network at the final filter output. This RC will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering.

The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

For a specific filter design, the total noise depends on the Q of each section and the cascade sequence. Table 3 shows typical 2nd order section noise (gain = 1) for Q values and supplies operating at 25°C. Noise increases by 20% at the highest operating temperatures.

Table 3. 2nd Order Section Noise (μV_{RMS}) for Modes 1, 1b, 2 or 3 (R2 = R4)

Q	V_S = ±2.5V	V_S = ±5V	V_S = ±7.5V
1	$40\mu V_{RMS}$	50	60
2	$50\mu V_{RMS}$	60	75
3	$60\mu V_{RMS}$	75	95
4	$75\mu V_{RMS}$	90	115
5	$90\mu V_{RMS}$	110	135

Aliasing

Aliasing is an inherent phenomenon of switched-capacitor filters and it occurs when the frequency of input signals approaches the sampling frequency. The input signals that produce the strongest aliased components have a frequency, f_{IN}, such as ($f_{SAMPLING} - f_{IN}$) falls into the filter's passband. For the LTC1264 the sampling frequency is twice f_{CLK}. If the input signal spectrum is not band-limited, aliasing may occur.

APPLICATIONS INFORMATION

For example, for an LTC1264 bandpass filter with f_{CENTER} = 100kHz and f_{CLK} = 2MHz, a 3.9MHz, 10mV input will produce a 100kHz, 10mV output. A 1st or 2nd order prefilter will reduce aliasing to acceptable levels in most cases.

A GUIDE TO BANDPASS DESIGN

Filter design tools like FCAD require design specification inputs such as passband ripple, attenuation, passband width and stopband width in order to calculate filter parameters f_0, Q, f_n or poles and zeroes. The results of these filter approximations most often require Q values which make excessive demands on the gain-bandwidth products of active filter realizations. The active filter designer should define a gain response so that the filter's mathematical approximation has practical requirements. Table 4 is a guide to practical design specifications for realizing bandpass filters with LTC1264 (please also refer to the Typical Maximum Q vs Clock Frequency and Bandpass Gain Error graphs under Typical Performance Characteristics).

A Bandpass Design Example

Filter Type:	Bandpass
Filter Response:	Butterworth
Passband Ripple:	3dB
Attenuation:	60dB
Center Frequency:	40kHz (f_{CENTER})
Passband Width:	10kHz
Stopband Width:	60kHz

Implementing the Bandpass Design

With the LTC1264 in Mode 1b, Butterworth and Chebyshev bandpass designs with f_{CLK} to f_{CENTER} ratios greater than 20:1 are possible.

First choose the clock frequency which in Mode 1b must be greater than 20 times the bandpass center frequency of 40kHz. For this example, let's choose f_{CLK} to be 1MHz. Table 6 lists the resistors for for the bandpass design example and Figure 11 shows the complete circuit.

Table 4. Bandpass Design Specifications (f_{CENTER} is center frequency of passband.)

PASSBAND RIPPLE (dB)	PASSBAND WIDTH (Hz)	STOPBAND WIDTH (Hz)	ATTENUATION (dB)
≤ 3dB for Butterworth	≥ f_{CENTER}/20	≥ 5 × Passband	–40 to –60
≤ 0.1 for Chebyshev	≥ f_{CENTER}/20	≥ 5 × Passband	–40 to –60

Note: Reducing passband ripple or attenuation will decrease Q values. The filter order may also increase.

Table 5. Calculated Filter Parameters

STAGE	f_0	Q
1	38.1201kHz	4.3346
2	41.9726kHz	4.3346
3	35.6418kHz	10.5221
4	44.8911kHz	10.5221

Table 6. Calculated Mode 1b Resistors to Nearest 1% Value Using Table 5 Filter Parameters and Figure 10 Equations

STAGE	R1	R2	R3	R5	R6
1	52.3k	10k	56.2k	5k	6.98k
2	47.5k	10k	51.1k	5k	11.8k
3	56.2k	10k	147k	5k	5.11k
4	44.2k	10k	118k	5k	20.5k

$$R2 = 10k$$

$$R5 = 5k$$

$$f_i = \frac{f_{CLK}}{20}$$

$$R1 = \frac{R3}{H_{OBP}} \text{ (FOR BANDPASS)}$$

$$R6 = \frac{R5 \bullet f_0^2}{\left(f_i^2 - f_0^2\right)}$$

$$H_{OBP} = \sqrt{Q^2\left[\left(\frac{f_0}{f_{CENTER}}\right) - \left(\frac{f_{CENTER}}{f_0}\right)\right]^2 + 1}$$

$$R3 = \frac{R2 \bullet Q}{\sqrt{\frac{R6}{(R6 + 5)}}}$$

1264 F10

Figure 10. Equations for Resistors in Mode 1b Operation

APPLICATIONS INFORMATION

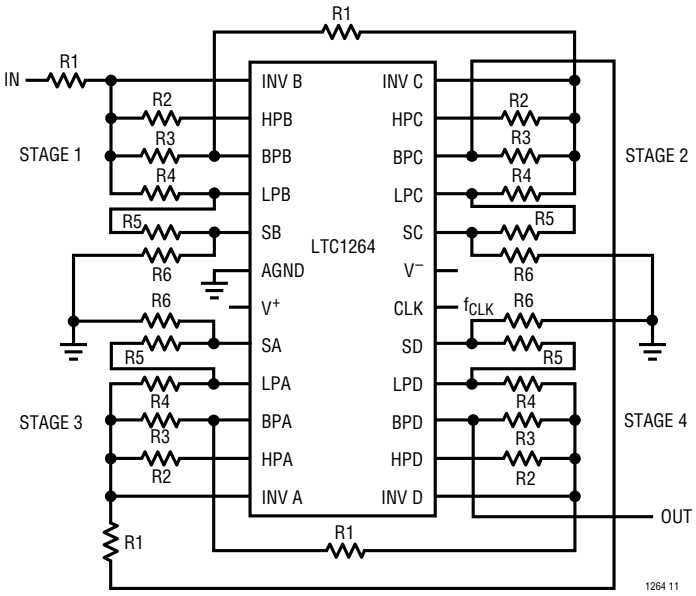


Figure 11. Mode 1b Bandpass Filter

Figures 12 and 13 show the gain response graphs of the 40kHz Butterworth bandpass design described above. The passband gain response graph (Figure 12) shows a 40kHz gain of – 0.4dB and a tilted passband from 37kHz to 43kHz. These errors are due to the 1% resistors used and the side-to-side matching of the LTC1264 f_{CLK}-to-f_{CENTER} ratio which typically is 0.4%. To adjust for 0dB gain at 40kHz, reduce the value of R1 in the first stage by 5%. To adjust for a flat passband, adjust by ±1% the value of R6 in stages 3 and 4. Adjusting R6 compensates for the side-to-side matching errors. Please refer to Figure 5 equations defining f_0 and Q as a function of R6.

The sequence of 2nd order stages and the bandpass gain H_{OBP} of each stage will determine the gain peaks at the filter's intermediate outputs. A given internal output can have several dB more gain than the final filter output. Gain peaks occur around the corners of the passband. The gain peaks can be reduced by increasing the R1 resistor of the first stage and decreasing the R1 resistor of the last stage by the same amount (multiplying the R1 resistor of the first stage and dividing the R1 resistor of the last stage by 2 for narrowband filter, and by 5 for wideband filter is a good rule of thumb). This adjustment may, however, increase the filter's passband noise.

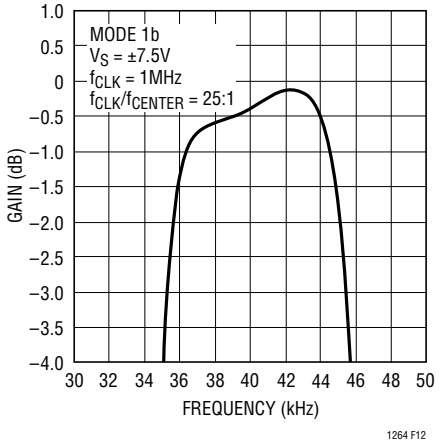


Figure 12. Passband Gain vs Frequency 40kHz Butterworth Bandpass

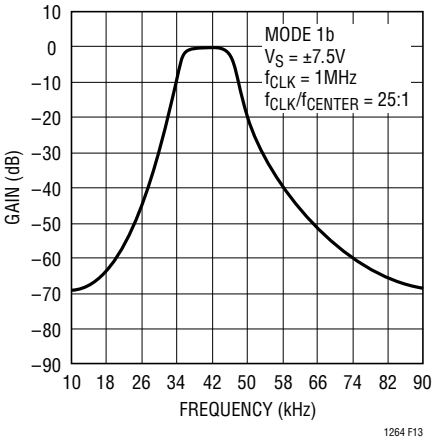
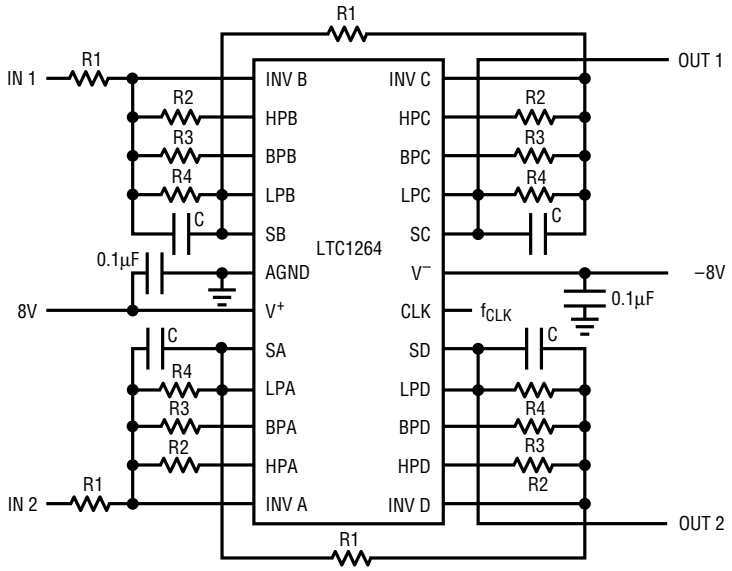


Figure 13. Gain vs Frequency 40kHz Butterworth Bandpass

TYPICAL APPLICATIONS

Linear Phase Clock-Tunable to 400kHz, Dual 4th Order Lowpass Filter



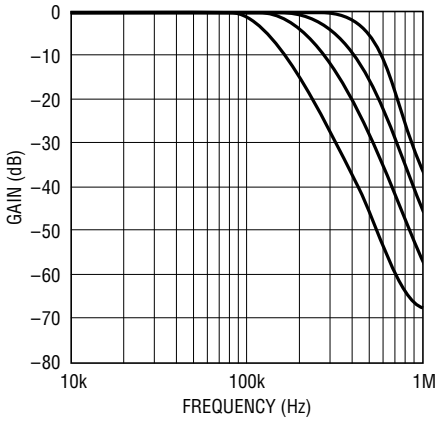
LTC1264 SIDE	B	C	A	D
MODE	2	2	2	2
R1	17.8k	20k	17.8k	20k
R2	27.4k	27.4k	27.4k	27.4k
R3	19.6k	21k	19.6k	21k
R4	51.1k	75k	51.1k	75k
C	5pF	5pF	5pF	5pF

f_{CLK}	f_{-3dB} (V_S = ±8V)
2MHz	125kHz
3MHz	200kHz
4MHz	275kHz
5MHz	400kHz

$T_A \leq 50°C$

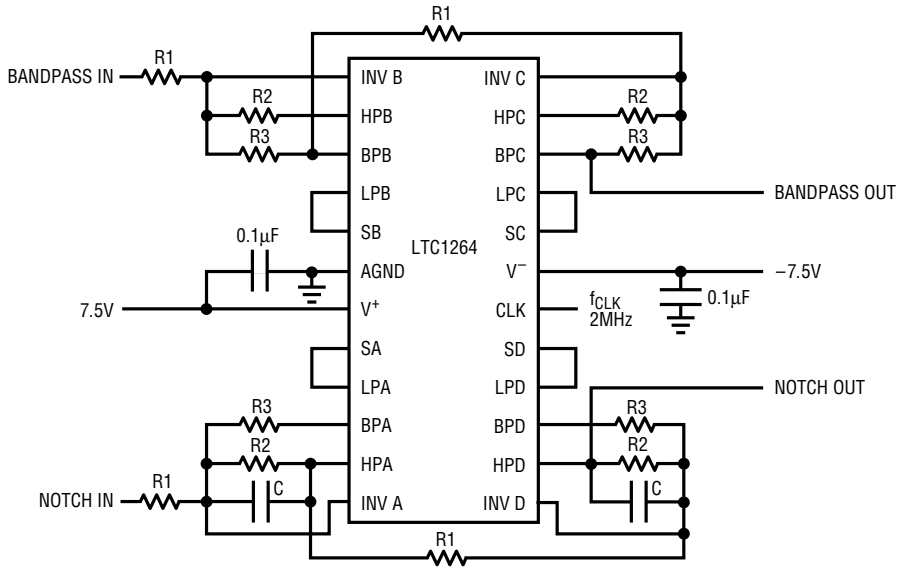
1264 TA04a

Gain vs Frequency



1264 TA04b

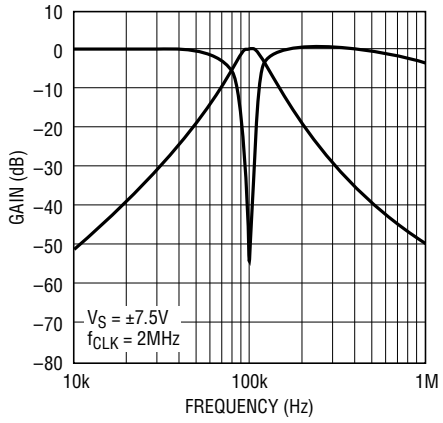
Clock-Tunable, $f_{CENTER} = f_{CLK}/20$, 100kHz, 4th Order Bandpass and Notch Filters



LTC1264 SIDE	B	C	A	D
MODE	1	1	1	1
R1	20k	20k	10k	10k
R2	10k	10k	10k	10k
R3	20k	20k	20k	20k
C			10pF	10pF

1264 TA05a

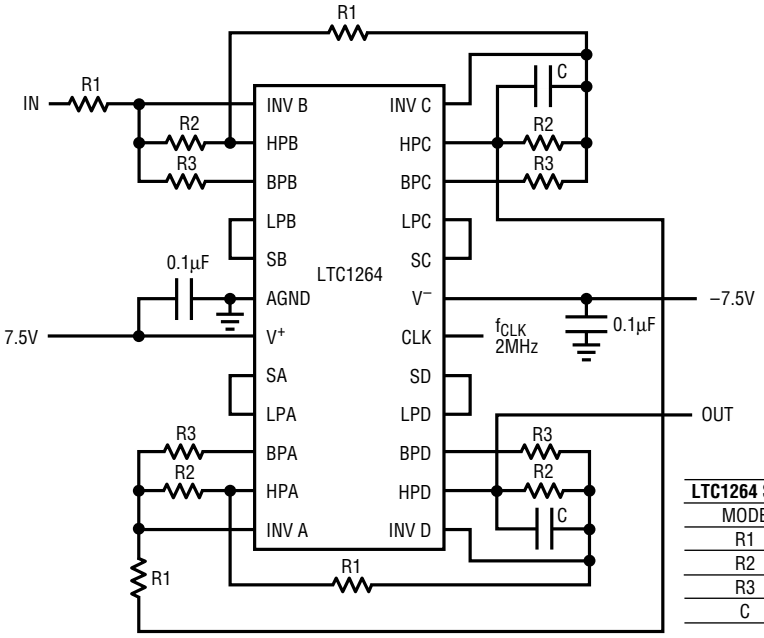
Gain vs Frequency



1264 TA05b

TYPICAL APPLICATIONS

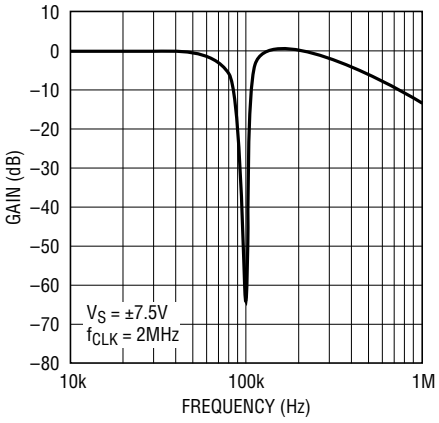
100kHz, 8th Order Notch Filter, f_{CLK}/f_{CENTER} = 20:1



LTC1264 SIDE	B	C	A	D
MODE	1	1	1	1
R1	36.5k	3.92k	7.5k	9.09k
R2	10k	10k	10k	10k
R3	50k	27.4k	50k	50k
C		30pF		30pF

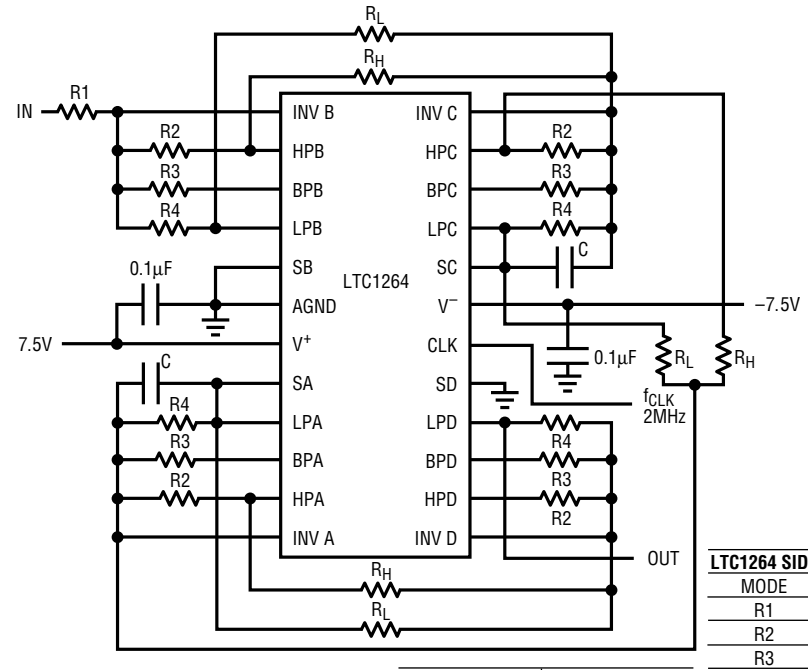
1264 TA06a

Gain vs Frequency



1264 TA06b

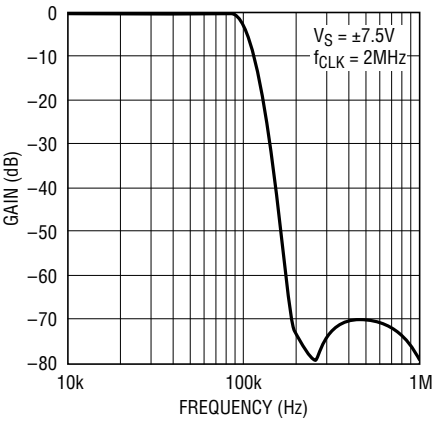
Clock-Tunable, 8th Order Elliptic Lowpass Filter, f_{CLK}/f_{CUTOFF} = 20:1



1264 TA03a

POWER SUPPLY	MAXIMUM f_{CLK}
±7.5V	3.6MHz (C = 10pF)
±5V	2.0MHz (C = 10pF)
SINGLE 5V	1.6MHz (C = 10pF)

Gain vs Frequency

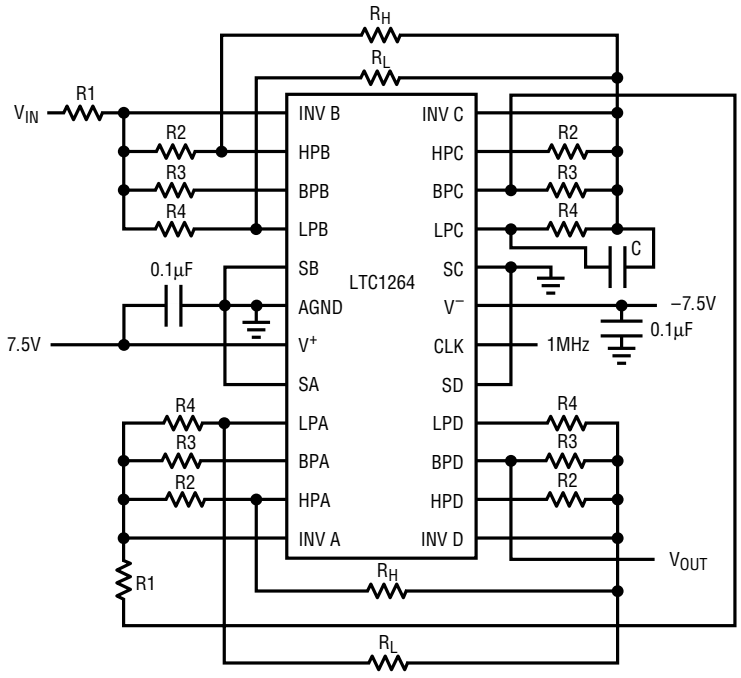


1264 TA03b

LTC1264 SIDE	B	C	A	D
MODE	3a	2n	2n	3
R1	27.4k			
R2	23.7k	20k	20k	29.4k
R3	20k	37.4k	37.4k	19.1k
R4	28k	100k	100k	48.7k
R_H	137k	100k	130k	
R_L	27.4k	31.6k	24.3k	
C		3pF	3pF	

TYPICAL APPLICATIONS

8th Order Bandpass Filter, Linear Phase

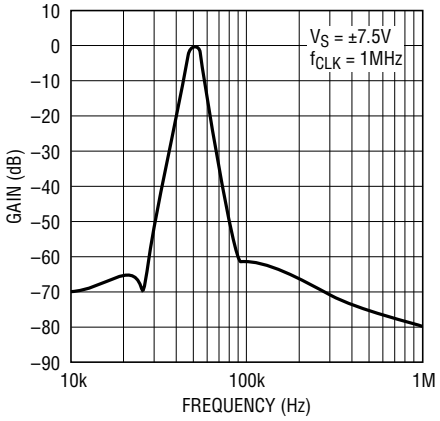


LTC1264 SIDE	B	C	A	D
MODE	3a	3	3a	3
R1	97.6k		32.4k	
R2	10.7k	12.4k	10.7k	10.0k
R3	39.2k	39.2k	12.4k	29.4k
R4	13.3k	10.7k	11.5k	10.0k
R_H		53.6		27.4k
R_L		15.0k		100.0k

f_{CLK}	C
1MHz	0pF
1.5MHz	5pF
2.0MHz	10pF

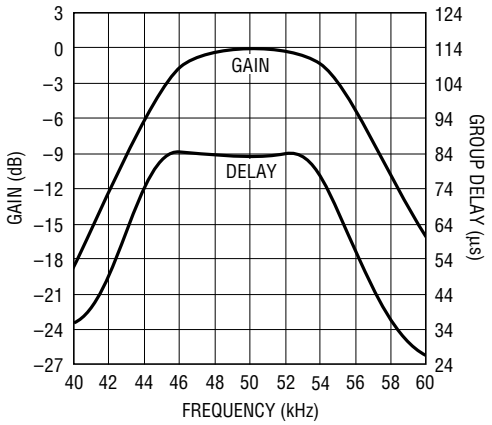
1264 TA07a

50kHz Bandpass Filter, Linear Phase Gain vs Frequency



1264 TA07b

Passband Gain and Group Delay

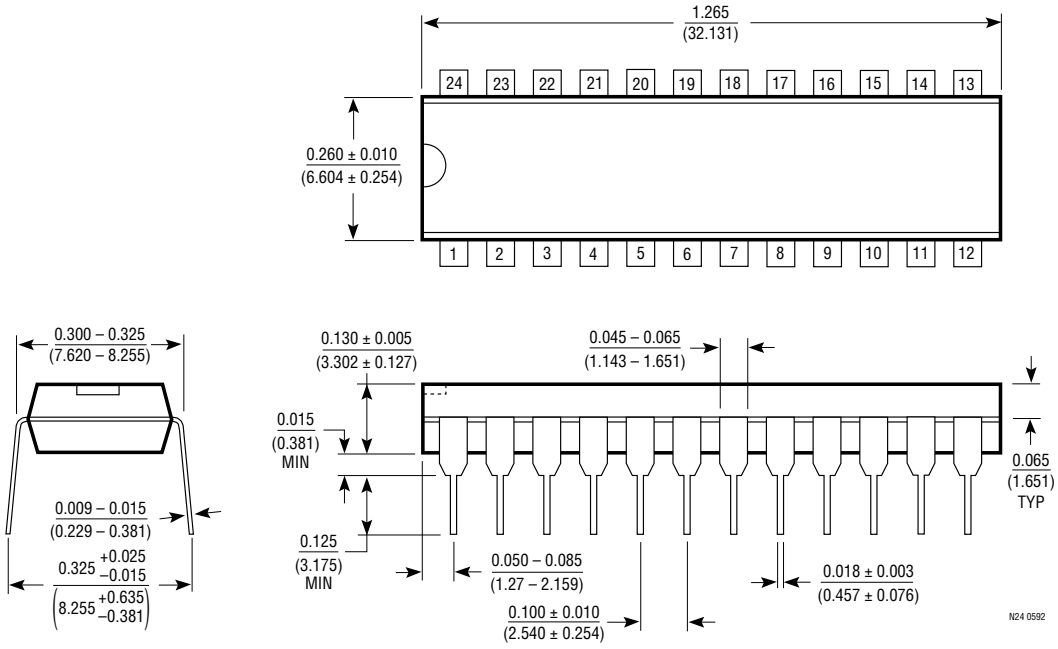


1264 TA07c

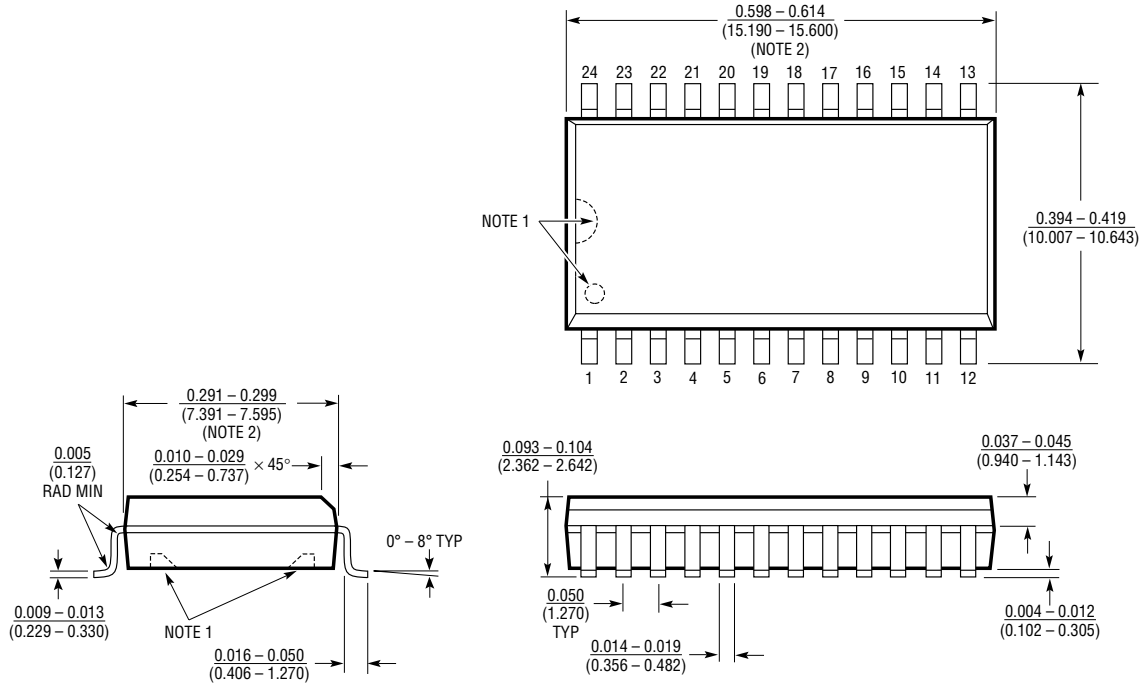
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
24-Lead Plastic DIP



S Package
24-Lead Plastic SOL



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 0693 10K REV 0