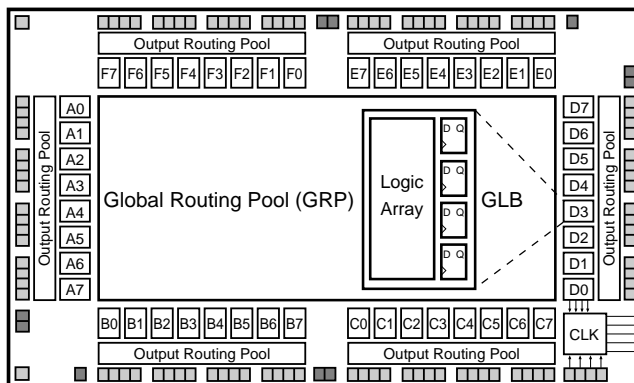


Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
 - 8000 PLD Gates
 - 96 I/O Pins, Ten Dedicated Inputs
 - 288 Registers
 - High-Speed Global Interconnects
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - $f_{max} = 80$ MHz Maximum Operating Frequency
 - $f_{max} = 50$ MHz for Industrial Devices
 - $t_{pd} = 15$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
 - In-System ProgrammableTM (ISPTM) 5-Volt Only
 - Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
 - Reprogram Soldered Devices for Faster Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Four Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity
- **ispLSI AND pLSI DEVELOPMENT TOOLS**
 - pDS[®] Software**
 - Easy to Use PC WindowsTM Interface
 - Boolean Logic Compiler
 - Manual Partitioning
 - Automatic Place and Route
 - Static Timing Table
 - pDS+TM Software**
 - Industry Standard, Third Party Design Environments
 - Schematic Capture, State Machine, HDL
 - Automatic Partitioning and Place and Route
 - Comprehensive Logic and Timing Simulation
 - PC and Workstation Platforms

Functional Block Diagram



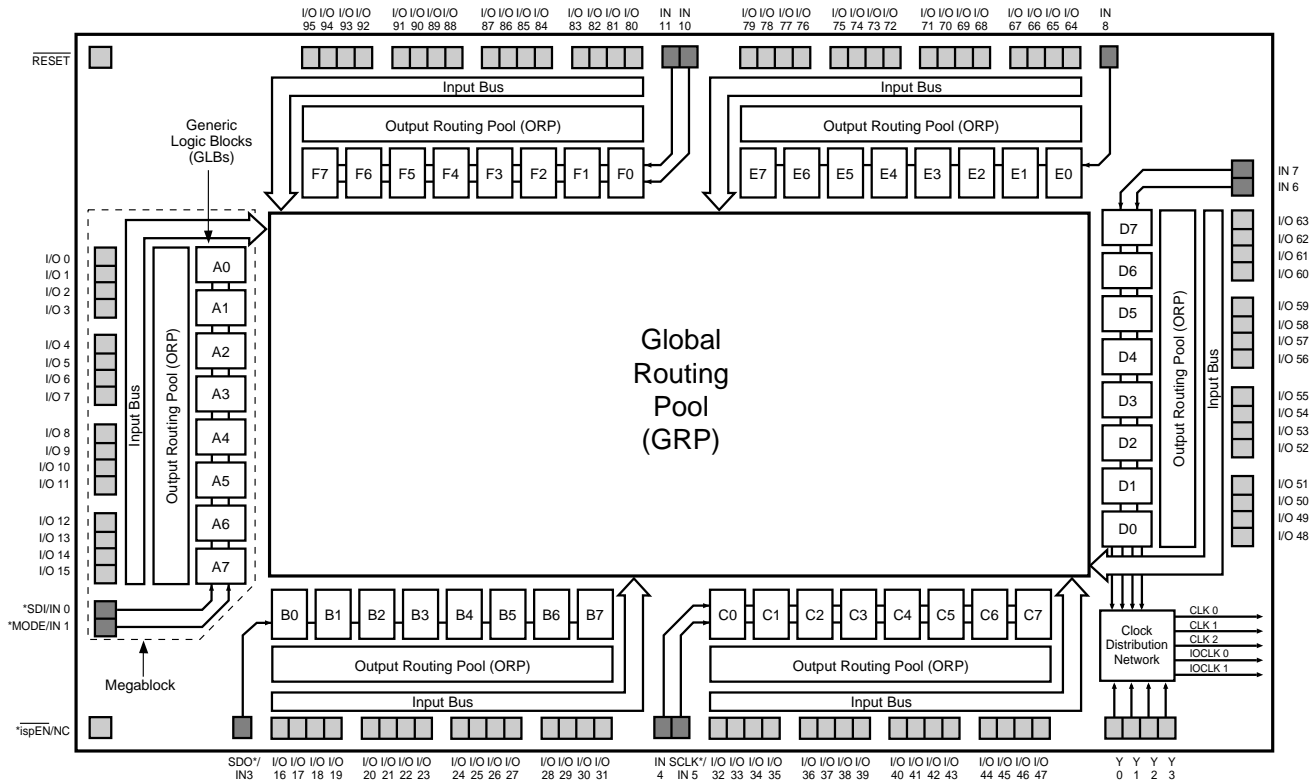
Description

The ispLSI and pLSI 1048 are High-Density Programmable Logic Devices which contain 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 1048 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see figure 1). There are a total of 48 GLBs in the ispLSI and pLSI 1048 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. ispLSI and pLSI 1048 Functional Block Diagram



*ISP Control Functions for ispLSI 1048 Only

0139F(1)-48-isp

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs (one dedicated input in Megablock B and E) and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI and pLSI 1048 devices contain six of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1048 devices are selected using the Clock Distribution Network. Four dedicated clockpins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI and pLSI 1048 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

Supply Voltage V_{CC} -0.5 to +7.0V
 Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T _A = 0°C to +70°C	4.75	5.25	V
		Industrial T _A = -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 1	V

Capacitance ($T_A=25^\circ\text{C}$, $f=1.0\text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM ¹	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	$V_{CC}=5.0V$, $V_{IN}=2.0V$
C_2	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$, V_{IO} , $V_Y=2.0V$

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	—	Years
ispLSI Erase/Reprogram Cycles	10000	—	Cycles
pLSI Erase/Reprogram Cycles	100	—	Cycles

Table 2- 0008B

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	$\leq 3\text{ns}$ 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

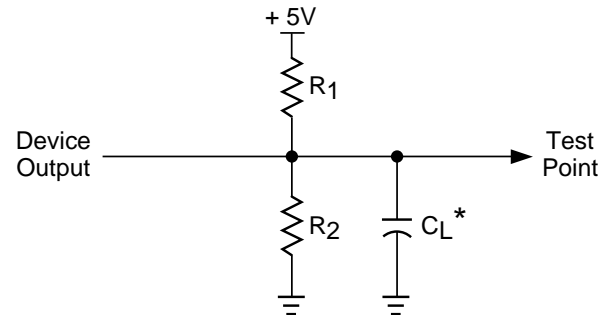
3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470 Ω	390 Ω	35pF
B	Active High	∞	390 Ω	35pF
	Active Low	470 Ω	390 Ω	35pF
C	Active High to Z at $V_{OH} - 0.5\text{V}$	∞	390 Ω	5pF
	Active Low to Z at $V_{OL} + 0.5\text{V}$	470 Ω	390 Ω	5pF

Figure 2. Test Load



*CL includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
V_{OL}	Output Low Voltage	$I_{OL} = 8\text{ mA}$	—	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4\text{ mA}$	2.4	—	—	V
I_{IL}	Input or I/O Low Leakage Current	$0\text{V} \leq V_{IN} \leq V_{IL} (\text{MAX.})$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$3.5\text{V} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
I_{IL-isp}	isp Input Low Leakage Current	$0\text{V} \leq V_{IN} \leq V_{IL} (\text{MAX.})$	—	—	-150	μA
I_{IL-PU}	I/O Active Pull-Up Current	$0\text{V} \leq V_{IN} \leq V_{IL}$	—	—	-150	μA
I_{OS1}	Output Short Circuit Current	$V_{CC} = 5\text{V}, V_{OUT} = 0.5\text{V}$	—	—	-200	mA
I_{CC}^{2,4}	Operating Power Supply Current	$V_{IL} = 0.5\text{V}, V_{IH} = 3.0\text{V}$ $f_{TOGGLE} = 1\text{ MHz}$	Commercial	165	235	mA
			Industrial	165	260	mA

- One output at a time for a maximum duration of one second. $V_{out} = 0.5\text{V}$ was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
- Measured using twelve 16-bit counters.
- Typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
- Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum I_{CC} .

Table 2- 0007A-48-isp

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-80		-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	18	–	24	ns
t _{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	20	–	23	–	30.7	ns
f _{max} (Int.)	A	3	Clock Frequency with Internal Feedback ³	80	–	71.4	–	53.6	–	MHz
f _{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	50	–	41.7	–	31.3	–	MHz
f _{max} (Tog.)	–	5	Clock Frequency, Max Toggle ⁴	100	–	83	–	71.4	–	MHz
t _{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	12	–	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	12	–	16	ns
t _{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
t _{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	12	–	16	–	ns
t _{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	14	–	18.7	ns
t _{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	–	17	–	17	–	22.7	ns
t _{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
t _{en}	B	14	Input to Output Enable	–	18	–	20	–	26.7	ns
t _{dis}	C	15	Input to Output Disable	–	18	–	20	–	26.7	ns
t _{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	7	–	ns
t _{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	7	–	ns
t _{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2	–	2.7	–	ns
t _{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	6.5	–	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.

2. Refer to Timing Model in this data sheet for further details.

3. Standard 16-Bit loadable counter using GRP feedback.

4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.

5. Reference Switching Test Conditions section.

Table 2- 0030A-48/80,70,50

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-80		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{iobp}	20	I/O Register Bypass	–	2.5	–	3.0	–	4.0	ns
t _{iolat}	21	I/O Latch Delay	–	3.3	–	4.0	–	5.3	ns
t _{iosu}	22	I/O Register Setup Time before Clock	5.3	–	6.0	–	8.1	–	ns
t _{ioh}	23	I/O Register Hold Time after Clock	1.5	–	0.5	–	0.9	–	ns
t _{ioco}	24	I/O Register Clock to Out Delay	–	2.5	–	3.0	–	3.9	ns
t _{ior}	25	I/O Register Reset to Out Delay	–	2.9	–	3.5	–	4.6	ns
t _{din}	26	Dedicated Input Delay	–	5.0	–	6.0	–	8.0	ns
GRP									
t _{grp1}	27	GRP Delay, 1 GLB Load	–	2.1	–	2.5	–	3.3	ns
t _{grp4}	28	GRP Delay, 4 GLB Loads	–	2.5	–	3.0	–	4.0	ns
t _{grp8}	29	GRP Delay, 8 GLB Loads	–	3.3	–	4.0	–	5.3	ns
t _{grp12}	30	GRP Delay, 12 GLB Loads	–	4.2	–	5.0	–	6.7	ns
t _{grp16}	31	GRP Delay, 16 GLB Loads	–	5.0	–	6.0	–	8.0	ns
t _{grp48}	32	GRP Delay, 48 GLB Loads	–	13.3	–	16.0	–	21.3	ns
GLB									
t _{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.4	–	6.5	–	8.6	ns
t _{1ptxor}	34	1 Product Term/XOR Path Delay	–	6.5	–	7.0	–	9.3	ns
t _{20ptxor}	35	20 Product Term/XOR Path Delay	–	7.6	–	7.5	–	10.0	ns
t _{xoradj}	36	XOR Adjacent Path Delay ³	–	8.4	–	9.5	–	12.7	ns
t _{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t _{gsu}	38	GLB Register Setup Time before Clock	0.8	–	1.5	–	2.0	–	ns
t _{gh}	39	GLB Register Hold Time after Clock	5.0	–	6.0	–	8.0	–	ns
t _{gco}	40	GLB Register Clock to Output Delay	–	2.1	–	2.5	–	3.3	ns
t _{gr}	41	GLB Register Reset to Output Delay	–	2.1	–	2.5	–	3.3	ns
t _{ptre}	42	GLB Product Term Reset to Register Delay	–	8.3	–	10.0	–	13.3	ns
t _{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	8.8	–	9.0	–	11.9	ns
t _{ptck}	44	GLB Product Term Clock Delay	2.9	6.3	3.5	7.5	4.6	9.9	ns
ORP									
t _{orp}	45	ORP Delay	–	3.2	–	3.5	–	4.7	ns
t _{orpbp}	46	ORP Bypass Delay	–	1.3	–	1.5	–	2.0	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

3. The XOR adjacent path can only be used by hard macros.

Table 2- 0036A-48/80,70,50.eps

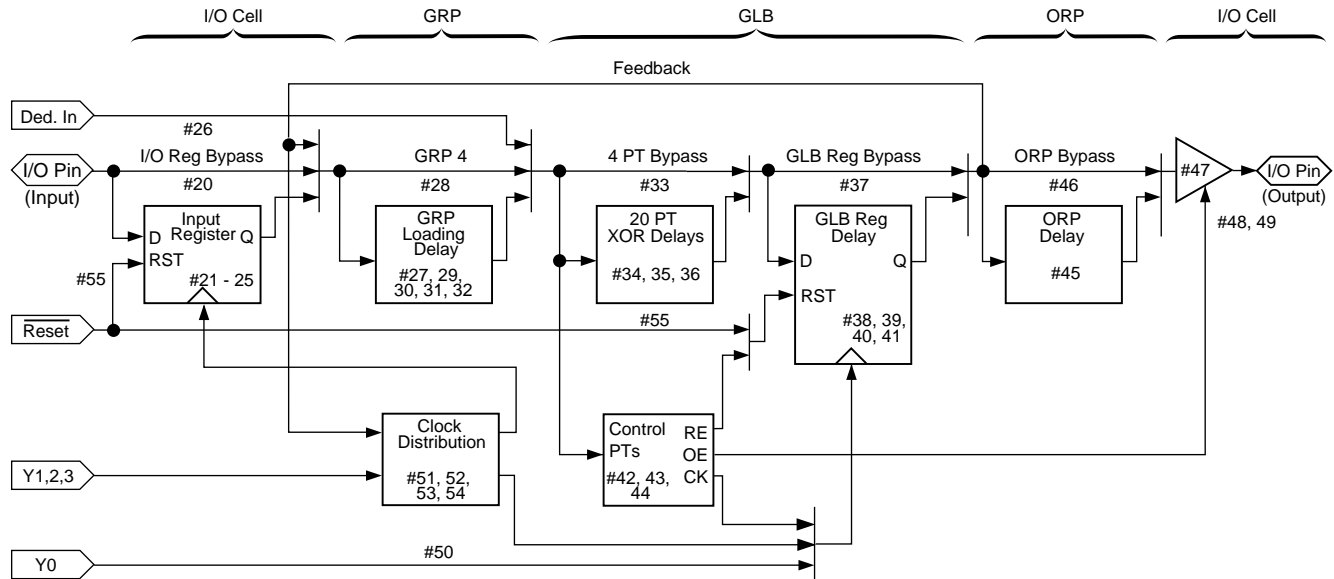
Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-80		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
tob	47	Output Buffer Delay	–	2.5	–	3.0	–	4.0	ns
toen	48	I/O Cell OE to Output Enabled	–	4.2	–	5.0	–	6.7	ns
todis	49	I/O Cell OE to Output Disabled	–	4.2	–	5.0	–	6.7	ns
Clocks									
tgy0	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.2	4.2	5.0	5.0	6.7	6.7	ns
tgy1/2	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.3	5.0	4.0	6.0	5.3	8.0	ns
tgcp	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.2	1.0	5.0	1.3	6.6	ns
tioy2/3	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.3	5.0	4.0	6.0	5.3	8.0	ns
tiocp	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.2	1.0	5.0	1.3	6.6	ns
Global Reset									
tgr	55	Global Reset to GLB and I/O Registers	–	9.2	–	8.0	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1048 Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

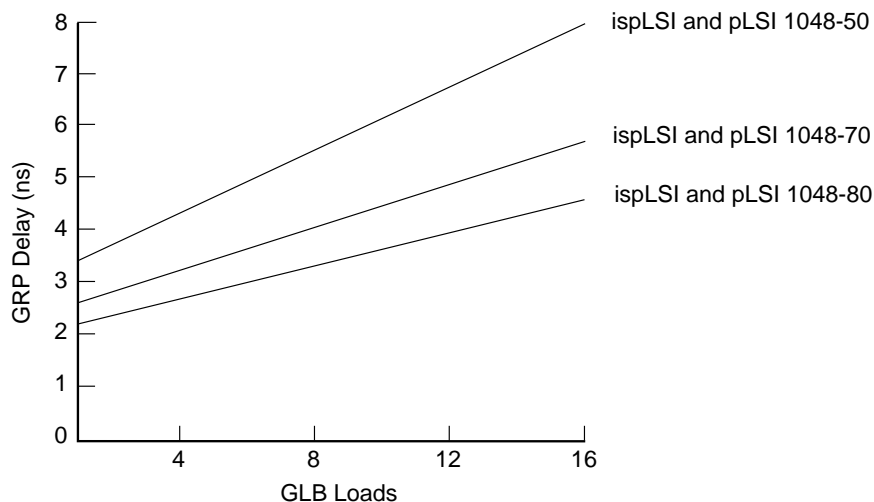
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 5.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (1.5) - (3.0 + 3.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 6.0 \text{ ns} &= (3.0 + 3.0 + 7.5) + (6.0) - (3.0 + 3.0 + 7.5) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 22.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (2.5) + (3.5 + 3.0)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 6.5 \text{ ns} &= (3.0 + 3.0 + 7.5) + (1.5) - (5.0 + 2.5 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 5.0 \text{ ns} &= (5.0 + 2.5 + 5.0) + (6.0) - (3.0 + 3.0 + 7.5) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 21.5 \text{ ns} &= (5.0 + 2.5 + 5.0) + (2.5) + (3.5 + 3.0)
 \end{aligned}$$

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1048-70.

Maximum GRP Delay vs GLB Loads

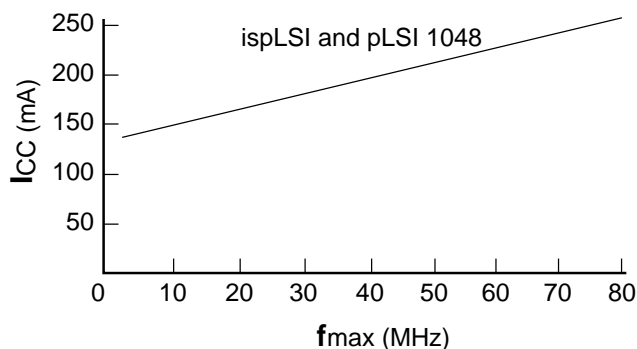


0126A-48-80-isp

Power Consumption

Power consumption in the ispLSI and pLSI 1048 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1048 using the following equation:

$$I_{CC} = 73 + (\# \text{ of PTs} \times 0.23) + (\# \text{ of nets} \times \text{Max. freq} \times 0.010) \text{ where:}$$

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions ($V_{CC} = 5.0V$, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-48-80-isp

In-System Programmability

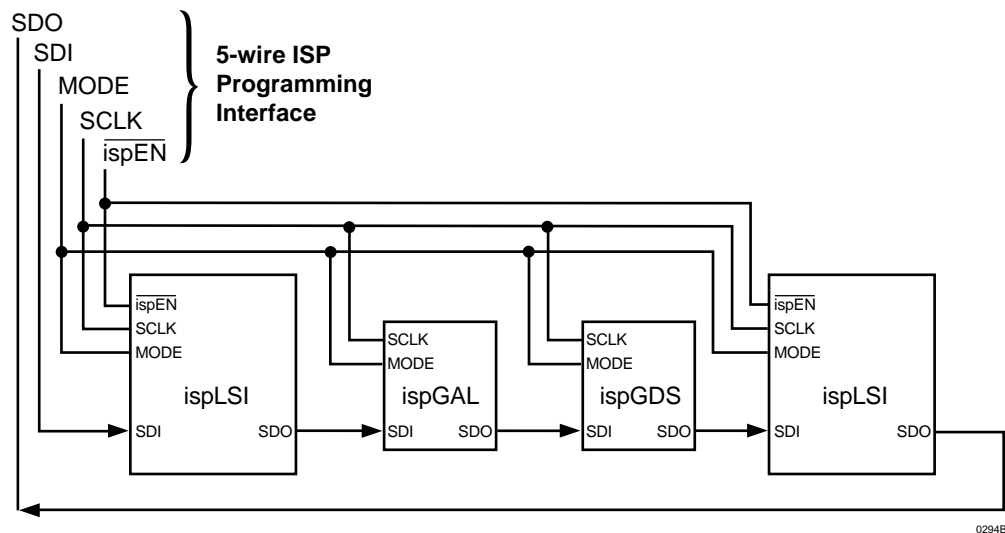
The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E²CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine

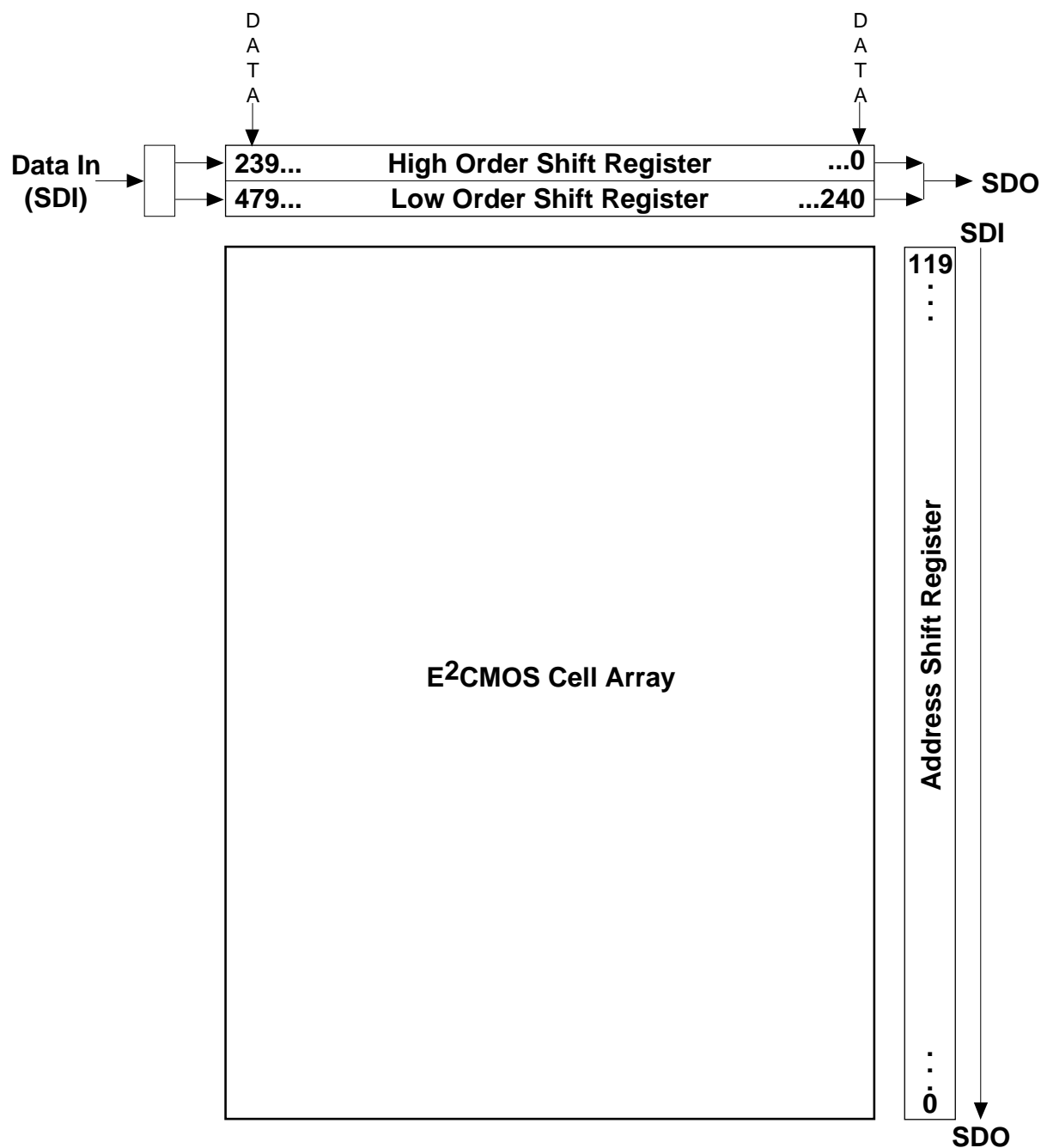
controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1048 is 0000 0100 (04 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1048 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification.
A logic "0" disables it.

Pin Description

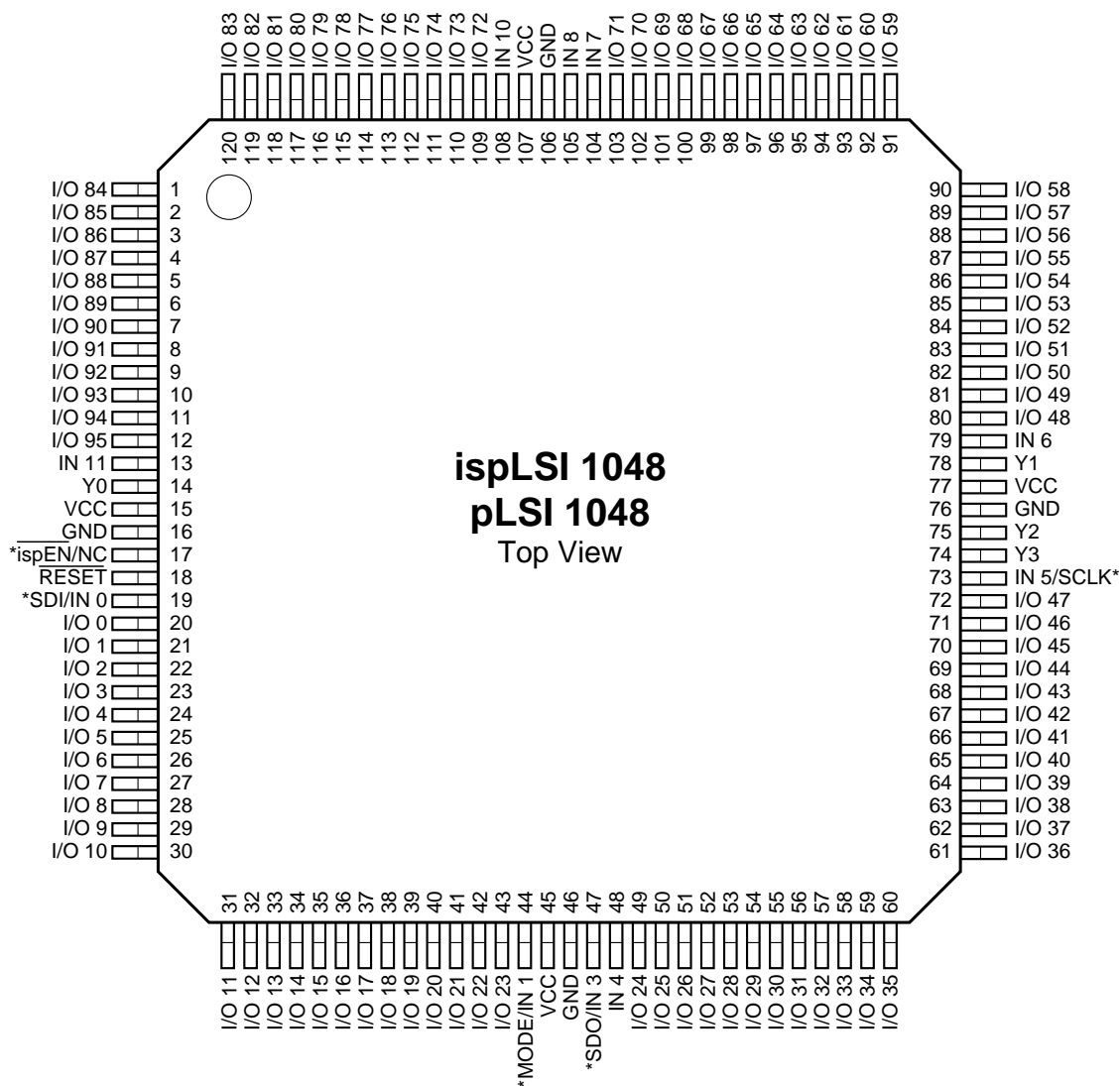
NAME	PQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 IN 6 - IN 11	48, 79, 104, 105, - 108, 13	Dedicated input pins to the device. (IN 2 and IN 9 not available)
$\overline{\text{ispEN}}^*/\text{NC}$ SDI [*] /IN 0 MODE [*] /IN 1 SDO [*] /IN 3 SCLK [*] /IN 5	17 19 44 47 73	<p>Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.</p> <p><u>Input</u> – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.</p> <p><u>Input</u> – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.</p> <p>Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.</p> <p><u>Input</u> – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.</p>
$\overline{\text{RESET}}$ Y0 Y1 Y2 Y3	18 14 78 75 74	<p>Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.</p> <p>Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.</p> <p>Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.</p> <p>Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.</p> <p>Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.</p>
GND VCC	46, 76, 106, 16 15, 45, 77, 107	Ground (GND) V _{CC}

*For ispLSI 1048 Only

Table 2- 0002C-48-isp

Pin Configuration

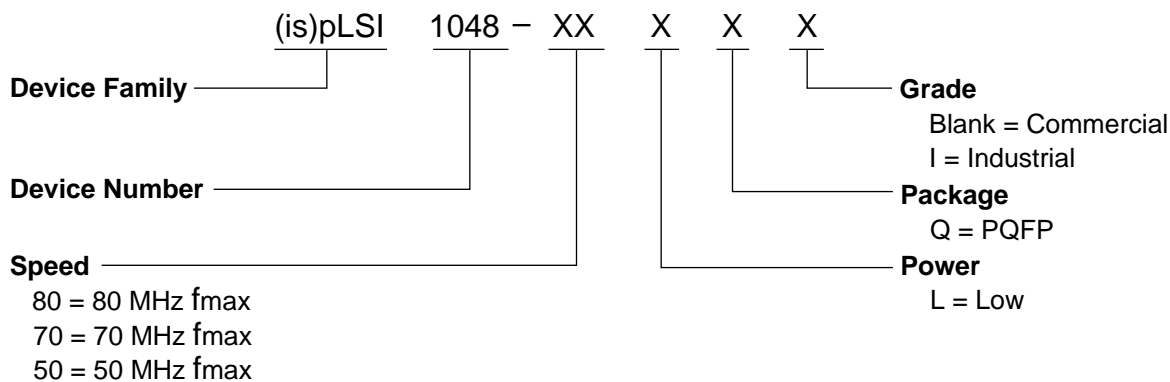
ispLSI and pLSI 1048 120-Pin PQFP Pinout Diagram



* Pins have dual function capability for ispLSI 1048 only (except pin 17, which is $\overline{\text{ispEN}}$ only).

0124 -48-isp

Part Number Description



0212-80B-isp1048

ispLSI and pLSI 1048 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
ispLSI	80	15	ispLSI 1048-80LQ	120-Pin PQFP
	70	18	ispLSI 1048-70LQ	120-Pin PQFP
	50	24	ispLSI 1048-50LQ	120-Pin PQFP
pLSI	80	15	pLSI 1048-80LQ	120-Pin PQFP
	70	18	pLSI 1048-70LQ	120-Pin PQFP
	50	24	pLSI 1048-50LQ	120-Pin PQFP

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
ispLSI	50	24	ispLSI 1048-50LQI	120-Pin PQFP
pLSI	50	24	pLSI 1048-50LQI	120-Pin PQFP

Table 2- 0041A-48-isp



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