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## Appendices

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1.0 General Description
A special F3856 PSU with a Keyboard Display Monitor (KDM) and a Debug monitor (KD-BUG) has been
developed by Fairchild to provide the F8 user with a convenient and powerful programming debug facility
to aid in the development of F8 programs. The debugging portion of the program (FAIR-BUG) provides
the user with an interactive system via a teletype terminal. The KDM segment provides a simple
alternative to an expensive terminal. FAIR-BUG and KDM will be discussed as separate subjects.

The KD-BUG PSU is assigned memory addresses '8000'-'87FF', with entry point being '8080'. The port
assignments are as follows:

| I/O Port A  | '08' |
| I/O Port B  | '09' |
| Local Int. Control | '0A' |
| Timer       | '0B' |

The Interrupt address vector for the timer is '0024' and for an External Interrupt is '00A4'.

1.1 Electrical Specifications
The dc and ac electrical characteristics of the F3856 PSU are, since this is just a standard PSU with a
special program on it, identical to those described in the F3856 PSU data sheet.

2.0 FAIR-BUG Overview
FAIR-BUG provides the following capabilities:

Display or Alter Memory Locations
Display or Alter Scratchpad Registers
Display or Alter I/O Ports
Display or Alter Accumulator, ISAR, Status (W Register)
Display or Alter PC0, DC0, DC1
Load Formatted Paper Tape (FAIR-BUG or Formulator Format)
Punch Formatted Paper Tape (Formulator Format)
Punch Paper Tape in PROM Format (4-Bit or 8-Bit Binary Format)
Entry from Keyboard or by Program Instruction
I/O Subroutines Available to User
Breakpoint
Block Memory Move
Hexadecimal Arithmetic

FAIR-BUG can be entered in several ways. Execution of program instructions such as PI '8080'; JMP
'8080'; LR P0, Q, or PK (Q or K contains '8080') can be used to achieve entry from another software
module. Another technique is to use hardware to decode the RESET state on the ROMC lines and force
the high order bit on the Data Bus to a '1' at this time.

FAIR-BUG will save the state of the machine upon entry and will restore it upon return to the users
program. Register 8 and PC1 are destroyed by FAIR-BUG; however, under program control the user can
save and restore these if necessary. The save area utilized by FAIR-BUG is scratchpad registers 3C to 3F
and also the last 26 bytes of user RAM. FAIR-BUG tests locations BDF-BFF and if there is RAM there, it
uses these locations for its save area; if it finds that these locations are not RAM, it assumes that locations
3DF-3FF of user memory are RAM and thus uses these locations for its save area. The interrupt is disabled
by FAIR-BUG and may be re-enabled by the user if desired.
Two I/O ports (8 and 9) are available to the user when FAIR-BUG is not executing, as is the Timer and External Interrupt facilities (FAIR-BUG does not use either of these). During FAIR-BUG execution Port 8 is used for serial input/output and control functions while Port 9 is used for parallel input from a high-speed paper tape reader. Assignments for Port 8 are: (1 = GND, 0 = +5 V).

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Serial input (0 Volts = MARK)</td>
</tr>
<tr>
<td>6</td>
<td>Character Ready Input (Parallel Device) (+5 V = READY)</td>
</tr>
<tr>
<td>5</td>
<td>Enter Key/Display Monitor</td>
</tr>
<tr>
<td>4</td>
<td>Device Ready Input (Parallel Device) (+5 V = READY)</td>
</tr>
<tr>
<td>3</td>
<td>Step Reader Output (Parallel Device) (0 Volts = Step)</td>
</tr>
<tr>
<td>2-1</td>
<td><strong>Bit 2 Bit 1 Baud Rate</strong></td>
</tr>
<tr>
<td></td>
<td>0 0 110 Baud for Serial Input/Output</td>
</tr>
<tr>
<td></td>
<td>0 1 300 Baud for Serial Input/Output</td>
</tr>
<tr>
<td></td>
<td>1 0 1200 Baud for Serial Input/Output</td>
</tr>
<tr>
<td></td>
<td>1 1 Baud Delay Counter in Memory Loc. 3FF (or BFF)</td>
</tr>
<tr>
<td>0</td>
<td>Serial Output (0 Volts = MARK)</td>
</tr>
</tbody>
</table>

If Port 9 is not utilized by FAIR-BUG, then Pins 3, 4, and 6 of Port 8 are also available to the user. If Port 9 is used for parallel input, the parallel input data should have logic '1' correspond to +5 V electrical level.

Bits 1 and 2 of Port 8 are examined when FAIR-BUG is entered to initialize the Baud Delay Counter. If Bits 2 and 3 are at ground so that the Baud Delay count is being obtained from memory location 3FF (or BFF), then the total delay count (time between bits for a bit serial I/O device) can be adjusted as follows:

\[
\text{Bit time interval} = (256 - \text{count}) \cdot 36 \, \mu\text{s} + 55 \, \mu\text{s} \quad (\Phi = 2 \, \text{MHz})
\]

Thus, 110 Baud requires a count of 06
300 Baud requires a count of A4
1200 Baud requires a count of EA

### 2.1 FAIR-BUG Commands

When FAIR-BUG is entered a prompt character (?) is sent to the output device. The user then has the option of using any of the debug commands. After each DEBUG execution the user is again prompted with (?). All data and input parameters are in hexadecimal notation. (C/R) following a command indicates a carriage return.

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>TYPE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>(C/R)</td>
<td>Display the contents of the Accumulator</td>
</tr>
<tr>
<td>D0</td>
<td>(C/R)</td>
<td>Display the contents of DC0</td>
</tr>
<tr>
<td>D1</td>
<td>(C/R)</td>
<td>Display the contents of DC1</td>
</tr>
<tr>
<td>I</td>
<td>(C/R)</td>
<td>Display the contents of ISAR</td>
</tr>
<tr>
<td>M XXXX</td>
<td>(C/R)</td>
<td>Display Memory Location XXXX</td>
</tr>
<tr>
<td>M XXXX-YYYY</td>
<td>(C/R)</td>
<td>Display Memory Location XXXX to YYYY</td>
</tr>
<tr>
<td>O XX</td>
<td>(C/R)</td>
<td>Display Port XX Data</td>
</tr>
<tr>
<td>P0</td>
<td>(C/R)</td>
<td>Display the contents of P0</td>
</tr>
<tr>
<td>R XX</td>
<td>(C/R)</td>
<td>Display the contents of Register XX</td>
</tr>
<tr>
<td>R XX-YY</td>
<td>(C/R)</td>
<td>Display the contents of Registers XX to YY</td>
</tr>
<tr>
<td>S</td>
<td>(C/R)</td>
<td>Display the contents of W Register, status</td>
</tr>
<tr>
<td>W</td>
<td>(C/R)</td>
<td>Display the contents of W Register, status</td>
</tr>
</tbody>
</table>
**COMMAND TYPE** | **COMMAND** | **FUNCTION (Continued)**
--- | --- | ---
Change | C XX (C/R) (C/R) | Change the previously displayed memory location or port or register to XX
| C XX (C/R) YY (C/R) | Change the sequential registers or memory locations to XX, YY...
| C XXXX (C/R) (C/R) | Change the previously displayed PC or DC to XXXX
Examine | E (C/R) | Display the last addressed register or memory location or port
Next | N (C/R) | Display the next register or memory location or port
Load | L (C/R) | Load formatted object paper tape. If (CK) prints, then checksum error has occurred on block last read
| H (C/R) | Load formatted object paper tape from high-speed reader
Hexadecimal | X aaaa ± bbbb = | Add or subtract value bbbb from value aaaa
Block Move | M dddd (C/R) | Move memory block starting at ssss and ending at address eee to memory destination address dddd
| V ssss-eeee (C/R) | Punch | B XXXX-YYYY-Z | Binary Punch PROM format; XXXX is starting page address and YYYY is ending page address. Z is number of bytes per block; 0 = 256, 1 = 512. To Punch 0 to BFF then enter B0-C00-0. 4-bit wide data.
| J XXXX-YYYY-Z | Same as B, except 8-bit wide data.
| F XXXX-YYYY (C/R) | Formatted punch for future load, Formulator format.
Go To | G (C/R) | Go to address of PCO
| G AAAA (C/R) | Change PCO to address AAAA, then go to AAAA and continue execution
Delete Command | [ | Delete command and start a new command input string
Breakpoint | UAAAA (C/R) | Set breakpoint (PK instruction) at address AAAA.
| T (C/R) | Clear breakpoint, restore user instruction.

NOTE: Clear Breakpoint must be issued prior to any IO port display or change commands or else instruction at AAAA will be incorrect.

**2.2 FAIR-BUG Command Usage**
A brief study of Appendix B will assist the reader in understanding FAIR-BUG command utilization. From these examples many advantages over console debugging are quite apparent. First and most important a history is recorded of the steps taken and the results displayed. Second is the accessability of the scratchpad registers as well as the other working registers of the system. Third is the simple access from the console to FAIR-BUG to the user.

One advantage that is not so apparent is that when a user wishes to end a debug session the user may save his modified program by punching the memory using the F command. In a subsequent debug session he may then load this "updated" program and continue to debug. If program patches were extensive much time and effort is saved. Of course the program may be re-assembled after editing the changes in order to obtain an updated program.

Another advantage and also not so apparent is the fact that Keyboard input is much less error prone. If the user uses a little care and examines his keyed input prior to the carriage return he can almost totally eliminate key-in errors. In addition, a debug session achieves more results in a quicker time.

**2.3 FAIR-BUG Input/Output**
The FAIR-BUG input/output routines assume that Port 8 of the PSU is available and is configured as shown in Appendix A. In order to communicate with FAIR-BUG an 11-bit serial type device such as a Teletype ASR 33 or compatible type TTY or CRT is required. FAIR-BUG has options to vary the Baud Rate by changing the counters for delay loops between bits. The timer is not utilized so the user is not deprived of this valuable resource. The counter value for 110 Baud is six which counts by incrementing an 8-bit register until zero; the six gives a loop count of 250. For 300 Baud the counter is initially H'A4' giving a loop
count of H'5C' or 92 decimal. Other Baud Rates can be achieved by modifying the counter. These counts assumed a system clock of 2 MHz. For a faster clock, the counter must be changed to produce more delay loops, while for a slower clock the counter must be changed to produce less delay loops. This is due to the fact that each instruction time will change and the total loop time will change while the device speed is always constant.

When the Baud Rate is not set to default to either 110 or 300 or 1200 then the Baud Rate must be put into RAM location H'BFF' or if this location is a PROM address then into RAM location H'3FF'.

2.4 Load from Parallel Input Device
The loader in FAIR-BUG can load from either a teletype or from a parallel source. The usual parallel source would be a high-speed paper tape reader which reads 100 to 300 characters per second. The parallel device is controlled using a “handshaking” protocol. The handshaking eliminates synchronizing problems because it forces the device to wait for the microprocessor and forces the microprocessor to wait for the device.

---

**FIGURE 1**
FAIR-BUG parallel read routine examines DEVICE READY and waits for the ready signal, it then looks for Character Ready and delays 100 μs after detecting the ready, then it reads a character before the output of Step Reader. This sequence is repeated for each character. Only the formats shown in Appendix C can be read by FAIR-BUG with the Load command. However, the user may use the subroutine PINP to read other formats. Bits 1-2 are examined when FAIR-BUG is entered to initialize the baud delay counter. See Appendix A for the I/O port pin assignments. The flow chart in Figure 1 indicates the steps necessary to load a paper tape program formatted as shown in Appendix C.

2.5 FAIR-BUG Subroutines

I/O Subroutines on the FAIR-BUG PSU are available to the user. These are listed below and documented in Appendix E.

<table>
<thead>
<tr>
<th>NAME</th>
<th>ENTRY ADDRESS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTY1</td>
<td>8553</td>
<td>Input 1 byte from TTY type device (11 bits serial/character)</td>
</tr>
<tr>
<td>TTY0</td>
<td>8593</td>
<td>Output 1 byte to TTY type device (11 bits serial/character)</td>
</tr>
<tr>
<td>TTCR</td>
<td>8578</td>
<td>Output CR, LF, &amp; 4 Null characters using TTY1 subroutine</td>
</tr>
<tr>
<td>PINP</td>
<td>853D</td>
<td>Input 1 byte from the parallel IP device (150μsec minimum delay between characters)</td>
</tr>
<tr>
<td>F0P1</td>
<td>811B</td>
<td>Output 1 or 2 hexadecimal digits in ASCII format from a memory location.</td>
</tr>
<tr>
<td>F0P2</td>
<td>811D</td>
<td>Output 1 or 2 hexadecimal digits in ASCII format from register QL.</td>
</tr>
<tr>
<td>BYTE</td>
<td>8515</td>
<td>Input 2 ASCII digits from a parallel or serial IP device; then convert them to one hexadecimal byte</td>
</tr>
</tbody>
</table>

2.6 Programming Examples

The following program linkages to FAIR-BUG are cited as examples as how to utilize FAIR-BUG as a "snap shot" display or breakpoint vehicle.

There are two general ways to enter FAIR-BUG; either through programmed instructions, or by manual intervention from the console. The manual entry is normally used for the following situations:

For initial program loading
For program punch and save
To start tracing a runaway program
To display or take further action following a BR*

The procedure to manually enter FAIR-BUG is to HALT, set DEBUG switch, push RESTART, then respond to prompt (?) with desired commands.

Programmed entry to FAIR-BUG can be achieved by building trace routines into the source program prior to assembly or else by patching the object program after loading it. In either case the following instructions provide the necessary linkage.
JMP H'8080  This is a 3 byte instruction that destroys the accumulator and does not save the program counter.

PI H'8080'  This is a 3 byte instruction that destroys the accumulator and pushes the program counter (PC0) to the stack (PC1).

LR P0,Q  This is a 1 byte instruction that does not destroy the accumulator and does not save the program counter.

PK  This is a 1 byte instruction that does not destroy the accumulator and pushes the program counter (PC0) to the stack (PC1)

These instructions are explained in detail in the F8 USERS GUIDE. It should be noted that all except the PI are priviledged instructions and that an interrupt cannot be serviced following these instructions. Furthermore, the first instruction executed at H'8080' is a disable interrupt which inhibits interrupts until an Enable instruction is issued.

Examination of these instructions discloses that the PK instruction is the most desirable to use since it is 1 byte, saves the accumulator, and saves the PC0; however, it does require the K register (R12 and R13) be preset. If K is not used in the program being tested this is an ideal instruction. A recommended procedure is to code into the users program at location 0 the following instructions:

```
LI H'80'
LR KU, A
LR KL, A
```

or

```
LI H'80'
LR QU, A
LR QL, A
```

If one of the above housekeeping procedures are used patching the user's program for tracing or display purpose becomes an easier proposition. Instead of using a 2 byte BR* or 3 byte JMP or PI the simpler PK or LR P0,Q may be used and the prompt (?) will indicate that a desired point has been reached. Display of PC1 will then determine which (if more than one) of the trace points has been reached. The disadvantage of using PK or PI is that the object program PC1 has been lost. If this is detrimental for a particular section of code being debugged the JMP or LR P0,Q instructions are available.

It can be noted that the options are numerous and the user must decide for himself which one or which combination is most desirable for his purpose.

It is suggested that the user try a small program as shown in Appendix B and utilize all the options of FAIR-BUG until he feels confident that he understands all the options. This will save much time and effort in future debug sessions.

3.0 Keyboard and Display Monitor (KDM)
The Keyboard and Display Monitor (KDM) is a program that allows the use of a keyboard and display unit in conjunction with any F8 kit or microprocessor system that has I/O Ports 0 and 1 for use by the KDM. The keyboard and display are shown below and the schematic diagram in Appendix F.

The reset to FAIR-BUG switch enters a save routine which saves PC0, DC0, DC1, ACC, R0-R7, and R9-R15 in RAM as shown in Appendix A. After the save, Port 8 bit 5 is examined. If this pin is tied to Vss then control goes to KDM. If this pin is left open then the FAIR-BUG monitor is in control.
KDM can now display or change any of the saved values or any other part of RAM memory. To restore these registers, prior to continuing execution of a program, the restore and continue subroutine must be executed. This is done by go to H'80E7'. The ISAR and status register will be destroyed. R16-R47 (decimal notation) will be unaltered.

3.1 Keyboard Instructions

0-9 and A-F Keys: When KDM is first entered the system will be in the addressing mode with zeros in the address display and the contents of memory location H'0000' in the data display. Use of any of these keys when in the addressing mode will cause the corresponding hex digit to be entered into the address display.

The data display will show the contents of the address being displayed. A maximum of four digits can be entered. If the system is in the store mode (see store mode key), then a maximum of two digits can be entered into the data display.

Store Mode Key
This key will cause the system to change from addressing mode to store mode or from store mode to addressing mode. When the system is in store mode the decimal point to the right of the right most display digit will be lit.

Enter Key
When in addressing mode this key will terminate digit entry so that a new address can be entered, if desired. When in store mode this key will cause the digits that were entered into the data display from the keyboard to be stored in the memory location indicated by the address display. The address display will then be automatically incremented by one.

Increment Address Key
Each depression of this key will increment the address display by one. If held down for more than 1.5 seconds the address display will increment continuously. This key will operate in both addressing and store modes.
**Decrement Address Key**
Similar to increment key except that the address will be decremented.

**Move Up Key**
This key will operate in store mode only. It will cause the contents of all memory locations between the presently addressed location and the next higher XXFF location to be moved one memory location higher in address. The previous contents of the location just after XXFF will be lost. A NOP (2B) will be inserted in the presently addressed location.

**Move Down Key**
This key will operate in store mode only. It will cause the contents of all memory locations between the presently addressed location plus one and the next higher XX00 location to be moved one memory location lower in address. The previous contents of the presently addressed location will be lost.

**Go Key**
This key will cause a jump to the memory location contained in the address display.

**Clear Key**
This key allows for the clearance of any hex digit entries that have not yet been followed by a function key.

**Reset Key**
If the toggle switch is in run position, this key will cause a jump to "0000" address. If the toggle switch is in the debug position, the reset will cause a jump to the beginning of the FAIR-BUG program and the state of the machine will be saved according to the rules of FAIR-BUG. At this point Bit 5 of the Port 8 (Pin 36 of the F3856) is examined. If it is found to be at VSS the program will jump to the KDM program. Otherwise, it will stay in FAIR-BUG.

**3.2 Subroutines**
There are three subroutines in the KDM program that can be utilized by a user's program:

- Keyboard Read (Scan)
- Display (Disp)
- Song Generation (Song)

**Scan**
A subroutine that allows the user to use the keyboard as input device is available at address H'8731'. The following sequence of instructions is a suggested way of using the subroutine:

```
KDB   PI      H'8731'
LI     H'FF'
XS      0
BNZ    KBD    BRANCH IF KEY STILL DOWN
LOOP   PI      H'8731'
LI     H'FF'
XS      0
BZ      LOOP   BRANCH IF NO KEYS
```

The above routine assures that a key has been released before accepting a new key. An H'FF' in register 0 indicates that no key was detected. Otherwise register 0 will contain a number corresponding to the keys in the following manner:
<table>
<thead>
<tr>
<th>KEY</th>
<th>REG 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-F</td>
<td>0-F</td>
</tr>
<tr>
<td>DA</td>
<td>10</td>
</tr>
<tr>
<td>ENT</td>
<td>11</td>
</tr>
<tr>
<td>IA</td>
<td>12</td>
</tr>
<tr>
<td>MOVE UP</td>
<td>13</td>
</tr>
<tr>
<td>MOVE DOWN</td>
<td>14</td>
</tr>
<tr>
<td>STM</td>
<td>15</td>
</tr>
<tr>
<td>GO</td>
<td>16</td>
</tr>
<tr>
<td>CLEAR</td>
<td>17</td>
</tr>
<tr>
<td>NO KEY</td>
<td>FF</td>
</tr>
</tbody>
</table>

The registers used by this subroutine are PC1, R0, R12, R13 and R48-R63. This subroutine also uses the display subroutine which takes the right hand four bit digits from R48-R53 and outputs them to the display, MSD to LSD respectively.

**Disp**
The display routine will display the six digits located in R48-R53.

ADDRESS:   H'8799'
ENTER:     R48-R53 (O'60'-O'65') DATA TO DISPLAY
EXIT:      R54-R55 (O'66'-O'67') DESTROYED

**Song**
A song generation subroutine can be utilized which outputs and audio signal (square wave) on Bit 6 of Port 8.

Load the note time value and pitch constants into memory in the following format:

```
DATA DC TIME VALUE CONSTANT (1)
DC PITCH CONSTANT (1)
::
DC TIME VALUE CONSTANT (n)
DC PITCH CONSTANT (n)
DC 0
```

ADDRESS:   H'87BE'
ENTER:     R7 TEMPO VALUE
            DC0 START OF DATA VALUES
EXIT:      R1-R9 DESTROYED
### PITCH VALUES

<table>
<thead>
<tr>
<th>Note</th>
<th>Hex Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>REST</td>
<td>7F</td>
</tr>
<tr>
<td>G₁</td>
<td>7E</td>
</tr>
<tr>
<td>G₂#</td>
<td>77</td>
</tr>
<tr>
<td>A₁</td>
<td>70</td>
</tr>
<tr>
<td>A₂#</td>
<td>6A</td>
</tr>
<tr>
<td>B₁</td>
<td>64</td>
</tr>
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<td>C</td>
<td>5E</td>
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<td>F</td>
<td>46</td>
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<td>1E</td>
</tr>
<tr>
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<td>1C</td>
</tr>
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<td>1A</td>
</tr>
<tr>
<td>A'#$</td>
<td>18</td>
</tr>
<tr>
<td>B'</td>
<td>17</td>
</tr>
<tr>
<td>C₂</td>
<td>16</td>
</tr>
</tbody>
</table>

### TEMPO VALUES

<table>
<thead>
<tr>
<th>BPM</th>
<th>Register 7 Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>6</td>
</tr>
<tr>
<td>48</td>
<td>5</td>
</tr>
<tr>
<td>60</td>
<td>4</td>
</tr>
<tr>
<td>80</td>
<td>3</td>
</tr>
<tr>
<td>120</td>
<td>2</td>
</tr>
<tr>
<td>240</td>
<td>1</td>
</tr>
</tbody>
</table>

### TIME VALUE

<table>
<thead>
<tr>
<th>Time Value of Note or Rest</th>
<th>Hex Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>20</td>
</tr>
<tr>
<td>.</td>
<td>18</td>
</tr>
<tr>
<td>.</td>
<td>10</td>
</tr>
<tr>
<td>.</td>
<td>C</td>
</tr>
<tr>
<td>.</td>
<td>8</td>
</tr>
<tr>
<td>.</td>
<td>6</td>
</tr>
<tr>
<td>.</td>
<td>4</td>
</tr>
<tr>
<td>.</td>
<td>3</td>
</tr>
<tr>
<td>.</td>
<td>2</td>
</tr>
</tbody>
</table>
APPENDIX A

FAIR-BUG PORTS ASSIGNMENT AND MEMORY UTILIZATION

ASSIGNMENTS FOR PORT 8

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Serial input</td>
</tr>
<tr>
<td>6</td>
<td>Character Ready (Parallel Device)</td>
</tr>
<tr>
<td>5</td>
<td>Enter Key/Display Monitor</td>
</tr>
<tr>
<td>4</td>
<td>Device Ready (Parallel Device)</td>
</tr>
<tr>
<td>3</td>
<td>Step Reader (Parallel Device)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2</th>
<th>bit 1</th>
<th>Baud Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>110 baud</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>300 baud</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1200 baud</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Baud delay counter in memory at “3FF” or “BFF”</td>
</tr>
</tbody>
</table>

Note: 0 = +5; 1 = GND, 0 V.

0        Serial Output

MAP OF FAIR-BUG MEMORY USE

RAM

<table>
<thead>
<tr>
<th>Address</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0XD8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0XC0</td>
<td>Work 2</td>
<td>Work 3</td>
<td>Work 3</td>
<td>Work 4</td>
<td>Work 5</td>
<td>Work 7</td>
<td>Work 8</td>
</tr>
<tr>
<td>0XE8</td>
<td>PCOL</td>
<td>PC1U</td>
<td>PC1L</td>
<td>DC0U</td>
<td>DCOL</td>
<td>DC1U</td>
<td>DC1L</td>
</tr>
<tr>
<td>0XF0</td>
<td>R1</td>
<td>R2</td>
<td>R3</td>
<td>R4</td>
<td>R5</td>
<td>R6</td>
<td>R7</td>
</tr>
<tr>
<td>0XF8</td>
<td>R9</td>
<td>R10</td>
<td>R11</td>
<td>R12</td>
<td>R13</td>
<td>R14</td>
<td>R15</td>
</tr>
</tbody>
</table>

NOTE: X = B or 3. If H'BEB' is RAM then H'BDF' to H'BFF' will be used as save area.
If H'BEB' is not RAM then H'3DF' to H'3FF' will be used as the save area.

NOTE: Work 1-8 is used to save:
1. Breakpoint address and user instruction.
2. Sequence of instructions to execute Outs, Out, Ins, or In sequence for Port Display or Change.

MAP OF FAIR-BUG SCRATCHPAD USE

Scratchpad

<table>
<thead>
<tr>
<th>Address</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3C-3F</td>
<td>Work A</td>
<td>Status</td>
<td>Work B</td>
</tr>
</tbody>
</table>

NOTE: Work A & B are used during the entry and exit routines of FAIRBUG when saving or restoring the state of the user’s program.
APPENDIX B
FAIR-BUG EXAMPLE 1

\[
\begin{align*}
\text{?M0} & \quad \text{M0000 = 00} \\
\text{?C 70 (CR) (CR)} & \\
\text{?NM0001 = 91} & \\
\text{?C0B (CR) (CR)} & \\
\text{?NM0002 = 00} & \\
\text{?C 5C (CR) (CR)} & \\
\text{?NM0003 = DD} & \\
\text{?C 1F (CR) (CR)} & \\
\text{?NM0004 = 04} & \\
\text{?C25 (CR) 3F (CR) 94 (CR) (CR)} & \\
\text{?CF9 (CR) 29 (CR) 80 (CR) (CR)} & \\
\text{?C80 (CR) (CR)} & \\
\text{?M0-A} & \\
\text{M0000 = 70 0B 5C 1F 25 3F 94 F9} \\
\text{M0008 = 29 80 80 D0 00 10 00 91} & \\
\text{?R0-3F} & \\
\text{R0000 = A4 FF 09 FF 00 00 FF 00} & \\
\text{R0008 = 83 0A 00 FF 81 97 03 FF} & \\
\text{R0010 = 0C 20 13 00 1E 00 BF 00} & \\
\text{R0018 = 9D 40 7D 01 DD 17 55 00} & \\
\text{R0020 = B7 F7 7F A2 FF 0E FF 22} & \\
\text{R0028 = FF 76 FF 3C FF CE 5F 20} & \\
\text{R0030 = 18 04 02 00 D9 04 7F 00} & \\
\text{R0038 = 75 01 57 4A 0F 0A 0A FF} & \\
\text{?G0} & \\
\text{(Program loop err.) Manual reset to FAIR-BUG} & \\
\text{?M7} & \\
\text{M0007 = F9} & \\
\text{?C FA} & \\
\text{?G0} & \\
\text{?R0-3F} & \\
\text{R0000 = 00 01 02 03 04 05 06 07} & \\
\text{R0008 = 80 09 0A 0B 0C DD 0E 0F} & \\
\text{R0010 = 10 11 12 13 14 15 16 17} & \\
\text{R0018 = 18 19 1A 1B 1C 1D 1E 1F} & \\
\text{R0020 = 20 21 22 23 24 25 26 27} & \\
\text{R0028 = 28 29 2A 2B 2C 2D 2E 2F} & \\
\text{R0030 = 30 31 32 33 34 35 36 37} & \\
\text{R0038 = 38 39 3A 3B 3E 09 09 0B} & \\
\text{?P0 0000} & \\
\text{?PI EEEE} & \\
\text{?M8} & \\
\text{M0008 = 29} & \\
\text{C28} & \\
\text{?G0} & \\
\text{?P0 000B} & \\
\text{?} & \\
\text{\{\) Store a Program to Set} & \\
\text{\{\) Scratchpad to 0-3F. Note two methods to store} & \\
\text{\{\) data in memory. The same} & \\
\text{\{\) may be done with} & \\
\text{\{\) registers also.} & \\
\text{\{\) LOOP} & \\
\text{\{\) LIS 0} & \\
\text{\{\) LR IS, A} & \\
\text{\{\) LR S,A} & \\
\text{\{\) INC} & \\
\text{\{\) CI H'3F} & \\
\text{\{\) BNZ LOOP} & \\
\text{\{\) JMP H'8080'} & \\
\text{\} Display Program} & \\
\text{\} Display Scratchpad} & \\
\text{\} Before Execution} & \\
\text{\} Go to loc 0 to Execute} & \\
\text{\} Correct BNZ Instruction} & \\
\text{\} Go to 0} & \\
\text{\} Display Registers after} & \\
\text{\} Execution.} & \\
\text{\} Note: R8, R3C-3F are used} & \\
\text{\} by FAIR-BUG} & \\
\text{\} PCO not saved by JMP} & \\
\text{\} Change JMP to PI} & \\
\text{\} Execute Again} & \\
\text{\} PCO Now saved!} & \\
\end{align*}
\]
FAIR-BUG EXAMPLE 1

R1-2 Types R0-R7
Next = R8
Change R8 to 55
Examine R8

Display DC1, Change, Examine,
Then Display Again
ISAR
Status
Memory Dump
Register Dump
Register Dump
Note: R40-R47 is Actually R0-R7

Punch Format (PROM Tape)
See Appendix D for Format

Formulator
Punch
Format
See
Appendix C

Display, Change, Examine Accumulator
NOTE: Accumulator is in R8 Therefore Next is R9
Go to 8080

PC0 Changed to 8080
Go to PC0 (8080)
APPENDIX C
FORMATTED TAPE
(FAIRBUG FORMAT)

Note: This example was loaded (L) by the instruction shown in Appendix B. This is ASCII 7 bit format.
APPENDIX C (Continued)
FORMATTED TAPE
(FORMULATOR FORMAT)

Start Block
Data Block Length
Address 1st Data Byte
Code

Data
Checksum

Length = 0 15 End
Next Available Address
Code
Checksum

Start Next Block
FAIRBUG FORMAT AND CHECKSUM

The following line of code is from Appendix C. The checksum is the sum of all the nibbles in the block.

```
X009100DD041000D17
```

<table>
<thead>
<tr>
<th>Data</th>
<th>Checksum</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
</tr>
</tbody>
</table>

7 = Checksum

FORMULATOR FORMAT AND CHECKSUM

The following line of code is from example 2. The checksum is the 2's complement of the sum of all the bytes in the record. Notice that when the checksum is also added to the sum the total is always zero for the low 16 bits.

```
:1800E80126C802F3268164FB20D900FF24F900F926F900FF2ED92EF5C1
```

```
<table>
<thead>
<tr>
<th>Data</th>
<th>Checksum</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Code, Type of record</td>
<td></td>
</tr>
<tr>
<td>Starting Address</td>
<td></td>
</tr>
<tr>
<td>Number of Data Bytes, H'18' = 24</td>
<td></td>
</tr>
</tbody>
</table>
```

```
| 18   | 26   | 24   | 2E   | E3   |
| 00   | 81   | F9   | D9   | FE   |
| E8   | 64   | 00   | 2E   | 34   |
| 00   | FB   | F9   | F5   | 2A   |
|      | 26   | 20   | 26   |      |
| C8   | D9   | F9   | 2A   |      |
| 02   | 00   | 00   |      |      |
| F3   | FF   | FF   |      |      |
|      |      |      |      |      |
| E3   | FE   | 34   |      |      |
```

\[3F = \text{Total Sum}\]

\[2's \text{ Complement} (3F + 1 = C1)\]
APPENDIX D
BINARY FORMAT
(PROM GENERATION FORMAT)

Note: This example was punched by the instruction shown in Appendix B. The first block is punched with 256 memory locations (high order bits). The next block has 256 memory locations (low order bits). Subsequent blocks then alternate high, low, high, low, etc. with a blank gap between. Only the low order 4 bits are significant and are punched in complement form. The table below shows examples of commands and the results produced.

<table>
<thead>
<tr>
<th>Input Command</th>
<th>Decimal Memory Addresses Punched</th>
<th># Blocks</th>
<th>Block Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>B 0-100-0</td>
<td>0-255</td>
<td>2</td>
<td>256</td>
</tr>
<tr>
<td>B 0-400-0</td>
<td>0-1023</td>
<td>8</td>
<td>256</td>
</tr>
<tr>
<td>B 100-200-0</td>
<td>256-511</td>
<td>2</td>
<td>256</td>
</tr>
<tr>
<td>B 0-400-1</td>
<td>0-1023</td>
<td>4</td>
<td>512</td>
</tr>
<tr>
<td>B 0-1000-1</td>
<td>0-4095</td>
<td>16</td>
<td>512</td>
</tr>
<tr>
<td>B 200-400-1</td>
<td>512-1023</td>
<td>2</td>
<td>512</td>
</tr>
</tbody>
</table>

PROM 8 BIT FORMAT

- Start Block

This format is 8 bits wide and is punched by: JXX00-YY00-L when: J0-100-0 it will punch data from Memory Address 0 to H'FF'.
L = 0 -256 bytes
L = 1 -512 bytes
L = 3 -1024 bytes

Data
APPENDIX E
FAIR-BUG SUBROUTINES

The following INPUT and OUTPUT subroutines exist in FAIR-BUG and should be called by the users program. All subroutines should be entered by: (PI Address).

TTY1 — Input 1 byte from TTY type device, without echo. Data is 11 bits/character being received on Port 8 Pin 7.

Address: H'8553'
Enter: R0 — Delay Counter
Exit: W Reg — Destroyed
      PC1 — User return address
      Accum — Input byte
      R0 — Unchanged
      R1 — Input byte
      R2 — -1

TTY0 — Output 1 byte to TTY type device. Data transmitted is 11 bits/character being output on Port 8 Pin 0.

Address: H'8593'
Enter: R0 — Delay Counter
      R1 — Byte to output
Exit: W Reg — Destroyed
      PC1 — User return address
      Accum — 0
      R0 — Unchanged
      R1 — -1
      R2 — 0

TTCR — Output CR/LF/NUL to TTY type device; subroutine TTY0 is called.

Address: H'8578'
Enter: R0 — Delay Counter
Exit: W Reg — Destroyed
      PC1 —
      Accum — 0
      K Reg — User return address
      R0 — Unchanged
      R1 — -1
      R2 — 0

PINP — Input 1 byte from parallel input device; minimum delay between characters is 150μs. Byte is received on Port 9 with control bits on Port 8, pins 3, 4, and 6.

Address: H'853D'
Enter: No setup
Exit: W Reg — Destroyed
      PC1 — User return address
      Accum — Input byte
      R1 — Input byte
BYTE — Input 2 ASCII hexadecimal characters and convert to 1 byte; also accumulate the checksum. If input is not ASCII characters 0-9 or A-F meaningless results will be returned. Either TTYI or PINP is called as input routine.

Address: H'8515'
Enter: Q — H'853D' (for parallel input)
     Q — H'8553' (serial input) RO = Delay Counter
     R7 — Previously accumulated checksum
Exit: W Reg — Destroyed
      PC1 — Destroyed
      Accum — Input byte
      K — User return address
      Q — Unchanged
      R0 — Unchanged
      R1 — Destroyed
      R2 — -1 (if serial IP), unchanged for parallel IP
      R7 — Checksum
      R8 — 0
      R11 — Input byte

F0P1 — Output byte of data from memory to TTY type device using TTY0 subroutine. Byte is converted to 1 or 2 ASCII hexidecimal characters.

Address: H'811B'
Enter: R0 — Delay Counter
      R8 — Flag Pos# = 0P Hi 4 bits, then Lo 4 as ASCII
      Neg# = 0P Lo 4 bits as ASCII
      DC0 — Memory address of data
Exit: W Reg — Destroyed
      PC1 — Destroyed
      Accum — Destroyed
      DC0 — DC0 + 1
      K Reg — User return address
      QL — Data byte
      R0 — Unchanged
      R1 — -1
      R2 — 0
      R7 — Checksum (low 4 bits significant)

F0P2 — Output byte of data from QL. Same routine as F0P1 except DC0 is not used.

Address: H'811D'
Enter: R0 — Delay Counter
      R8 — Same as F0P1
      QL — Data byte to output
Exit: Same as F0P1
APPENDIX F (Continued)

PARTS DESCRIPTION

Q1, Q2, Q3  9N04  HEX Inverter
Q5, Q7  2N2222  NPN Transistor
Q8 - Q13  9368  7 Segment Decoding Latch
Q4  9308  Dual 4 bit latch
D1 - D6  FND500  7 Segment LED Display
D7 - D14  FLV110  LED Lamps
Q6  2N3638  PNP Transistor
D16 - D21  1N461  Diode
D15  1N4001  Diode

PINOUT DESCRIPTION

P86  Output Pin for Song
P07  Output Blanking Signal
P06  Output Signal for Decimal Point
P00 - P05  Output Signal for Digit Select
P14 - P17  Input Signals, Keyboard Read
P10 - P13  Output Signals, Digit to Display

NOTE: P86 Designates Port 8, Bit 6.

APPENDIX G

ASCII CHARACTER CODES

<table>
<thead>
<tr>
<th>Character</th>
<th>7 Bit Hex Code</th>
<th>Character</th>
<th>7 Bit Hex Code</th>
<th>Character</th>
<th>7 Bit Hex Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Space)</td>
<td>20</td>
<td>0</td>
<td>30</td>
<td>H</td>
<td>48</td>
</tr>
<tr>
<td>!</td>
<td>21</td>
<td>1</td>
<td>31</td>
<td>I</td>
<td>49</td>
</tr>
<tr>
<td>&quot;</td>
<td>22</td>
<td>2</td>
<td>32</td>
<td>J</td>
<td>4A</td>
</tr>
<tr>
<td>#</td>
<td>23</td>
<td>3</td>
<td>33</td>
<td>K</td>
<td>4B</td>
</tr>
<tr>
<td>$</td>
<td>24</td>
<td>4</td>
<td>34</td>
<td>L</td>
<td>4C</td>
</tr>
<tr>
<td>%</td>
<td>25</td>
<td>5</td>
<td>35</td>
<td>M</td>
<td>4D</td>
</tr>
<tr>
<td>&amp;</td>
<td>26</td>
<td>6</td>
<td>36</td>
<td>N</td>
<td>4E</td>
</tr>
<tr>
<td>' (Quote)</td>
<td>27</td>
<td>7</td>
<td>37</td>
<td>O</td>
<td>4F</td>
</tr>
<tr>
<td>(</td>
<td>28</td>
<td>8</td>
<td>38</td>
<td>P</td>
<td>50</td>
</tr>
<tr>
<td>)</td>
<td>29</td>
<td>9</td>
<td>39</td>
<td>Q</td>
<td>51</td>
</tr>
<tr>
<td>*</td>
<td>2A</td>
<td>:)</td>
<td>3A</td>
<td>R</td>
<td>52</td>
</tr>
<tr>
<td>+</td>
<td>2B</td>
<td>;)</td>
<td>3B</td>
<td>S</td>
<td>53</td>
</tr>
<tr>
<td>, (Comma)</td>
<td>2C</td>
<td>&gt;</td>
<td>3C</td>
<td>T</td>
<td>54</td>
</tr>
<tr>
<td>-</td>
<td>2D</td>
<td>=</td>
<td>3D</td>
<td>U</td>
<td>55</td>
</tr>
<tr>
<td>.</td>
<td>2E</td>
<td>&lt;</td>
<td>3E</td>
<td>V</td>
<td>56</td>
</tr>
<tr>
<td>/</td>
<td>2F</td>
<td>?</td>
<td>3F</td>
<td>W</td>
<td>57</td>
</tr>
<tr>
<td>Line Feed</td>
<td>0A</td>
<td>@</td>
<td>40</td>
<td>X</td>
<td>58</td>
</tr>
<tr>
<td>Carriage RTN</td>
<td>0D</td>
<td>A</td>
<td>41</td>
<td>Y</td>
<td>59</td>
</tr>
<tr>
<td>Bell</td>
<td>87</td>
<td>B</td>
<td>42</td>
<td>Z</td>
<td>5A</td>
</tr>
<tr>
<td>Punch ON</td>
<td>92</td>
<td>C</td>
<td>43</td>
<td>[</td>
<td>5B</td>
</tr>
<tr>
<td>Punch OFF</td>
<td>94</td>
<td>D</td>
<td>44</td>
<td>\</td>
<td>5C</td>
</tr>
<tr>
<td>Reader ON</td>
<td>91</td>
<td>E</td>
<td>45</td>
<td>)</td>
<td>5D</td>
</tr>
<tr>
<td>Reader OFF</td>
<td>93</td>
<td>F</td>
<td>46</td>
<td>1</td>
<td>5E</td>
</tr>
<tr>
<td>Null</td>
<td>7F</td>
<td>G</td>
<td>47</td>
<td>←</td>
<td>5F</td>
</tr>
<tr>
<td>Null</td>
<td>FF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERRS</td>
<td>LOC</td>
<td>OBJECT</td>
<td>ADDR LINE</td>
<td>SOURCE</td>
<td>STATEMENT</td>
</tr>
<tr>
<td>------</td>
<td>-----</td>
<td>--------</td>
<td>-----------</td>
<td>--------</td>
<td>-----------</td>
</tr>
<tr>
<td>0001</td>
<td>*FAIRBUG</td>
<td>+</td>
<td>EDUCATOR</td>
<td>J.EFSTATHIOU</td>
<td></td>
</tr>
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FORMULATOR ASSEMBLER (REV 3.0)

ERRS LDC OBJECT ADDR LINE SOURCE STATEMENT

8066 1E 0184 LR J+I STATUS TO R9
80B7 4A 0185 LR A+10
8088 5D 0186 LR I+10 R10 TO R76
8089 4B 0187 LR A+11
808A 5C 0188 LR S+A R11 TO R77
808B 11 0189 LR H+DC DC TO R 10-11
808C 2A00EB 0EB 0191 DCI MH1 CHECK ADDRESS OF SCRATCH RAM
808F 16 0192 LM
80C0 18 0193 CON
80C1 2A00EB 0EB 0194 DCI MH1
80C4 17 0195 ST WRITE COMPLEMENT
80C5 2A01EB 0EB 0196 DCI MH1
80C8 8C 0197 XM XDR SHOULD BE Z
80C9 2A01EB 0EB 0198 DCI MH1
80CC 8404 8D01 0199 BZ BG1 IF ZERO SCRATCH
80CD 2A03EB 0EB 0200 DCI MLD NOT 4K CRATCH M
80D1 4A 0201 BG1 LR A+10
80D2 17 0202 ST
80D3 4B 0203 LR A+11
80D4 17 0204 ST DC NOW IN RAM
80D5 2C 0205 XDC
80D6 11 0206 LR H+DC DC1
80D7 2C 0207 XDC
80D8 4A 0208 LR A+10
80D9 17 0209 ST DC1 UPPER
80DA 4B 0210 LR A+11
80DB 17 0211 ST DC1 LOWER
80DD 4E 0212 LR A+D
80DE 5B 0213 LR 11,A RESTORE R11
80DF 4C 0214 LR A+S
80E0 5A 0215 LR 10,A RESTORE 10
80E1 49 0216 LR A+9
80E2 5E 0217 LR B+9
80E3 5A 0218 LR A+S
80E4 59 0219 LR +A
80E4 298000 8000 0220 JMP BSL1 TO FINISH SAVE
80E7 80E7 0221 \* RESTORE ROUTINE RESET REGISTERS THEN RE
80EF 07 0233 LR QU,A DC TO R14
80F0 16 0234 LM
80F1 16 0235 LR 0L,A DC TO R15
80F2 16 0236 XDC
80F3 16 0237 LR DC,O DC0 RESTORE
80F4 16 0238 XDC
80F5 07 0239 LM
80F6 2C 0240 LR QU,A
80F7 16 0241 LM
80F8 2C 0242 LR 0L,A DC1 NOW IN O
80FD 70 0243 LIS 0
8044 \*LOOP TO RESTORE R0-R13 FROM SCRATCH RAM
APPENDIX H (Continued)

FORMULATOR ASSEMBLER (REV 3.0)

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FORMULATOR ASSEMBLER (REV 3.0)

ERRS LOC OBJECT ADDR LINE SOURCE STATEMENT

81B 0B 0306 LR IS:A ISAR=3
81C 7B 0307 FA LIS 4
81D 5B 0308 LR CC:A CHAR CNT=4
*READ CHARACTER
81E 288553 8553 0310 FB PI TTYI GET CHAR
81F 217F 0311 NI H'??'F'
820 57 0312 LR 7,A
821 250D 0313 CI CR
822 843E 8185 0314 BZ CORE CORRECT FIELD B
823 288593 8593 0315 PI TTYD ECHO INPUT CHAR
824 87 0316 LR A,7
825 252D 0317 CI C'-' FIELD SEPARATOR
826 8433 8182 0318 BZ CORN
827 842F 0319 CI C'+'
828 843D 0321 CI C'='
829 8430 8187 0322 BZ CORT
82A 855B 0323 CI H'SB' KILL CHAR?
82B 8478 81D3 0324 BZ STR1 KILL INPUT
*MUST BE HEX 0-9, OR A-F
82C 252F 0326 CI H'2F' LESS THAN ZERO
82D 81DF 813E 0327 BP FB ERROR IGNORE
82E 8146 0328 CI H'46' F?
82F 810B 813E 0329 BM FB ERROR IGNORE
830 2400 0330 AI H'D0'
831 2509 0331 CI H'9'
832 8107 8170 0332 BP FOK
833 8151 0333 CI H'10'
834 81DF 813E 0334 BP FB ERROR+IGNORE IT
835 24F9 0335 AI H'F9'
836 83B 0336 FOK DS CC
837 811C 813E 0337 BM FB FULL FIELD IGNORE
*ZERO LO 4 BITS, THEN ADD THIS DIGIT
838 52 0339 LR 2,A
839 4C 0340 LR A,S
840 15 0341 SL 4
841 2C 0342 AS 2
842 5D 0343 LR I,A TO PARAMETER LO
843 71 0344 LIS 1
844 FB 0345 NS CC
845 84C3 813E 0346 BZ FB EVEN CHAR, 2 DIG
846 4E 0347 LR A,D SET ISAR BACK 1
847 8FC0 813E 0348 BR7 FB GET NEXT DIGIT
848 73 0349 LIS 3
849 9035 81B6 0350 BR COR7 PARAMETERS FULL
850 59 0351 CORN LR 9,A
851 9003 8187 0352 BR CORT
*CORRECT HEX FIELD, RIGHT JUSTIFY
852 7D 0353 CORE LIS H'I'
853 57 0359 LR 7,A
854 74 0360 CORT LIS 4
855 EB 0361 XS CC
856 814F 81A9 0362 BZ COR6 NO PARAMETERS
857 83B 0363 DS CC
858 911B 81A8 0364 BM COR5 FIELD ABCD, ADK
859 940C 819B 0365 BNZ COR1
860 7F 0366 LIS 15

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## APPENDIX H (Continued)

FORMULATOR ASSEMBLER (REV 3.0)

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*ROUTINE TO FETCH DIRECTIVE, THEN CALL PARAME

* THEN GO TO CORRECT PROCESS ROUTINE THRU

| 81B9 | 01  | 0400   | TBLSC| DC   | AL1(AI-A) ACCUMULATOR DIS |
|      |     |        |      | DC   | AL1(B-A) BINARY DUMP     |
| 81BA | 9E  | 0401   |      | DC   | AL1(C-A) CHANGE FIELD    |
| 81BB | 06  | 0402   |      | DC   | AL1(D-A) DC DISPLAY      |
| 81BC | 42  | 0403   |      | DC   | AL1(E-A) EXAMINE         |
| 81BD | 47  | 0404   |      | DC   | AL1(F-A) FORMATTED PUNCH |
| 81BE | 4D  | 0405   |      | DC   | AL1(G-A) GO TO           |
| 81BF | 5D  | 0406   |      | DC   | AL1(H-A) HIGH SPEED LOAD |
| 81C0 | 6A  | 0407   |      | DC   | AL1(I-A) ISAR DISPLAY    |
| 81C1 | 5F  | 0408   |      | DC   | AL1(J-A) 8 BIT PROM PUNC |
| 81C2 | A2  | 0409   |      | DC   | AL1(K-A) K               |
| 81C3 | FF  | 0410   |      | DC   | AL1(L-A) LOAD            |
| 81C4 | 70  | 0411   |      | DC   | AL1(M-A) MEMORY DISPLAY  |
| 81C5 | 73  | 0412   |      | DC   | AL1(N-A) NEXT DISPLAY    |
| 81C6 | 76  | 0413   | 4C   | DC   | AL1(O-A) PORT DISPLAY    |
| 81C7 | 6D  | 0414   |      | DC   | AL1(P-A) PC DISPLAY      |
| 81C8 | 82  | 0415   |      | DC   | AL1(q-A) q               |
| 81C9 | FF  | 0416   |      | DC   | AL1(r-A) REGISTER DISPLA |
| 81CA | A8  | 0417   |      | DC   | AL1(s-A) STATUS DISPLAY  |
| 81CB | 9A  | 0418   |      | DC   | AL1(t-A) CLEAR POI      |
| 81CC | 04  | 0419   |      | DC   | AL1(u-A) BREAKPOINT     |
| 81CD | A5  | 0420   |      | DC   | AL1(v-A) MOVE BLOCK     |
| 81CE | FC  | 0421   |      | DC   | AL1(w-A) W (STATUS) DISP |
| 81CF | 9A  | 0422   |      | DC   | AL1(x-A) HEX ARITHMETIC |
| 81D0 | 02  | 0423   | HXX  | DC   | AL1(x-A) HEX ARITHMETIC |
| 81D1 | 4B  | 0424   | STRT | LR   | A,11 FREE R11          |
| 81D2 | 07  | 0425   | LR   | OL,A|                  |
| 81D3 | 888578| 8578   | 0426 | STR1 | PI TTRR WRITE CR/LF   |
| 81D6 | 203F| 0427   | LI   | C'1' | PROMPT CHARACTERE      |
APPENDIX H (Continued)

FORMULATOR ASSEMBLER (REV 3.0)

ERRS  LOC  OBJECT  ADDR  LINE  SOURCE STATEMENT

81D8  51  0428  LR  CHRS,A
81D9  288593  8593  0429  PI  TTYO
     *READ INPUT CHARACTER
81DC  288553  8553  0430  READ  PI  TTYI
81DF  53  0432  LR  3,A  SAVE CHAR
81E0  288593  8593  0433  PI  TTYO  ECHO CHAR
81E3  43  0434  LR  A+3
81E4  217F  0435  NI  H'7F'  7 BITS ONLY
81E6  2540  0436  CI  H'40'
81E8  81EA  81D3  0437  BP  STR1  LESS THAN 'A' I
81EA  2558  0438  CI  C'X'
81EC  91E6  81D3  0439  BM  STR1  GREATER THAN 'W
81EE  211F  0440  NI  H'1F'  SAVE 5 BITS ONL
81F0  2881B8  81B8  0441  DCI  (TBL-1)
81F3  8E  0442  ADC
81F4  16  0443  LM  GET TABLE VALUE
81F5  05  0444  RPTC  LR  KL,A  SAVE INDEX IN R
81F6  1F  0445  INC  SET STATUS
81F7  84DB  81D3  0446  BZ  STR1  INVALID CONTROL
     *NOW INPUT PARAMETERS IF ANY
81F9  298139  8139  0447  JMP  FECH
81FC  03  0448  RTN  LR  A,QL
81FD  5B  0449  LR  11,A  RESTORE R11
     *MAKE LO ADDRESS START ON 8 BYTE BOUNDARY
     *MAKE HI ADDRESS END ON 8 BYTE BOUNDARY
81FE  72  0450  LIS  2
81FF  F8  0451  NS  FCNT
8200  8418  8219  0452  BZ  RTN1  NOT 2 OR 3 PARA
8202  01  0453  LR  A,KL
8203  2502  0454  CI  (X-A)
8205  9404  820A  0455  BNZ  NHX
8207  29829A  829A  0456  JMP  HEX
820A  25F8  0457  CI  (V-A)
820C  8417  8224  0458  BM  MOVE
820E  46  0459  LR  A,6
820F  2207  0460  DI  7
8211  56  0461  LR  6,A
8212  20F8  0462  LI  H'F8'
8214  F4  0463  NS  4
8215  54  0464  LR  4,A
8216  5B  0465  LR  11,A
8217  43  0466  LR  A,3
8218  5A  0467  LR  10,A
     *CALC ADDRESS TO GET TO PROCESS ROUTINE
8219  01  0468  RTN1  LR  A,KL
821A  24B9  0469  AI  LODY  LO 8 BIT ADDRESS
821C  05  0470  LR  KL,A
821D  2082  0471  LI  HIBY  HI 8 BIT ADDRESS
821F  19  0472  LNK
8220  04  0473  LR  KU,A
8221  09  0474  LR  P,K
8222  02  0475  LR  A,GU  HI ADDRESS IF N
8223  1C  0476  POP
     *MOVE MEMORY BLOCK
8224  F2  0477  AI  LOBY  LO 8 BIT ADDRESS
8225  92  0478  LR  KL,A
8226  2082  0479  LI  HIBY  HI 8 BIT ADDRESS
8228  13  0480  LR  KU,A
8229  09  0481  LR  P,K
822A  02  0482  LR  A,GU  HI ADDRESS IF N

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<td>0491</td>
<td>+  R10-11 =CURRENT SOURCE BYTE ADDRESS</td>
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**NOTE:** The above text contains assembly code. The assembly language used is typical for a specific computer architecture, which might not be universally recognized. The code is structured to load, store, and manipulate data, with comments indicating the purpose of certain segments of the code.
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### APPENDIX H (Continued)

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BNZ    CONT
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H'3F'    MASK TO SIX BIT
H'D0'    ASCII CONVERT--
BC    4     CARRY IF IT WAS
H'39'    FINISH CONVERS
AI    CKSM MAKE THE COMPAR
SL    4     LO 4 BITS TO HI
BZ    IDLE  IF OK, LET'S GE
IN    E1    SETA PI  BYTE   GET NEW LOAD AD
    P1    BYTE
    LR    10A
    PI    BYTE
    LR    11A
    LR    DC+H  SET THE ADDRES
    BR    IDLE  ENDX NS  XFLG  HAVE AN *, BUT
    BZ    IDLE  MUST BE ONLY AT
    EZ    IDLE  WAS 2A+0 OR 2A

******  HALT LOOP FOR WHEN FINISHED  ******
    STPP  H'93'  READER OFF COMM
    LR    CHRS,A  PASS
    SLF3  JMP    PLXX  SLF3
NDF    LIR    0
FORM   LIS    0
    LR    CKSM,A  ZERO CKSM TO START
    CM    XFLG,A
    LR    LENGTH OF BLOCK
    PI    BYTE
    XS    CCNT
    NS    CCNT
    BI    STPP  ZERO RECORD IS
    PI    BYTE  ADDRESS HI
    LR    10A
    PI    BYTE  ADDRESS LO
    LR    11A
    LR    DC+H
    PI    BYTE  CODE BYTE
    NS    CHR1
    BZ    IDLE  NOT DATA RECORD
    NS    CHR1
    NF    DATA
    BR    IDLE
    P1    BYTE  DATA FETCH
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A28
## APPENDIX H (Continued)

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**PORT CHANGE ROUTINE**

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### GET A BYTE

1085 **GET A BYTE**

1086 **GETS THE BYTE, CONVERTS, AND ADDS TO**

1087 **SAVE PC1**

8515 08 1086 BYTE LR K,P

8516 72 1087 LI 2

8517 58 1088 LR HFLG,A SET THE HALF FL

8518 4B | 1089 AGAN LR A,CHR1

8519 15 | 1090 SL 4

851A 5B | 1091 LR CHR1,A

851B | 28853C 1092 PI CHAR

851E | 213F 1093 | NI | H'3F' MASK TO 6 BITS

8520 24D0 | 1094 AI H'DO' ASCII CONVERT--

8522 | 8203 1095 BC **4

8524 | 2439 1096 AI H'39' NEXT CLEAN UP A

8526 | CB | 1097 AS CHR1

8527 | 5B | 1098 LR CHR1,A TEMP STORE

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A29
**APPENDIX H (Continued)**

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FORMULATOR ASSEMBLER (REV 3.0)

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8599 BB 1197
859A BB 1198
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859D 94FA 8598 1201
859F 32 1202
85A0 9402 85A3 1203
85A2 1C 1204
85A3 71 1205
85A4 FA 1206
85A5 BB 1207
85A6 41 1208
85A7 12 1209
85A9 2480 1210
85AA 51 1211
85AB 90EB 8597 1212
85AD 70 1213
85AE 52 1214
85AF 207F 1220

8578 08 TIOC LR K,P
8579 7D LISR CR
857A 51 LR CHRS,A
857B 288593 8593 PI TTYD
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8592 0C PK RETURN
8593 7B TTYD LISR H'0B'
8594 52 LR BCT,A SET BIT COUNT F
8595 70 LISR 0
8596 BB OUTS OPOR OUTPUT START BI
8597 40 DLY1 LR A,BAUD GET DELAY COUNT
8598 BB DLY2 OUTS MUSE NOP FOR DELAY
8599 BB OUTS MUSE
859A BB OUTS MUSE
859B 2401 AI H'01' INCX WITH A 5 U
859D 94FA 8598 DLY2 BNZ DLY5
859F 32 DZ BCT
85A0 9402 85A3 BNZ DLY5 NEXT BIT
85A2 1C POP ALL FINI,BACK T
85A3 71 LISR 1 GET CHARACTER
85A4 FA NS CHRS MASK OFF ALL BU
85A5 BB OUTS OPOR OUTPUT THE NEW
85A6 41 LR A,CHRS NOW SHIFT THE C
85A7 12 SR 1
85A9 2480 AI H'80' FILL,WITH 1'S F
85AA 51 LR CHRS,A
85AB 90EB 8597 EDUX BR DLY1 DELAY,THEN
85AD 70 1213
85AE 52 1214
85AF 207F 1220

85AD 70 EDUC LISR CLEAR INTERRUPT PORTS
85AE 52 LR 2,A CLEAR STORE MODE FLAG
85AF 207F LI H'7F'
APPENDIX H (Continued)

FORMULATOR ASSEMBLER (REV 3.0)

ERRS LOC OBJECT ADDR LINE SOURCE STATEMENT

25B1 B0 1221 OUTS 0
25B2 67 1222 LISU 7
25B3 68 1223 LISL 0
25B4 1F 1224 INC
25B5 5D 1225 LR I,A
25B6 02 1226 LR A+OU SAVE OU FOR RETURN TO FAI-
25B7 5E 1227 LR I,A
25B8 66 1228 * LOAD ZEROS INTO ADDRESS DISPLAY AND DC
25B9 5F 1229 A9 LISU 6
25BA 6B 1230 LISL 3
25BB 70 1231 LIS 0
25BC 5E 1232 A20 LR D,A
25BD 8FFE 85BB 1233 BR7 A20
25BE 74 1234 LIS 4
25BF 57 1235 LR 7,A
25C0 A0000 0000 1236 * LOAD MEMORY TO DATA DISPLAY
25C3 0E 1237 DCI 0
25C4 88713 8713 1239 PI MTDD
25C7 288731 8731 1240 * SCAN KEYBOARD
25CA 2012 1241 A3 PI SCAN
25CC E0 1242 LI H'12'
25CD 8417 85E5 1243 XS 0
25CF 24FE 1244 BZ A38 BRANCH IF IA KEY
25D1 8413 85E5 1245 AI H'FE' WAS IT H'10'?
25D2 76 1246 BZ A38 BRANCH IF DA KEY
25D4 56 1247 LIS 6
25D5 2020 1248 LR 6,A LOAD DELAY TIME FOR REPEAT
25D7 55 1249 LI H'20'
25D8 40 1250 LR 5,A LOAD FIRST DELAY TIME FOR RE
25DA 1F 1251 A0
25DB 94EC 85C7 1252 INC
25DC 288731 8731 1253 BNZ A3 BRANCH IF KEY STILL DOWN
25DF 40 1254 A5 PI SCAN
25E0 40 1255 LR A0
25E1 84FA 85DC 1256 INC
25E2 900E 85F2 1257 BZ A5 BRANCH IF NO KEYS
25E3 E5 1258 BR A54
25E5 5D 1259 A38 XS 5
25E6 8404 85EB 1260 BZ A53 BRANCH IF FIRST DELAY IS OV
25E8 35 1261 DS 5
25E9 90DD 85C7 1262 BR A3
25EA 36 1263 A53 DS 6
25EB 94DA 85C7 1264 BNZ A3 BRANCH IF DELAY TIME IS OVE
25EE 76 1265 LIS 6
25EF 56 1266 LR 6,A RELOAD DELAY TIME FOR REPEA
25F0 90EB 85DC 1267 BR A5
25F2 11 1268 * DETERMINE WHICH KEY WAS DETECTED
25F3 2010 1269 A54 LR H,DC
25F5 F0 1270 LI H'10'
25F6 9404 85FB 1271 NS 0
25F8 298697 8697 1273 JMP A27
25FB 2A860B 860B 1274 A6 DCI FUNC
25FE 7F 1275 LIS 15
25FF F0 1276 NS 0
2600 50 1277 LR 0,A
2601 8406 8608 1278 BZ A19
2603 73 1279 A4 LIS 3
2604 8E 1280 ADC
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A32
# APPENDIX H (Continued)

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APPENDIX H (Continued)

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8705 54  1471    LR  A, D
8706 4E  1472    LR  A, D
8707 15  1473    SL  4
8708 4E  1474    XS  4
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870C 04  1477    LR  KU, A
870D 0F  1478    LR  DC, O
870E 1C  1479    POP
870F 07  1480    A36    LR  0, A
8710 05  1481    LR  KL, A
8711 90F2 8704 1482    BR  A15
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8715 54  1488    LR  A, D
8716 14  1489    SR  4
8717 5D  1490    LR  1, A
8718 7F  1491    LIS  15
8719 F4  1492    MS  4
871A 5C  1493    LR  S, A
871B 1C  1494    POP
1495    *
1496    *    INCREMENT ADDRESS DISPLAY SUBROUTINE
1497    *
871C 6B  1498    IMAD LISR 3
871D 4C  1499    A21    LR  A, S
871E 1F  1500    INC
871F 15  1501    SL  4
8720 14  1502    SR  4
8721 5E  1503    LR  D, A
8722 9403 8726 1504    BNZ  A22    BRANCH IF DIGIT WAS NOT 'F'
8724 8FF8 871D 1505    BR7  A21    BRANCH IF NOT MSD
8726 1C  1506    A22    POP
1507    *
1508    *    DECREMENT ADDRESS DISPLAY SUBROUTINE
1509    *
8727 6B  1510    DEAD LISR 3
8728 3C  1511    A31    DS  S
8729 4C  1512    LR  A, S
872A 14  1513    SR  4
872B 8404 8730 1514    BZ  A32    BRANCH IF DIGIT WAS NOT ZERO
872D 5E  1515    LR  D, A    15 TO DISPLAY REG.
872E 8FF9 8728 1516    BR7  A31    BRANCH IF NOT MSD
8730 1C  1517    A32    POP
1518    *
1519    *    SCAN KEYBOARD SUBROUTINE
1520    *
8731 08  1521    SCAN LR  K, P
8732 0A  1522    LR  A, IS
8733 65  1523    LISU 5
8734 6F  1524    LISL 7
8735 5E  1525    LR  D, A
FORMULATOR ASSEMBLER (REV 3.0)

ERRS  LOC  OBJECT  ADDR  LINE  SOURCE STATEMENT

8736  2017  1527  A39  LI  H'17'
8738  50   1528  LR  0,a
8739  20FE  1529  *LOAD FIRST STROBE
873B  5C   1530  LI  H'FE'
873D  B1   1531  LR  S,a
873E  20C0  1532  *OUTPUT STROBE
873F  7F   1533  A40  LIS  15  BLANK DISPLAY
8740  B0   1534  DUTS 1
8741  4E   1535  LI  H'CO'
8744  3C   1536  DUTS 0
8747  8417  1537  LR  A,D
8748  B0   1538  DUTS 0
8749  30   1539  *READ KEYS
874A  74   1540  LIS  4
874C  5C   1541  LR  S,a
874D  14   1542  INS  1
874E  8417  1543  SR  4
874F  875F  1544  B2  A43  BRANCH IF NO KEY IN THIS CO
8750  15   1545  SL  4
8751  9108  1546  A41  BM  A42  BRANCH IF KEY IS IN THIS RO
8752  50   1547  *GO TO NEXT ROW IF NOT LAST ROW
8753  6C   1548  DS  0
8754  71   1549  DS  S
8755  EC   1550  B2  A47  BRANCH IF LAST ROW IN THIS
8756  9426  1551  SL  1
8757  877D  1552  BR  A41
8758  50   1553  *IS THIS FIRST SCAN
8759  4C   1554  A42  LISL 4
875A  71   1555  LSS  1
875B  5C   1556  XS  S
875C  9426  1557  BNZ  A4B  BRANCH IF KBD FLAG NOT SET
875D  877D  1558  *RESET KBD FLAG
875E  5E   1559  LR  D,a
8760  90F8  1560  *COMPARE TWO SCANS
8761  6C   1561  LR  S,a
8762  71   1562  XS  0
8763  50   1563  B2  A46  BRANCH IF SCANS ARE THE SAME
8764  90F8  1564  BR  A45
8765  6E   1565  *CHANGE KEY CODE FOR NEXT COLUMN
8766  8419  1566  A43  LISL 6
8767  20FC  1567  LI  H'FC'
8768  C0   1568  AS  0
8769  50   1569  LR  0,a
876A  4C   1570  *SHIFT STROBE ONE POSITION
876B  13   1571  A44  LR  A,S
876C  2301  1572  SL  1
876D  5C   1573  XI  1
876E  5C   1574  LR  S,a
876F  2140  1575  *HAS LAST COLUMN BEEN SCANNED ALREADY
8770  50   1576  MI  H'40'
8771  9400  1577  BNZ  A40  BRANCH IF NOT LAST STROBE
8772  873C  1578  *STORE 'FF' IN KEY CODE REGISTER
8773  20FF  1579  A45  LI  H'FF'
8774  50   1580  LR  0,a
8775  6C   1581  *RESET KBD FLAG
8776  7C   1582  LISL 4
8777  70   1583  LSS  0
8778  5C   1584  LR  S,a
8779  900C  1585  BR  A51
877A  50   1586  *RESTORE ISAR
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APPENDIX H (Continued)

87B0  13    1648  SL  1
87B5  56    1649  LR  0,A
87B6  8FF0  87A7  1650  BR ? A52
87B8  6E    1651  LSL 6.
87B9  4D    1652  LR  A,1
87BA  50    1653  LR  0,A  RESTORE REG. 0
87BB  4C    1654  LR  A,3
87BC  51    1655  LR  1,A  RESTORE REG. 1
87BD  1C    1656  POP
1657     +  SONG SUBROUTINE
1658     +  LOAD STARTING LOCATION OF SONG CONSTANT
1659     +  LOAD TEMPO INTO R7.
1660     +  LOAD TEMPO INTO R7.
1661     +
87BE  20040  1662  SONG LI H'40'
87C0  56    1663  LR  6,A  SET NOTE FLAG
87C1  47    1664  LR  A,7
87C2  55    1665  LR  5,A  STORE TEMPO CONSTANT IN WDR
87C3  16    1666  LM
87C4  54    1667  LR  4,A  STORE NOTE DURATION CONSTANT
87C5  51    1668  LR  1,A  RETAIN NOTE DURATION CONSTANT
87C6  F1    1669  NS  1
87C7  8437  87FF  1670  BZ  FINS  END OF SONG IF NOTE DURATION
87C9  16    1671  LM
87CA  53    1672  LR  3,A  RETAIN NOTE PITCH CONSTANT
87CB  237F  1673  XI H'7F'
87CD  9402  87D0  1674  BNZ A2  BRANCH IF NOT A REST
87CF  56    1675  LR  6,A  CLEAR NOTE FLAG
87D0  20FF  1676  A2  LI H'FF'
87D2  59    1677  LR  9,A  LOAD PITCH COUNTER A
87D3  76    1678  LSS  6
87D4  58    1679  LR  8,A  LOAD PITCH COUNTER B
87DE  50    1680  A55  LR  A,3
87D6  52    1681  LR  2,A  STORE NOTE PITCH CONSTANT
87D7  A8    1682  INS  8
87D9  E6    1683  XS  6
87DA  B8    1684  OUTS  8  TOGGLE OUTPUT PORT
87DB  39    1685  A11  DS  9
87DC  9404  87E0  1686  BNZ A8  BRANCH IF PITCH COUNTER A N
87DD  38    1687  DS  8
87DE  8406  87E5  1688  BZ A7  BRANCH IF PITCH COUNTER B I
87E0  32    1689  A8  DS  2  DECREMENT NOTE PITCH CONSTANT
87E1  81F8  87DA  1690  BP A11  BRANCH IF NOTE PITCH CONSTANT
87E3  9FF1  87D5  1691  BR A55  GO TO Toggling OF OUTPUT
87E5  32    1692  A7  DS  2  DEC. NOTE PITCH CONSTANT T
87E6  32    1693  DS  2
87E7  76    1694  LSS  6
87E8  58    1695  LR  3,A  RELOAD PITCH COUNTER B
87E9  34    1696  DS  4  DECREMENT NOTE DURATION CON
87EA  9408  87F3  1697  BNZ A10  BRANCH IF NOTE DURATION CON
87EC  41    1698  LR  A,1
87ED  54    1699  LR  4,A  RELOAD NOTE DURATION CONSTANT
87EE  35    1700  DS  5  DECREMENT TEMPO CONSTANT
87EF  94EA  87DA  1701  BNZ A11  BRANCH IF TEMPO CONSTANT NO
87F1  90CC  87BE  1702  BR SONG GO TO NEXT NOTE
87F3  71    1703  A10  LSS  1
87F4  E5    1704  XS  5
87F5  97E4  87DA  1705  BNZ A11  BRANCH IF TEMPO CONSTANT NO
87F7  32    1706  DS  2  DEC. NOTE PITCH CONSTANT T
87F8  71    1707  LSS  1
87F9  E4    1708  XS  4
87FA  94DF  87DA  1709  BNZ A11  BRANCH IF NOTE DURATION CON
87FC  56    1710  LR  6,A  CLEAR NOTE FLAG TO PROVIDE
87FD  90DC  87DA  1711  BR A11
87FF  1C    1712  FINS POP
1713    END