82C575 COMMUNICATION MICROCHANNEL™ INTERFACE CHIP

- Compatible with IBM Microchannel™ specifications
- Provides highly integrated Microchannel™ compatible interface solution for most communication adapter applications
- Suitable for most 8 bit slave IO peripheral applications
- Unique and flexible Card ID assignment
- Supports POS registers
- Four POS register bit outputs for system configuration
- Resource relocation capability to avoid address conflict
- Dual resource relocators to support multiple peripherals per card
- Sophisticated Card Channel Ready signal generator
- On chip system wait state generator
- Low power CMOS technology
- 68 pins PLCC package

The 82C575 is a highly integrated Microchannel™ compatible interface chip for use in personal computer applications compatible with the IBM PS/2 standard. It supports the Microchannel™ compatible interface to most of the 8 bit IO slave devices. The adapter IO address can be programmed during the setup procedure, this resource relocation capability avoids adapter address conflicts. The interrupt level can also be selected via software. The on-chip wait state generator allows the user to optimize the system bus timing to his/her specific needs. A unique Card ID generator does not require any external components.

All these features greatly simplify the design of a circuit to interface to the Microchannel™ compatible bus.

The 82C575 supports application markets such as intelligent Modems, SDLC/BISYNC/UART adapter card applications, instrumentation, etc. The dual resource relocater provides the capability to support multiple peripheral system with a maximum of 32 IO address space. The 82C575 is fabricated using advanced CMOS technology and is packaged in a 68 pin PLCC.

* IBM is a trademark of International Business Machine corporation.

Figure 1. 82C575 Functional Block Diagram
### 82C575 Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Type</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-68</td>
<td>I</td>
<td>ID0-5</td>
<td>Adapter Identification bits 0 to 7 for both low byte (Register 100) and high byte (Register 101). ID0 is the least significant bit (LSB) and ID7 is the most significant bit (MSB). The individual multiplexed ID bit can be tied to ( V_{CC} ), ( V_{SS} ), CTLA or CTLB according to the following table:</td>
</tr>
<tr>
<td>2-3</td>
<td>I</td>
<td>ID6-7</td>
<td>( V_{CC} ): If both high and low byte bits are &quot;1&quot;. ( V_{SS} ): If both high and low byte bits are &quot;0&quot;. CTLA: If high byte bit is &quot;0&quot; and low byte bit is &quot;1&quot;. CTLB: If high byte bit is &quot;1&quot; and low byte bit is &quot;0&quot;. The values of these pins are returned by executing a READ ID command during the adapter setup operation. The input buffers have internal pullup resistors. They can be left floating instead of being tied to ( V_{CC} ).</td>
</tr>
<tr>
<td>5-4</td>
<td>O</td>
<td>OUT0-1</td>
<td>Outputs from POS register 102 bits 1 to 4. They can be used as the general purpose control signals for the system configuration, such as interrupt level selection.</td>
</tr>
<tr>
<td>55-56</td>
<td>O</td>
<td>OUT2-3</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>I</td>
<td>RDYIN</td>
<td>Active high Ready Input from a slow IO device. For external asynchronous extended channel cycle operation, CDCHRDY goes inactive at the beginning of the cycle and stays inactive until a low to high transition is detected on RDYIN pin.</td>
</tr>
<tr>
<td>7</td>
<td>O</td>
<td>CDEN</td>
<td>Active high Card Enable. It is the output of POS register 102 bit 0.</td>
</tr>
<tr>
<td>8-11</td>
<td>O</td>
<td>AO3-0</td>
<td>Latched Address Output 3 to 0. These bits are latched by ADL and are used by the peripheral device to address the 82C575 internal registers.</td>
</tr>
<tr>
<td>12</td>
<td>O</td>
<td>IOWR</td>
<td>Active low IO write strobe. It is the decoded command from CPU to load the information into the the registers of the externally addressed IO slave device. It goes active only when the IO address matches the primary or secondary resource relocater address.</td>
</tr>
<tr>
<td>13</td>
<td>O</td>
<td>IORD</td>
<td>Active low IO read strobe. It is the decoded command from CPU to read the device registers. It goes active only when the IO address matches the primary or secondary resource relocater address.</td>
</tr>
<tr>
<td>14</td>
<td>O</td>
<td>BCS</td>
<td>Active low 74LS245 buffer chip enable. It goes active if the internal POS registers or external IO device is addressed. (Either read or write operation.)</td>
</tr>
<tr>
<td>15</td>
<td>O</td>
<td>BCTL</td>
<td>Active low external 74LS245 buffer transfer direction control signal. It becomes active during an IO READ operation if the POS registers or external IO device is addressed.</td>
</tr>
</tbody>
</table>
82C575 Pin Description (Continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Type</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>I</td>
<td>RESET</td>
<td>Active high hardware reset signal to initialize the chip. It should stay high for a minimum period of 500 ns.</td>
</tr>
<tr>
<td>17</td>
<td>B</td>
<td>D7</td>
<td>System data bits 7 to 0. These bits are used to transfer the data to and from the CPU data bus during the configuration cycle. They are 3-state bidirectional lines.</td>
</tr>
<tr>
<td>20-26</td>
<td>B</td>
<td>D6-0</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>O</td>
<td>CDSFBK</td>
<td>Active low Card Select Feedback. This signal goes active when an IO slave peripheral is addressed by the host. It stays inactive during a setup cycle.</td>
</tr>
<tr>
<td>28</td>
<td>O</td>
<td>CDCHRDY</td>
<td>Card Channel Ready. This signal is used by an external slow peripheral device to extend the channel cycle. During the setup operation, CDCHRDY always stays active and bus cycle is not extended. The maximum time CDCHRDY can stay inactive is 3 µs.</td>
</tr>
<tr>
<td>29</td>
<td>I</td>
<td>CMD</td>
<td>Active low Command signal to define when data is valid on the data bus. It is used to generate the IO/memory read and write commands and is also used to latch the status signals.</td>
</tr>
<tr>
<td>30</td>
<td>I</td>
<td>M/IO</td>
<td>Memory/Input Output. If M/IO is high, it indicates a memory cycle. If it is low, it indicates an IO cycle.</td>
</tr>
<tr>
<td>31</td>
<td>I</td>
<td>S1</td>
<td>Status bits 1 and 0. These signals indicate the start and the type of channel cycle. It is used with M/IO to generate the memory or IO read and write commands.</td>
</tr>
<tr>
<td>32</td>
<td>I</td>
<td>S0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>M/IO</th>
<th>S0</th>
<th>S1</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>IO Write</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>IO Read</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Memory Write</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Memory Read</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>33</td>
<td>I</td>
<td>ADL</td>
<td>Active low Address Decode Latch. It is used to latch the A0-3 address lines.</td>
</tr>
<tr>
<td>34</td>
<td>I</td>
<td>A12</td>
<td>System Address bits 15 to 0. These bits are used for the address decoding of the external IO device. They are also used to address the POS registers.</td>
</tr>
<tr>
<td>36-38</td>
<td>I</td>
<td>A13-15</td>
<td></td>
</tr>
<tr>
<td>39-50</td>
<td>I</td>
<td>A0-11</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>I</td>
<td>CLK</td>
<td>14.3 MHz System Clock. It is used to generate a system wait state.</td>
</tr>
</tbody>
</table>
### 82C575 Pin Description (Continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Type</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>54</td>
<td>I</td>
<td>CDSETUP</td>
<td>Active low Card Setup enable signal. During configuration and error recovery procedures, CDSETUP becomes active along with IO Read/Write commands to access the POS registers.</td>
</tr>
<tr>
<td>57</td>
<td>I</td>
<td>MASK2</td>
<td>Active low mask bits for the comparators of both primary and secondary relocaters. When a mask bit is low, the comparison of the corresponding address input (A2-3) with the relocater address bits 2 to 3 is bypassed. The input buffers have internal pull up resistors. They can be left floating for a “1” value.</td>
</tr>
<tr>
<td>58</td>
<td>I</td>
<td>MASK3</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>I</td>
<td>WSSL0</td>
<td>Wait State Selection signals. They are used to control the system wait state.</td>
</tr>
<tr>
<td>60</td>
<td>I</td>
<td>WSSL1</td>
<td></td>
</tr>
</tbody>
</table>

### WSSL1 WSSL0 Function

<table>
<thead>
<tr>
<th>WSSL1</th>
<th>WSSL0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Synchronous Extented bus cycle</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Synchronous Wait State 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Synchronous Wait State 2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>External asynchronous Extented bus cycle</td>
</tr>
</tbody>
</table>

Synchronous Extended bus cycle is used for 120 ns (Max) read access time peripheral. Synchronous Wait State 1 is for the 250 ns (Max) Read delay time device and Synchronous Wait State 2 for the 460 ns (Max) read delay time peripheral. The External asynchronous Extended bus cycle is used to extend the system bus cycle by using the external RDYIN control signal.

| 62     | O      | CTLA/PRMCS | In set-up cycle, they are Control Output signals for the adapter identification bits. CTLA goes active high while reading the low byte ID (Register 100). CTLB becomes active while reading the high byte ID (Register 101). |
| 61     | O      | CT LB/SDRYCS | In normal operation cycle, those two pins are Peripheral Chip Select signals. PRMCS goes active low when the IO address matches the primary resource relocater address. SDRYCS goes active low when IO address matches the secondary resource relocater. |

| 18,52  | I      | V<sub>CC</sub> | 5V Power Supply. |
| 1,19,  | I      | V<sub>SS</sub> | Power Supply Ground. |
| 35,53  |       |             |                |

**Note:**
- I = Input
- O = Output
- B = Bidirectional
82C575 Functional Description

The 82C575 block diagram is illustrated in Fig 1. The chip consists of the following functional blocks:

- POS Registers
- Peripheral Commands and Card Select Feedback Generator
- Dual Resource Relocator Logic
- Wait state and Card Channel Ready Signal Generator

POS Registers

A total of 6 POS registers are supported by 82C575. These registers can be accessed only during configuration cycle by activating CDSETUP, M/IO to low. The description of each register are as follows:

1. 100H: Low Byte ID Register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID7</td>
<td>ID6 ID5 ID4 ID3 ID2 ID1 ID0</td>
</tr>
</tbody>
</table>

This register is a read only register. The reading of this register returns the contents of pins ID7-ID0.

2. 101H: High Byte ID Register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID15</td>
<td>ID14 ID13 ID12 ID11 ID10 ID9 ID8</td>
</tr>
</tbody>
</table>

This register is a read only register. The reading of this register returns the contents of pins ID7-ID0.

The ID7 to 0 are the multiplexed pins for both low and high ID bytes. Each individual bit can be tied to VCC, VSS, CTLA or CTLB depending on the bit value in the high and low byte register as described in the pin description. For example if 100 low byte ID is “00110110” and 101 high byte ID is “01011010” starting with MSB, ID7 should be tied to VSS, ID6 to CTLB, ID5 to CTLA, ID4 to VCC, ID3 to CTLB, ID2 to CTLA, ID1 to VCC and ID0 to VSS.

3. 102H: Control Register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SADR15</td>
<td>SADR14 SRDYEN OUT3 OUT2 OUT1 OUT0 CDEN</td>
</tr>
</tbody>
</table>

Bits 1 to 4 are brought out to OUT0-3 pins. They can be used for system configuration.

Bits 5, 6 and 7 are used with registers 0103H, 0104H and 0105H and are described below.

Register 102H is readable and writable. All the bits are reset to "0" by RESET signal.

4. 103H: Low Byte Primary Card Address and Secondary Card Address Register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADR7</td>
<td>PADR6 PADR5 PADR4 PADR3 PADR2 SADR8 SADR3</td>
</tr>
</tbody>
</table>

5. 104H: High Byte Primary Card Address Register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PADR15</td>
<td>PADR14 PADR13 PADR12 PADR11 PADR10 PADR9 PADR8</td>
</tr>
</tbody>
</table>


<table>
<thead>
<tr>
<th>Bit</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X SADR13 SADR12 SADR7 SADR6 SADR5 SADR4</td>
</tr>
</tbody>
</table>

The Card Address registers are read/write registers. They are used for resource relocation to avoid adapter conflicts. In case of the same adapter address, the host can reassign the board address. There are two sets of adapter address: Primary and Secondary. For Primary relocator, address bits 15 to 2 are programmable. For Secondary relocater, only bits 15 to 12, bit 8, bits 7 to 3 are programmable. SRDYEN (0102H bit 5) is used to enable the secondary address relocation feature: a zero enables the secondary address relocation registers. Bits 6 and 7 of 0105H are not used and will be read as one’s. The unprogrammed bits in the Secondary relocater (SADR11-9, SADR2) are the same value as the Primary address register bits.

To generate IO read/write commands for the peripheral, or to activate the CDSFBK, or inactivate the CDCHR&DY signals, the address from host A15 to A4 have to match the Primary or the Secondary address register bits. A3 or A2 may bypass the comparison if the individual mask bit is activated by forcing MASK3-2 pins to VSS. A1 to A0 will always bypass the
comparison. The PRMCS signal goes active low if the IO address matches the Primary address register. It can be used as the chip enable signal for the primary peripheral. The SDRYCS signal goes active low when IO address matches the secondary address register and S RDYEN = 0, and can be used as the chip enable for a secondary peripheral. In case only the primary peripheral is used in a system, disable secondary address relocation (S RDYEN = 1).

Peripheral Commands and Card Select Feedback Generator

The peripheral read/write command is generated by decoding the IO or memory address, M/IO, S0, S1, status and gating with CMD signal.

To generate IO read/write commands, the address from host needs to match the dual relocater card address as programmed in the POS registers. (A2-A3 comparison can be bypassed by activating MASK3 to MASK2 individually.)

The Card Select Feedback (CDSFBK) is used to inform the host that the adapter is selected. It stays inactive during a setup cycle. It is generated by decoding the IO address space and S0, S1 status. It should go active within 50 ns after Address and M/IO become valid and within 25 ns from the time status becomes active.

Dual Resource Relocator Logic

Two sets of the resource relocater address registers are supported in this chip. The operation of this block is described in the POS Registers section.

Wait State and Card Channel Ready Generator

The basic channel cycle time in an IBM PS/2 compatible system is 200 ns. It can be extended by using CDCHRDY signal. There are four ways to extend the cycle: Synchronous, Synchronous wait state 1, Synchronous wait state 2 and External Asynchronous.

During a setup cycle, the 82C575 requires no wait states for read/write operations from the host CPU, CDCHRDY is always active and no cycle extension is required. In normal IO operation, the bus cycle is always extended either synchronously or asynchronously.

When the peripheral is addressed, CDCHRDY will go low within 55 ns from the time M/IO and Address become valid (25 ns from the time status S0, S1 become valid) and then returns high within 25 ns after CMD becomes active. The bus cycle is extended from 200 ns to 300 ns, this is called a synchronous extension. This mode is for a peripheral that has a read access delay time of less than 120 ns.

For Synchronous wait state 1 operation, CDCHRDY will go low and stay low for 210 ns to 290 ns from the time CMD goes active. This mode is for a peripheral that has a maximum read access time of 250 ns.

For Synchronous wait state 2 operation, CDCHRDY will go low and stay low for 420 ns to 500 ns after CMD goes active. This can fit the application with the peripheral having read access delay time less than 460 ns.

For External Asynchronous operation, CDCHRDY will go inactive just like synchronous IO access but it will stay low until a low to high transition on pin RDYIN is detected. This mode is for the extremely slow peripheral access.

Application

Figure 2 show an application diagram for 8 bit IO slave peripherals. The Card ID is selected by tying ID0-7 to $V_{CC}$, $V_{SS}$, CTLA or CTLB according the table described in the pin description section. This provides a very flexible method for ID selection. Two resource relocaters are supported which make the multiple peripherals per card applications feasible. Address bits 0 to 3 are latched by the 82C575 for these peripherals. The 82C575 also provides the 74LS245 buffer chip select and direction control signals. The OUT0-3 and CDEN can be used for the system configuration such as interrupt level selection. Due to the high integration of the chip, only a few external components are required to implement a low cost, low parts count solution for Microchannel compatible adapter boards.
Figure 2. 82C575 Application Diagram for 8-Bit I/O Slave Peripheral
### 82C575 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
<td>7.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$V_I$</td>
<td>-0.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_O$</td>
<td>-0.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Operation Temperature</td>
<td>$T_{op}$</td>
<td>-25</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{stg}$</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operation Conditions.

### 82C575 Operation Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>$T_A$</td>
<td>0</td>
<td>70</td>
<td>°C</td>
</tr>
</tbody>
</table>

### 82C575 DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Current</td>
<td>$I_{CC}$</td>
<td>30</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>$V_{IL}$</td>
<td>-0.5</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>$V_{IH}$</td>
<td>2.0</td>
<td>$V_{CC} + 0.5$</td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage (Note 1)</td>
<td>$V_{OL}$</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output High Voltage (Note 1)</td>
<td>$V_{OH}$</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>$I_{IL1}$</td>
<td>-100</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>For $V_{IN} = 0$ to $V_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pins ID0-7, MASK2-3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>$I_{IL2}$</td>
<td>-10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>For all other input pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Tri-State Leakage Current for $V_O = 0$ to $V_{CC}$</td>
<td>$I_{OL}$</td>
<td>-10</td>
<td>10</td>
<td>µA</td>
</tr>
</tbody>
</table>

**Note 1:** $I_{OL} = 6$ mA, $I_{OH} = -2$ mA for pins CDCHRDY, CDSFBK. $I_{OL} = 2.4$ mA, $I_{OH} = -400$ µA for all other pins.
**Capacitance** \((T_A = 25°C, V_{CC} = 0)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance</td>
<td>(C_{IN})</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>For (f_C = 1) MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>(C_{OUT})</td>
<td>20</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>I/O Capacitance</td>
<td>(C_{I/O})</td>
<td>20</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**82C575 AC Characteristics**

\((T_A = 0°C \text{ to } 70°C, V_{CC} = 5V \pm 5\% \text{, } C_L = 60\ pF \text{ for all the output pins})\)

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<td>S0, S1 Set-up to CMD Active</td>
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<td>A0-15, M/I0 Set-up to CMD Active</td>
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<td>CDSETUP Set-up to CMD Active</td>
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<td>CDSETUP Setup time from ADL Active</td>
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<td>CDSETUP Hold time from ADL Inactive</td>
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<td>t8</td>
<td>Write Data Set-up to CMD Inactive</td>
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<td>Write Data Hold time from CMD Inactive</td>
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<td>OUT0-3, CDEN Delay time from Data Valid</td>
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<td>Read Data Delay from CMD Active</td>
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<td>BCS, BCTL Assert Delay from CMD Active</td>
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<td>BCS, BCTL Deassert Delay from CMD Inactive</td>
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<td>CMD Active Pulse Width in SETUP Cycle</td>
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<td>CTLA, CTLB Assert and Deassert delay time from ADL Active</td>
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<td>CDSFBK Active Delay from Address, M/I0, Valid</td>
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<td>CDSFBK Active Delay from Status Active</td>
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<td>CDCHRDY Inactive Delay from Status Active</td>
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### 82C575 AC Characteristics (Continued)

(T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ± 5%, C<sub>L</sub> = 60 pF for all the output pins)

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<td>CDCHRDY Inactive Delay from Address, M/IO, Valid</td>
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<td>CDCHRDY Release Delay from CMD Active in Synchronous Extended Cycle</td>
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<td>CMD Active Pulse Width in both Sync and External Asyn Extended Cycles</td>
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<td>IORD, IOWR Active Delay from CMD Active</td>
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<td>IORD, IOWR Inactive Delay from CMD Inactive</td>
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<td>READ DATA Valid from CMD Active in Sync Extended Cycle</td>
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<td>PRMCS, SDRYCS Assert and Deassert delay time from ADL Active</td>
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<td>t33</td>
<td>CLK High time</td>
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<td>t34</td>
<td>CLK Low time</td>
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<td>t35</td>
<td>CLK Cycle time</td>
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<td>READ DATA Valid from CDCHRDY Active in External Async Extended, Synch Wait State 1 and Sync Wait State 2 bus cycle</td>
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<td>CDCHRDY Release delay time from IORD, IOWR going Active:</td>
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<td>For Synchronous Wait State 1</td>
<td>210</td>
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<td>For Synchronous Wait State 2</td>
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<td>CDCHRDY Release delay time from RDYIN Active in External Async Extended cycle</td>
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82C575 Timing Diagrams

POS Register Setup Cycle Timing
82C575 Timing Diagrams (Continued)

Synchronous Extended Cycle Timing
82C575 Timing Diagrams (Continued)

Synchronous Wait State 1 & Wait State 2 Cycle Timing
82C575 Timing Diagrams (Continued)

External Asynchronous Extended Cycle Timing
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<td>INDIANA</td>
<td>Hall-Mark 4275 W. 96th Street</td>
<td>Indianapolis, IN 46268</td>
<td>317-872-8875</td>
<td>800-423-6638</td>
<td>800-772-0112</td>
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<td>Hall-Mark 10809 Lakeview Drive</td>
<td>Lenexa, KS 66215</td>
<td>913-888-4747</td>
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<td>UTAH</td>
<td>Anthem 1615 West 2200 South</td>
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</tbody>
</table>
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