82C570 CHIPSLink™
SINGLE CHIP "3270" PROTOCOL CONTROLLER

- Implements IBM 3270 Communication Protocol
- Provides IBM 3278/79 and IRMA™ emulation adapter cards interface
- Supports both CUT and DFT modes
- Type A coaxial transmitter and receiver
- 8X Digital Phase Locked Loop (DPLL)
- On chip 4.7 MIPS microcontroller

The 82C570 is a highly integrated IBM 3270 coaxial type A protocol controller chip. It serves as an I/O processor to emulate most of the IBM terminals and printers. It works with IBM 3276/3274/3174 control units either locally or remotely attached.

The 82C570 internal microcode supports most display terminals and printers in both CUT and DFT modes except 3279-S3G due to the large memory requirement. The programmed symbol and APA graphics for 3179/G and 3270 PC/G can only be supported in DFT mode. There are provisions for adding an additional 8K x 8 SRAM and using external microcode.

The 82C570 provides both IRMA and IBM emulation adapter compatible interface. All the IRMA and IBM emulation, file transfer and application software can run on the adapter using 82C570.

The 82C570 along with an external 120ns 8K x 8 SRAM, line driver, line receiver and pulse transformer, a complete 3270 protocol emulation adapter can be built easily.

The 82C570 is fabricated using advanced CMOS technology and is packaged in an 84 pin PLCC.

Figure 1. 82C570 Functional Block Diagram
### 82C570 Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Type</th>
<th>Symbol</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC Bus Interface</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19-21</td>
<td>I</td>
<td>A0-2</td>
<td>System Address bit 0 to 19. These bits are used to address the memory and I/O devices. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB).</td>
</tr>
<tr>
<td>23-39</td>
<td>I</td>
<td>A3-19</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>I</td>
<td>IORD</td>
<td>Active low I/O read strobe. It is used by the system CPU to read the 82C570 internal registers.</td>
</tr>
<tr>
<td>41</td>
<td>I</td>
<td>IOWR</td>
<td>Active low I/O write strobe. It is used by the system CPU to load the information into the internal registers.</td>
</tr>
<tr>
<td>44</td>
<td>I</td>
<td>MEMRD</td>
<td>Active low memory read strobe. When this signal is active, the display buffer is read.</td>
</tr>
<tr>
<td>45</td>
<td>I</td>
<td>MEMWR</td>
<td>Active low memory write strobe. When active, the display buffer is written or the external microcode is being downloaded.</td>
</tr>
<tr>
<td>46</td>
<td>I</td>
<td>AEN</td>
<td>Active high address enable for DMA transfers. When this line is active, DMA controller has the control of the bus. When it is low, IORD IOWR MEMRD MEMWR are enabled for 82C570.</td>
</tr>
<tr>
<td>47</td>
<td>T</td>
<td>READY</td>
<td>READY is a active high output signal to indicate to the host system that a data transfer will be completed. During I/O transfer, this signal will always be tri-stated. For memory read or write operation, READY will be deasserted for a period of 220 ns - 460 ns to inform the host to insert the wait state. READY has the tri-state buffer and requires external pull up resistor. It can drive the system bus directly.</td>
</tr>
<tr>
<td>48</td>
<td>T</td>
<td>IRQ</td>
<td>Interrupt request signal. When IRQ is active, it will go low for 100 ns - 250 ns then return to tri-state. It is designed for the edge triggered interrupt system.</td>
</tr>
<tr>
<td>49</td>
<td>I</td>
<td>RESET</td>
<td>Active high hardware reset signal. When reset is active, it initializes the chip and the program counter of the microcontroller is reset to address 0.</td>
</tr>
<tr>
<td>50</td>
<td>T</td>
<td>IRQ1</td>
<td>Level interrupt request signal. When a interrupt is initiated, IRQ1 will be held active low until it is acknowledged by the system interrupt service routine. It stays tri-stated when it is inactive.</td>
</tr>
<tr>
<td>51</td>
<td>O</td>
<td>BCS</td>
<td>Active low external 74LS245 buffer enable signal. It goes active when the internal registers or the display buffer RAM are accessed. (Either read or write.)</td>
</tr>
<tr>
<td>52-59</td>
<td>B</td>
<td>D0-7</td>
<td>System data bit 0 to 7. These bits are used to transfer data to and from the CPU data bus. They are 3 state bidirectional lines.</td>
</tr>
</tbody>
</table>
**82C570 Pin Description** (Continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Type</th>
<th>Symbol</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Serial interface</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>I</td>
<td>RXD</td>
<td>Receive input data. It is the serial biphase Manchester II encoded bit stream from the controller unit. RXD is connected to the TTL level output of the external differential receive amplifier.</td>
</tr>
<tr>
<td>61</td>
<td>O</td>
<td>TXD</td>
<td>Transmit data output. It is the biphase Manchester II encoded data output from the transmitter. An external line driver is required for cable interface.</td>
</tr>
<tr>
<td>62</td>
<td>O</td>
<td>TXACT</td>
<td>Active high transmit active signal. It goes high while the transmitter is transmitting.</td>
</tr>
<tr>
<td>65</td>
<td>O</td>
<td>TXDLY</td>
<td>Delayed transmit output data. It has a delay of 1/4 bit time from TXD. TXDLY is designed for an easy implementation of the cable waveform precompensation.</td>
</tr>
<tr>
<td><strong>Buffer RAM interface</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7-3</td>
<td>O</td>
<td>MA0-4</td>
<td>Memory address bit 0 to 12. These bits are used to address the RAM buffer. MA0 is the least significant bit and MA12 is the most significant bit.</td>
</tr>
<tr>
<td>84-77</td>
<td>O</td>
<td>MA5-12</td>
<td></td>
</tr>
<tr>
<td>18-11</td>
<td>B</td>
<td>MD0-7</td>
<td>Memory data bit 0 to bit 15. They are 3 state lines used to transfer the data between RAM, 82C570, control units and system CPU. MD0 is the least significant bit and MD15 is the most significant bit.</td>
</tr>
<tr>
<td>76-69</td>
<td>B</td>
<td>MD8-15</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>O</td>
<td>RAMWR</td>
<td>Active low memory write strobe signal. It is active when system CPU, control unit or 82C570 write the buffer RAM.</td>
</tr>
<tr>
<td>9</td>
<td>O</td>
<td>RAMRD</td>
<td>Active low memory read strobe signal.</td>
</tr>
<tr>
<td>10</td>
<td>O</td>
<td>MCS1</td>
<td>Active low memory selection 1. It is used to enable the first RAM.</td>
</tr>
<tr>
<td>68</td>
<td>O</td>
<td>MCS2</td>
<td>Active low memory selection 2 used for the enabling of the second RAM.</td>
</tr>
<tr>
<td><strong>Miscellaneous</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>67,66</td>
<td>I/O</td>
<td>X1, X2</td>
<td>Crystal oscillator input. A fundamental frequency parallel resonant crystal should be connected to this pair. Alternatively, an external clock source may be connected to X1 input by floating X2. The clock frequency should be 18.8696 MHz with an accuracy of ± 0.01%.</td>
</tr>
<tr>
<td>1,42,63</td>
<td>I</td>
<td>VCC</td>
<td>5 Volt power supply.</td>
</tr>
<tr>
<td>2,22,43,64</td>
<td>I</td>
<td>VSS</td>
<td>Power supply ground.</td>
</tr>
</tbody>
</table>

**Note:**  
I = Input  
O = Output  
T = 3-state output  
B = Bidirectional
82C570 Functional Description

The 82C570 block diagram is illustrated in Fig 1. The chip consists of the following functional blocks:

- Serial Interface Section
- Host System Interface Logic
- SRAM Control Block
- Microcontroller
- IRMA and IBM Adapter Interface

The internal microcode supports three operation modes:

- 3278/79 Display CUT mode (78E).
  Displays in CUT mode will have 4K display buffer storage and 4K Extented Attribute Buffer (EAB) storage. This will support all the terminal types except the 3279-S3G which needs 64K programmed symbol memory.

- 3287 Printer CUT mode (87E).
  Printer in CUT mode will use 4K or 8K (configurable) bytes of the buffer for information and message storage. The 82C570 will put all the information inside the buffer and generate an interrupt after receiving the START OPERATION command.

- Distributed Function Terminal mode (DFT).
  Displays and printers in DFT mode use 8K memory for input and output storage followed by a 128 bytes of memory for data communication. The 82C570 will put all the information inside the buffer and generate an interrupt after receiving the START OPERATION command.

3270 Coaxial Type A Protocol Overview

The RG62AU coaxial cable is used to connect between control unit and device (terminal, printer, PC) with a maximum length of 1.5 meters. The data transmission is encoded by using the bi-phase Manchester II technique which has a fix bit rate of 2.3587 MHz.

In the bi-phase Manchester II encoding, the 1st half of the bit cell consists of the complementary data and the 2nd half of the bit cell is the true data. There is always a central bit transition in the normal bit cell except in the transmission starting or ending sequence which have the code violations in the bit frame.

The transmission packet between the adapter and control unit is composed of the following:
1. Transmission Start Sequence (Code Violation Sequence).
2. One or more data frames.
3. Transmission Ending Sequence (Mini Code Violation Sequence).

At the beginning of the packet, five consecutive “1” bits followed by one and half bits high level and one and half bits low level will be transmitted by adapter or the control unit. This is called the Transmission Start Sequence. At the end of the packet, a Transmission Ending Sequence is sent to signify the completion of the data frame. It consists of a “0” bit followed by two bits of high level without central bit transition. Fig 2 shows the Start and Ending Sequence.

![Transmission Start and Ending Sequence](image)

Figure 2. Transmission Start and Ending Sequence

The data frame is composed of 12 bits starting with “1” sync bit and ending with even frame parity bit. The frames have three formats: command word, data word and status word.
**COMMAND WORD:**

b1: Sync Bit = 1.
b2-4: Address Bits. Bits 2-4 = 0 for Base. Bits 2-4 = X for Feature.
b5-9: Command ID.
b10: Unused.
b11: Command Bit = 1.
b12: Frame Parity. Even parity for b1 through b11.

The command word is from control unit only. It can be read or write type. For the read type command, the chip responds with either data or status word. For a write type command, the chip responds with TT/AR (Transmit Turnaround/Auto Response). For any good command from the control unit, the chip will respond within 5µs after receiving the last bit of the ending sequence.

**DATA WORD:**

b1: Sync Bit = 1.
b2-9: Data Byte. Bit 2 is the most significant bit and bit 9 is the least significant bit.
b10: Data byte parity. Odd parity for bit 2 through 9.
b11: Data Bit = 0.
b12: Frame parity. Even parity for b1 through b11.

The data word can be from control unit or the adapter. For control unit, it always follows the write command. For the adapter, it is the response of the read command.

**STATUS WORD:**

b1: Sync Bit = 1.
b12: Frame even parity.

For no keystroke returned:
TT/AR: b2-11 = 0.
Poll request: b6 = 1.
Operation complete: b9 = 1.
POR complete: b8 = 1, b10 = 1.
Feature error: b11 = 1.

For keystroke returned:
b2-9: Keyboard scan code.
b10: 1.
b11: 0.

The status word is returned from the chip in response to the Poll command from the control unit.

**Serial Interface Section**

The Serial Interface section consists of several signals that are used to connect the external analog circuit. The external transmission line driver (DP3487/MC3487) and receiver (DP3486/MC3486) and pulse transformer (PE85762) are used for the cable interface.

The TXACT goes active high while the transmitter is transmitting, it is used to enable the tri-state line driver. The transmit data (TXD) and transmit delay data (TXDLY) are also connected to the driver. The output of the driver feeds into the integrated pulse transformer which consists of the resistor and capacitor network and provides the proper signal level. The waveform at the coaxial cable is precompensated. The signals on the cable are polarized. The line receiver converts the differential cable signals (Minimum amplitude of 40mV and minimum pulse width of 185ns) to TTL level receive data RXD. Fig 3 shows the transmit and receive waveform.

The transmitter logic includes transmit holding register, transmit shift register, parity generator, starting and ending sequence generators, Manchester encoder. The content of b11 of the transmit frame is controlled by the microcode. Bit 10 can be the data byte parity bit or programmed by the microcode.

The receiver consists of receive shift register, receive hold register, parity checker, starting and ending sequence detector, clock and data recovery circuit. The clock/data recovery circuit consists of a sophisticated 8X digital phase locked loop which can tolerate a maximum of ±35ns data jitter. The receive overrun, frame parity error and missing sync bit will cause the receive error state which disables the receiving and waits for the next starting sequence. Two receiver modes are supported: Mode 0 supports the 12 bits frame. Mode 1 supports both 8 bits (1st frame only) and 12 bits frame which may fit the 3299 multiplexor application.
The chip has an on-chip crystal oscillator. The 18.8696 MHz fundamental mode parallel resonant crystal is connected to pins X1 and X2. It requires two 20 pF capacitors to ground to prevent spurious oscillation. Alternatively, an external clock source may be connected to X1 input by floating pin X2. The 18.8696 MHz clock is used in receiver for data and clock recovery. It is divided down to generate the transmit clock for the frame encoding. It is also used in the microcontroller as the processor clock.

**Host System Interface Section**

The 82C570 provides a very simple method to interface with the IBM PC/XT, PC/AT and PS/2 model 30. Also together with the 82C574 microchannel interface chip, the 82C570 can support the PS/2 model 50, 60 and 80 easily.

The data bus is one byte wide to transfer the data between the host system and the I/O registers or the display memory. An external 74LS245 data buffer is recommended to use between the system data bus and D0-7. BCS is provided to turn on the buffer and the direction control is generated externally by NANDing the MEMWR and iOWR signals.

The system address bus is connected directly to the chip for the I/O and memory space decoding. The READY signal is used to control the display buffer read or write operations. Two interrupt request systems are supported: IRQ is used in the edge triggered system (IBM PC/XT/AT) and IRQ1 is used in the level interrupt system (PS/2 model 50, 60, 80).

The 82C570 supports both external and internal micro code operations by programming the 228H Operation Register. The detailed function of this register is described as follows:

**228H Operation Register:**

This register is used to control the operation of 82C570.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>Unused.</td>
</tr>
<tr>
<td>b6</td>
<td>Unused.</td>
</tr>
<tr>
<td>b5</td>
<td>Test 2. It is used for the chip testing purpose and should be held low in normal operation.</td>
</tr>
<tr>
<td>b4</td>
<td>Microcontroller Program Counter Reset Signal.</td>
</tr>
<tr>
<td>b3</td>
<td>Test 1. A bit to control the testing function. This bit should stay low in normal operation.</td>
</tr>
<tr>
<td>b2</td>
<td>External Microcode Download Control Signal.</td>
</tr>
<tr>
<td>b1</td>
<td>External Microcode Operation Mode.</td>
</tr>
<tr>
<td>b0</td>
<td>Software Reset.</td>
</tr>
</tbody>
</table>

All the bits are reset when RESET pin goes active. The external micro code is down-
loadable from floppy disk by executing the memory write operation with b2 (external microcode download control signal) and b1 (external microcode operation mode) high. After the completion of download process, b0 (Software Reset signal) should be turn on for a minimum period of 500 ns to initialize the chip again before doing other operation.

**SRAM Control Block**

The memory used by the 82C570 consists of 8K x 8 static RAMs with 120 ns access time. The Address (MA0-12), Data (MD0-7) Read/Write control (RAMRD, RAMWR), and memory chip enable signals (MCS1, MCS2) are all provided by 82C570.

If the user uses the internal microcode, only one 8K x 8 RAM is required (MCS1 is active). The lower half 4K is for data buffer and the higher half 4K is for the EAB buffer. The memory is dual ported between Host System (PC) and microcontroller. The arbitration logic is built on the chip with microcontroller having higher priority. When the Host accesses the memory, the memory Address MA0-12 are the same value as the Host Address A0-12. A12 controls the lower or higher half portion of the RAM. The READY signal controls the wait state and signifies the completion of the memory access.

If the external microcode is used, two 8K x 8 RAMs are required. MCS1 enables the first RAM and MCS2 enables the second RAM. The microcode can be downloaded from the floppy by enabling the MEMWR signal with the b1 and b2 on in register 228H. It can be read back for verification by enabling MEMRD with same b1 and b2 value. The microcode is relocated by the 82C570 with the 1st 4K of the microcode (A12 = 0) locating at the higher half of the first RAM (MCS1 active and MA12 = 1) and the 2nd 4K (A12 = 1) locating at the higher half of the second RAM (MCS2 active and MA12 = 1). To read or write the data/EAB buffer, the register 228H b1 should be high and b2 should stay low. The data buffer is located at the lower half of the first RAM (MCS1 active and MA12 = 0) with the Host address A12 = 0. The EAB buffer is located at the lower half of the second RAM (MCS2 active and MA12 = 0) with the Host address A12 = 1. The memory access is arbitrated between Host, microcontroller and microcode access. The microcontroller has the highest priority and the microcode access has the lowest priority.

**Microcontroller Section**

The 82C570 contains a very high speed microengine. The microcode is 16 bits wide and the data transfer between registers and memory is 8 bits wide. Each microcode command executes in 212ns except when executing from external microcode, and fetching or storing data memory in which case a microinstruction takes 414 ns.

The microcontroller is composed of an ALU, working registers (With general and special functions), zero flag, zero flag stack, program counter, program counter stack and two accumulators, two RAM address counters.

The microinstructions supported by the microcontroller are listed as below:

- Immediate ALU Operation
- Source/Destination ALU Operation
- Conditional Branch
- Pulse Function
- Jump on Accumulator
- Return from Interrupt
- Long Jump

The detailed operation of each instruction is described in the different document: 82C570 Microcode Specification.

**IRMA and IBM Adapter Interface**

The 82C570 provides both IRMA and IBM adapter cards interface compatible registers. All the terminal emulation and file transfer application software written for these two boards can also run on the adapter cards using 82C570 chip.
IRMA Interface

There are 6 I/O addressible registers and 13 IRMA commands defined in this interface. To initiate a command, the host CPU puts the command codes in IRMA0 register and the associated arguments in IRMA1-3 registers. The command request flag is set by writing any data to I/O address 226H. During idle, the microcontroller keeps on polling this flag bit. Once the set flag is detected, it starts to execute the command and reset this command flag. After the command is processed, the microcontroller put the execution results and status back to the IRMA0-3 registers.

The description of the registers is listed as follows:

220H-223H IRMA0-IRMA3 registers. These four registers are the communication box between host system and control unit. They contain the command codes and the arguments after being written by the CPU. The command execution results and status are put back to these registers after the command processing.

226H Not defined. The command request flag is set by executing an I/O write to this address.

227H Status Flag register. When the CPU reads this register, b7 indicates the attention request flag and b6 indicates command request flag. b5-b0 are "0" and unused. The attention request flag is cleared by executing an I/O write to this address. It is set when the main status bits are changed from "0" to "1" with the attention mask bits set in the corresponding bits.

Main Status Register:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>Auxiliary Status change occurred.</td>
</tr>
<tr>
<td>b6</td>
<td>Trigger occurred.</td>
</tr>
<tr>
<td>b5</td>
<td>Key buffer empty.</td>
</tr>
<tr>
<td>b4</td>
<td>Unused.</td>
</tr>
<tr>
<td>b3</td>
<td>Reset command from control unit.</td>
</tr>
<tr>
<td>b2</td>
<td>Unused.</td>
</tr>
<tr>
<td>b1</td>
<td>Buffer modified. The buffer write commands set this bit.</td>
</tr>
<tr>
<td>b0</td>
<td>Cursor address loaded.</td>
</tr>
</tbody>
</table>

Bits 7, 6, 3, 1, 0 can be cleared by PC using Clear Main Status Bits command.

Auxiliary Register:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>Unused.</td>
</tr>
<tr>
<td>b6</td>
<td>Unit Polled. This bit is set by a Poll command and reset after being read by the microcontroller.</td>
</tr>
<tr>
<td>b5</td>
<td>Sound alarm.</td>
</tr>
<tr>
<td>b4</td>
<td>Display inhibited.</td>
</tr>
<tr>
<td>b3</td>
<td>Cursor inhibited.</td>
</tr>
<tr>
<td>b2</td>
<td>Reverse cursor enabled.</td>
</tr>
<tr>
<td>b1</td>
<td>Cursor blink enable.</td>
</tr>
<tr>
<td>b0</td>
<td>Keyboard click enable.</td>
</tr>
</tbody>
</table>

B0 through B5 are set and reset by the control unit.
The IRMA commands supported by the internal microcode are listed as follows:

<table>
<thead>
<tr>
<th>Code (b3-b0)</th>
<th>Command Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read Buffer Data</td>
</tr>
<tr>
<td>1</td>
<td>Write Buffer Data</td>
</tr>
<tr>
<td>2</td>
<td>Read Status/Cursor Position</td>
</tr>
<tr>
<td>3</td>
<td>Clear Main Status Bits</td>
</tr>
<tr>
<td>4</td>
<td>Send Keystroke</td>
</tr>
<tr>
<td>5</td>
<td>Send Selector Pen Location</td>
</tr>
<tr>
<td>6</td>
<td>Execute Power-on-Reset</td>
</tr>
<tr>
<td>7</td>
<td>Load Trigger Data and Mask</td>
</tr>
<tr>
<td>8</td>
<td>Load Trigger Address</td>
</tr>
<tr>
<td>9</td>
<td>Load Attention Mask</td>
</tr>
<tr>
<td>A</td>
<td>Set Terminal Type</td>
</tr>
<tr>
<td>C</td>
<td>Read Terminal Information</td>
</tr>
<tr>
<td>E</td>
<td>Return revision ID and OEM number</td>
</tr>
</tbody>
</table>

Read Buffer Data:
For this command, IRMA0-3 registers contain the command code and the buffer address. The main status, buffer data and the corresponding EAB data are returned at the end of the execution.

<table>
<thead>
<tr>
<th>Registers</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRMA1 ADDR (L)</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>IRMA2 ADDR (H)</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>IRMA3 Data for Write</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

Write Buffer Data:
The operation of this command is similar to Read Buffer Data command except that it executes the writing of buffer.

<table>
<thead>
<tr>
<th>Registers</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0 Command 4</td>
<td>Main Status</td>
<td></td>
</tr>
<tr>
<td>IRMA1 X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2 X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3 Key Scan Code</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

Read Status/Cursor Position:
This command reads the cursor address and the main/Aux status registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0 Command 2</td>
<td>Main Status</td>
<td></td>
</tr>
<tr>
<td>IRMA1 X</td>
<td>Cursor Address Low</td>
<td></td>
</tr>
<tr>
<td>IRMA2 X</td>
<td>Cursor Address High</td>
<td></td>
</tr>
<tr>
<td>IRMA3 X</td>
<td>Aux Status</td>
<td></td>
</tr>
</tbody>
</table>

Clear Main Status Bits:
This command is used to clear the main status bits. Five bits (b7,6,3,1,0) can be reset by the PC. The status bits are cleared if the corresponding clear mask bits are “1”. The returned status bits are the status after the command has been executed.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0 Command 3</td>
<td>Main Status</td>
<td></td>
</tr>
<tr>
<td>IRMA1 X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2 X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3 Bits Clear Mask</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

Send Keystroke Command:
This command causes the chip to send a key scan code to the control unit. It resets bit 5 (Key buffer empty) of the main status register to “0”.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0 Command 4</td>
<td>Main Status</td>
<td></td>
</tr>
<tr>
<td>IRMA1 X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2 X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3 Key Scan Code</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>
Send Selector Pen Location:
This command causes the light pen position to be sent to the control unit.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>Command 5</td>
<td>Main Status</td>
</tr>
<tr>
<td>IRMA1</td>
<td>Row on Screen</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2</td>
<td>Field ID on Screen</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Execute Power on Reset:
This command causes the chip appears to the control unit that it has been reset.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>Command 6</td>
<td>Main Status</td>
</tr>
<tr>
<td>IRMA1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Load Trigger Data and Mask:
This command loads the trigger data and trigger mask registers. The trigger occurred bit will be set if the buffer address matches the trigger address and the buffer data bits match the corresponding trigger data bits. (Only the bits with the value of “1” in the mask register are compared.)

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>Command 7</td>
<td>Main Status</td>
</tr>
<tr>
<td>IRMA1</td>
<td>Data Pattern</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2</td>
<td>Mask Pattern</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Load Trigger Address:
This command sets the buffer position for the data/mask comparison. The trigger occurred bit should be reset by this command.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>Command 8</td>
<td>Main Status</td>
</tr>
<tr>
<td>IRMA1</td>
<td>ADDR (L)</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2</td>
<td>ADDR (H)</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Load Attention Mask:
This command loads the attention mask register. Whenever the main status bits change from “0” to “1”, the Attention Request flag is set if the corresponding attention mask register bits are set to “1”.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>Command 9</td>
<td>Main Status</td>
</tr>
<tr>
<td>IRMA1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3</td>
<td>Mask Pattern</td>
<td>X</td>
</tr>
</tbody>
</table>

Set Terminal Type:
This command is used to set the terminal type. If a new type is assigned, the POR status is issued and the new terminal type is stored, otherwise no action is taken.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>Command A</td>
<td>Main Status</td>
</tr>
<tr>
<td>IRMA1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA2</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>IRMA3</td>
<td>New Terminal ID</td>
<td>X</td>
</tr>
</tbody>
</table>
Read Terminal Information:
This command is used to get the terminal conditions.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>C</td>
<td>Command C</td>
</tr>
<tr>
<td>IRMA1</td>
<td></td>
<td>Starting EAB Page Number</td>
</tr>
<tr>
<td>IRMA2</td>
<td></td>
<td>Starting Internal Variable Page Number</td>
</tr>
<tr>
<td>IRMA3</td>
<td></td>
<td>Current Terminal Type</td>
</tr>
</tbody>
</table>

Return Revision ID and OEM Number:
A unique number is assigned for the application.

<table>
<thead>
<tr>
<th>Register</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRMA0</td>
<td>C</td>
<td>Command E</td>
</tr>
<tr>
<td>IRMA1</td>
<td></td>
<td>Low 2 BCD digits of Revision Number</td>
</tr>
<tr>
<td>IRMA2</td>
<td></td>
<td>High 2 BCD digits of Revision Number</td>
</tr>
<tr>
<td>IRMA3</td>
<td></td>
<td>OEM Number</td>
</tr>
</tbody>
</table>

IBM Interface
For IBM application software interface, the 82C570 provides 11 registers with I/O mapped addresses from 2D0-2DA for the communication between host CPU and the control unit.

Table 1

<table>
<thead>
<tr>
<th>I/O Address</th>
<th>Registers</th>
<th>POR contents</th>
<th>PC Read</th>
<th>PC Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>02D0</td>
<td>PC Adapter Interrupt Status</td>
<td>0 0 X 1 X X X X</td>
<td>Data</td>
<td>Reset Mask</td>
</tr>
<tr>
<td>02D1</td>
<td>Visual/Sound</td>
<td>X 0 Z Z Z Z Z Z</td>
<td>Data</td>
<td>Reset Alarm</td>
</tr>
<tr>
<td>02D2</td>
<td>Cursor Address Low</td>
<td>X X X Z Z Z Z Z</td>
<td>Data</td>
<td></td>
</tr>
<tr>
<td>02D3</td>
<td>Cursor Address High</td>
<td>Z E Z E Z Z Z Z</td>
<td>Data</td>
<td></td>
</tr>
<tr>
<td>02D4</td>
<td>PC Adapter Control</td>
<td>1 0 0 Z Z 0 0 0</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>02D5</td>
<td>Scan Code</td>
<td>X X X X X X X X X</td>
<td>Data</td>
<td></td>
</tr>
<tr>
<td>02D6</td>
<td>Terminal ID</td>
<td>X X X X X X X X X</td>
<td>Data</td>
<td></td>
</tr>
<tr>
<td>02D7</td>
<td>Segment</td>
<td>1 1 0 0 1 1 1 0</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>02D8</td>
<td>Page Change Low</td>
<td>X X X X X X X X X</td>
<td>Data</td>
<td>Reset Mask</td>
</tr>
<tr>
<td>02D9</td>
<td>Page Change High</td>
<td>X X X X X X X X X</td>
<td>Data</td>
<td>Reset Mask</td>
</tr>
<tr>
<td>02DA</td>
<td>87E Status</td>
<td>X X X X X X X X X</td>
<td>Data</td>
<td>Reset Mask</td>
</tr>
</tbody>
</table>

Note: 0 - hardware reset  
Z - internal microcode reset  
X - Undetermined  
1 - hardware set  
E - internal microcode set
PC Adapter Interrupt Status Register:

- **b0**: Keystroke Accepted (78E mode) Start Operation Command (DFT and 87E modes).
  - In 78E mode, this bit is set by the chip when a keystroke is acknowledged by the control unit and reset by PC.
  - In 87E and DFT modes, this bit is set by the chip when a Start Operation command is decoded and reset by PC.

- **b1**: Reset Command (All modes). This bit is set when a Reset command is decoded and reset by PC.

- **b2**: In 78E mode, this bit represents "Visual/Sound Registers Updated". It is set when the Load Control Register command is decoded or when the sound alarm enable/disable clicker has been decoded in a Poll command. In 87E mode, this bit is set when the enable/disable operation has been decoded in a Poll command. In DFT mode, the decoding of the Diagnostic Reset command sets this bit.

- **b3**: Read Terminal ID Command. This bit is used in DFT mode only. The decoding of the Read Terminal ID command sets this bit.

- **b4**: Base Buffer Modified Complete. This bit is used in 78E mode. It is set at the termination of a Write Data, Clear and Insert commands.

- **b5**: Load I/O Address Command. This bit is set when the the Load I/O Address High or Low commands are received in the 78E mode. When set, it will generate the interrupt to the PC if the mask bit is off and bit 3 (Inhibit cursor bit) of the Visual/Sound register is off if the conditional inhibit disable bit (Bit 6 in the PC adapter register) is set.

- **b6**: Buffer Being Modified. This bit is used in 78E mode only. It is set at the beginning of the Write Data, Clear and Insert command. It is reset at the end of the command when Base Buffer Modified Complete bit is set.

- **b7**: Interrupt Generated. This bit is set when one of the interrupt status bits b0-b5 is on and the interrupt mask bit is off. It is reset by the PC when it resets the interrupt bits or when the mask bit is on.

Visual/Sound Register:

- **b0**: Characters per line. 132 characters per line if this bit is "1". 80 characters per line for "0".

- **b1**: Inhibit feature step of the buffer address counter.

- **b2**: Inhibit display.

- **b3**: Inhibit cursor.

- **b4**: Reverse cursor.

- **b5**: Blink cursor.

- **b6**: Sound alarm.

- **b7**: Click enable.

This register is set and reset by the control unit except b6 which is reset by the Host by writing anything to this register. The loading of this register causes b2 (Visual/Sound Updated bit) of the PC Adapter Interrupt Status register to be set.

Cursor Address Low Register:

This register is readable only. It contains the value of low byte buffer address counter.

Cursor Address High Register:

Similar to Cursor Address Low register, the register is readable only and contains the value of high byte buffer address counter.
PC Adapter Control Register:

This register can be read and written by PC.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>Coaxial Cable Enable. It is set (Enabled) by the PC and reset by PC or Reset signal. The writing of 220H register will also set this bit. When it is reset, the chip is disabled and unable to respond to the control unit. POR response will be returned for the first Poll command after the coaxial cable is enabled.</td>
</tr>
<tr>
<td>b1</td>
<td>78E, 87E/DFT mode. If “1”, the chip operates in DFT mode. If “0”, it operates in 78E or 87E mode.</td>
</tr>
<tr>
<td>b2</td>
<td>87E/78E mode. The chip is configurated as 87E mode if b1 = “0” and b2 = “1”. It is configurated as 78E mode if b2 = “0” and b1 = “0”.</td>
</tr>
<tr>
<td>b3</td>
<td>Keystroke Available. This bit is used in 78E mode only. When set, it indicates that the scan code has been loaded by PC. It is reset by the Poll Acknowledge and Reset commands.</td>
</tr>
<tr>
<td>b4</td>
<td>Request Poll. When set by the PC, it causes the poll request bit to be returned for the next poll response. It is reset by the Poll Acknowledge command. This bit is used in 87E and DFT modes only.</td>
</tr>
<tr>
<td>b5</td>
<td>Test bit. The test function is not implemented by the internal microcode.</td>
</tr>
<tr>
<td>b6</td>
<td>“Reset Cursor” for 87E mode. It resets the buffer address counter to 0 when it is active. “Conditional Interrupt Disable” for 78E mode. When this bit is set, the decoding of Load I/O Address command interrupts are disabled if bit 3 (inhibit cursor bit) of the Visual/Sound register is set.</td>
</tr>
<tr>
<td>b7</td>
<td>Disable Interrupts. This bit is set when Reset signal is active. It can be set and reset by PC. When active, it inhibits all interrupts (B0 to B5 in the PC Adapter Interrupt Status register) to the PC. The interrupt status bits can be set even with this mask bit on.</td>
</tr>
</tbody>
</table>

Scan Code Register:

This register holds the keystroke code to be sent to the control unit. This register should not be changed if bit 3 of the PC-Adapter Control register (keystroke available bit) is set. The contents sent to the control unit is the one’s complement value of this register.

Terminal ID Register:

This register represents the terminal ID. It is programmed by the Host before enabling the coaxial cable. The content of the data sent to the control unit is the one’s complement of this register.

For DFT and 87E modes: “01” H should be programmed. For 78E mode:

- bit 4-7 Keyboard ID.
- bit 1-3 3278/3279 Models.
  - 010 for model 2
  - 011 for model 3
  - 111 for model 4
  - 110 for model 5

Segment Register:

Bit 0 of this register controls the enabling of the buffer memory access. A “0” allows the memory read/write. The memory access is prohibited if this bit is “1”.

Bit 1 to 7 of the Segment Register is written by PC for the desired memory block address. It is used for the memory relocation. Bit 1 to 7 are compared with PC address bit 13 to 19. Only a match in the comparison will enable the memory access. The Reset default value of the register is “CE”.
Page Change Low Register:
This register indicates the change of each 256 bytes of the lower 2K buffer space. During the write command from the control unit, the bit will be set if any modification of the corresponding 256 byte page buffer happens. The bit gets reset when the Host (PC) writes to this register and the corresponding data bus bit is “1”.

The buffer locations that correspond to each bit are listed as follows:

<table>
<thead>
<tr>
<th>bit</th>
<th>buffer locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 - 255</td>
</tr>
<tr>
<td>1</td>
<td>256 - 511</td>
</tr>
<tr>
<td>2</td>
<td>512 - 767</td>
</tr>
<tr>
<td>3</td>
<td>768 - 1023</td>
</tr>
<tr>
<td>4</td>
<td>1024 - 1279</td>
</tr>
<tr>
<td>5</td>
<td>1280 - 1535</td>
</tr>
<tr>
<td>6</td>
<td>1536 - 1791</td>
</tr>
<tr>
<td>7</td>
<td>1792 - 2047</td>
</tr>
</tbody>
</table>

Page Change High Register:
Similiar to Page Change Low Register, this register indicates the change of each 256 bytes of the higher 2K buffer space. The bits are set and reset the same way as Page Change Low Register.

The following table shows the buffer locations corresponding to each data bus bit:

<table>
<thead>
<tr>
<th>bit</th>
<th>buffer locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2048 - 2303</td>
</tr>
<tr>
<td>1</td>
<td>2304 - 2559</td>
</tr>
<tr>
<td>2</td>
<td>2560 - 2815</td>
</tr>
<tr>
<td>3</td>
<td>2816 - 3071</td>
</tr>
<tr>
<td>4</td>
<td>3072 - 3327</td>
</tr>
<tr>
<td>5</td>
<td>3328 - 3583</td>
</tr>
<tr>
<td>6</td>
<td>3584 - 3839</td>
</tr>
<tr>
<td>7</td>
<td>3840 - 4095</td>
</tr>
</tbody>
</table>

87E Status Register:
This register is dedicated for 87E mode operation only. Bits are set by the control unit and reset under mask by PC.

<table>
<thead>
<tr>
<th>bit</th>
<th>function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-4</td>
<td>Unused.</td>
</tr>
<tr>
<td>5</td>
<td>87E sound alarm. It is set by the Poll command.</td>
</tr>
<tr>
<td>6</td>
<td>Disable operation. This bit is set by Poll or Poll Acknowledge command.</td>
</tr>
<tr>
<td>7</td>
<td>Enable operation. Set by Start Operation, Poll or Poll Acknowledge commands.</td>
</tr>
</tbody>
</table>

Features and Commands Supported by Internal Microcode

Base Feature
The 82C570 internal microcode supports most of the base feature commands. Table 2 lists all the commands supported. The description of the commands is as follows:

Poll:
This command doesn't use the address portion of the command word. The functions of the frame bit 2 and bit 3 are assigned as follows:

<table>
<thead>
<tr>
<th>b2</th>
<th>b3</th>
<th>78E mode function</th>
<th>87E mode function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Enable keyboard clicker.</td>
<td>Enable operation.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Disable keyboard clicker.</td>
<td>Disable operation.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Sound alarm.</td>
<td>Sound alarm.</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>None of the above.</td>
<td>None of the above.</td>
</tr>
</tbody>
</table>
The following status frames are returned to the control unit in response to the Poll command:

<table>
<thead>
<tr>
<th>Response</th>
<th>Frame Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>POR complete</td>
<td>0 0 0 0 0 0 0 1 0 1 0</td>
</tr>
<tr>
<td>TT/AR</td>
<td>0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Keystroke available</td>
<td>2-9 Scan Code 1 0</td>
</tr>
<tr>
<td>Base status</td>
<td>0 0 0 0 x 0 0 x 0 x</td>
</tr>
</tbody>
</table>

The base status bit 6 is set for poll request (For DFT and 87E modes only). Bit 9 is active if the operation is complete. The feature error will set bit 11. The priority of the multiple poll responses is listed as below:

1. Feature error. 2. POR complete. 3. Poll request. 4. Operation complete. 5. Keystroke available. 6. Any other feature status.

Reset:

The decoding of this command sets bit 1 (Reset command decoded bit) of the PC Adapter Interrupt Status register. Both data and EAB buffers will not be cleared. The buffer address counter is set to "0050H" for 78E and DFT modes, and "0000" for 87E mode. TT/AR is returned to the control unit. The chip can accept two or more Reset command (Without intervening Poll commands) and responds with a single POR response to a subsequent Poll.

Read Data:

The return of this command is the data at the location of current buffer address counter. The address counter is incremented by one at the completion of the command.

Load Address Counter High:

The decoding of this command causes the chip to load the next data frame into the high byte of the buffer address counter. In 78E mode, it sets the bit 5 of the PC-Adapter Interrupt Status.

Read Address Counter High:

The 82C570 responds to this command by sending the content of the high byte buffer address counter. It is supported in both 78E and 87E modes only.

Clear:

This command clears all or part of the data buffer to null (0). The clear operation terminates at the location where the data value matches with the pattern byte (The data frame that follows the command) in conjunction with the Mask Register, or terminates at address 0 if no match has been found. All the locations from the starting address up to the matched location (Not included) are cleared. The address counter contains the matching location address. The corresponding locations of the EAB are also cleared to nulls under the control of the EAB Mask register.

In 78E mode, bit 6 (Buffer being modified) of the PC Adapter Interrupt Status register is set at the beginning of the command. At the completion of the command, this bit is reset and bit 4 (Base buffer modified complete) of the register is set.

Start Operation:

This command is supported in both DFT and 87E modes. In DFT mode, TT/AR is returned, bit 0 (Start Operation command) of the Adapter Interrupt Status register is set at the decoding of the command. For 87E mode, the response is same except that no action is taken if there is any pending status. Bit 7 (Enable operation) of the 87E Status register is also set in this mode.

Read Terminal ID:

The response of this command is the return of the following data byte:

<table>
<thead>
<tr>
<th>Mode</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78E</td>
<td>b2-5</td>
<td>Keyboard ID.</td>
</tr>
<tr>
<td></td>
<td>b6-8</td>
<td>Terminal ID.</td>
</tr>
<tr>
<td></td>
<td>b9</td>
<td>0</td>
</tr>
<tr>
<td>87E</td>
<td>b2-8</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>b9</td>
<td>1</td>
</tr>
<tr>
<td>DFT</td>
<td>b2-8</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>b9</td>
<td>1</td>
</tr>
</tbody>
</table>
In DFT mode, the decoding of this command sets bit 3 (Read Terminal ID command) of the PC Adapter Interrupt Status register. In 87E and 78E modes, it reset bit 9 and bit 11 (operation complete and feature error) of the status word.

Load Control Register:
This command loads the next data frame into the Visual/Sound Register (2D1) or IRMA Auxiliary Register.

The function of each bit is listed as follows:

<table>
<thead>
<tr>
<th>Frame Bits</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>80 characters per line if this bit is &quot;0&quot;. 132 characters if &quot;1&quot;.</td>
</tr>
<tr>
<td>5</td>
<td>Inhibit feature step of the buffer address counter.</td>
</tr>
<tr>
<td>6</td>
<td>Inhibit display.</td>
</tr>
<tr>
<td>7</td>
<td>Inhibit cursor display.</td>
</tr>
<tr>
<td>8</td>
<td>Reverse image cursor.</td>
</tr>
<tr>
<td>9</td>
<td>Cursor blinking.</td>
</tr>
</tbody>
</table>

In 78E mode, bit 2 of the PC Adapter Interrupt Status (Visual/Sound Register Updated) will be set to "1" at the completion of this command.

Read Multiple:
The Read Multiple will cause the chip to return one or more data words from buffer memory beginning at the current buffer address counter. The counter increments by one each time the buffer is accessed. The maximum number the chip can read depends on the Secondary Control Register bit 0. If this bit is "0", the read will terminate when the two low order bits of the buffer address counter becomes "00" which gives a maximum of 4 bytes of reading data. If it is "1", the read will terminate when the five low order bits of the counter becomes "00000" and give a maximum of 32 bytes of data.

Write Data:
The decoding of the Write Data command will cause the chip to put all the following data frames into the buffer memory until another command is received. The buffer address counter increments by one for every data written. In 78E mode, the 1st data word following the command sets bit 6 (Buffer being modified) of the PC Adapter Interrupt Status register. At the completion of the command, bit 4 of the register (Base buffer modified complete) is set.

Read Status:
In 78E and 87E modes, the return of this command is as follows:

Frame bit 1: Sync bit
bit 2-3: 0
bit 4: "1" for not busy
bit 5-6: 0
bit 7: "1" for feature error
bit 8: "1" for operation complete
bit 9-11: 0
bit 12: Frame parity

Insert:
This command causes the chip to accept the following data frame and put it in the buffer storage at the current address counter location. The old storage data is shifted one location ahead. This process continues for each successive location until a null (00) character or attribute is found, or the address counter steps to zero.

The EAB (Extended attribute buffer) is also shifted with the contents of the EAB Mask register being inserted at the initial location.

In 78E mode, bit 6 of the PC Adapter Interrupt Status Register (Buffer being modified) is asserted at the beginning of command. At the completion of the command, this bit is de-asserted and bit 4 (base buffer modified complete) is set.
Search Forward:
This command is supported in 78E and 87E modes only. The command causes the chip to search for each buffer storage starting with the current address counter. This process will keep on going until a match in the pattern byte (The data frame that follows the command). The bit comparison happens only on the bit with corresponding mask bit equal to “1”. The address counter increments by one after each comparison. The address counter contains the value of the buffer address of the first matched data. The search will terminate at address 0 if no match is found.

Poll Acknowledge:
This command is sent by the control unit when it receives the non-zero status. TT/AR is returned by the chip after receiving this command. If the chip receives a second Poll command instead of Poll Acknowledge, it will return the same status. In the case that a new status is available before the first returned status is acknowledged, the new status will be stacked by the chip.

In 78E mode, if the sending of the keystroke is acknowledged by the control unit, the receiving of this command will set bit 0 (Keystroke Accepted) of the Interrupt Status register.

If this command contains the sound alarm or enable/disable clicker in 78E mode or enable/disable operation in 87E mode, it will set bit 2 (Visual/Sound Register Updated) of the Interrupt Status register.

Search Backward:
The operation of Search Backward command is similar to Search Forward command except that the address counter decrements by one after each comparison. If no byte match is found the search will terminate at one location past address 0. (Address counter bits 0 to 11 are set to “1”).

Load Address Low:
Similar to Load Address High command, this command causes the chip to load the next data frame into the low byte of the buffer address counter. In 78E mode, the decoding of the command sets bit 5 of the PC-Adapter Interrupt Status register.

Read Address Low:
Similar to Read Address High command, the content of buffer address low counter is returned in response to this command.

It is ignored in DFT mode.

Load Mask:
This command causes the chip to load the next byte into the mask register. The mask register is used with Search and Clear commands. A “1” bit in the mask enables the bit in the buffer to compare with the pattern byte. Load Mask command is supported in 78E and 87E modes only.

Load Secondary Control Register:
The decoding of this command interprets the data byte following the command as the control bit for the Read Multiple command. If b0 is “0”, the termination of Read Multiple command will be 0 to 4 bytes. If it is “1”, the termination will be 0 to 32 bytes.

Diagnostic Reset:
This command is supported in DFT mode only. It is ignored in both 78E and 87E modes. In DFT mode, the response of this command will be the return of TT/AR and the setting of bit 2 in PC Adapter Interrupt Status register.
Table 2

<table>
<thead>
<tr>
<th>Command Name</th>
<th>Command Code B5-B9</th>
<th>R/W</th>
<th>CUT Mode Display</th>
<th>CUT Mode Printer</th>
<th>DFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poll</td>
<td>00001</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Reset</td>
<td>00010</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Read Data</td>
<td>00011</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Load Address Counter High</td>
<td>00100</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Read Address Counter High</td>
<td>00101</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Clear</td>
<td>00110</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Start Operation</td>
<td>01000</td>
<td>W</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Read Terminal ID</td>
<td>01001</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Load Control Register</td>
<td>01010</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Multiple</td>
<td>01011</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>Write Data</td>
<td>01100</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Read Status</td>
<td>01101</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Insert</td>
<td>01110</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Search Forward</td>
<td>10000</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Poll Acknowledge</td>
<td>10001</td>
<td>R</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Search Backward</td>
<td>10010</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Load Address Counter Low</td>
<td>10100</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Read Address Counter Low</td>
<td>10101</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Load Mask</td>
<td>10110</td>
<td>W</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>Load Secondary Control Register</td>
<td>11010</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>Diagnostic Reset</td>
<td>11100</td>
<td>W</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
</tbody>
</table>

Selector Pen Feature:

Table 3 lists the selector pen feature supported by 82C570 internal microcode. The explanation of each command is as follows:

POLL: The status response is the same as in the base feature.

READ ROW COUNT: The response of this command will send the row count indicating the display row detected.

READ FEATURE ID: 25H will be returned as the feature ID.
Table 3

<table>
<thead>
<tr>
<th>Command Name</th>
<th>Command Code b6-b9</th>
<th>R/W</th>
<th>CUT Mode Display</th>
<th>CUT Mode Printer</th>
<th>DFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poll</td>
<td>0001</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Row Count</td>
<td>0011</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Feature ID</td>
<td>01X1</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Selector</td>
<td>1111</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
</tbody>
</table>

Extended Character Set Feature:

Table 4 lists the extended character set feature supported by 82C570 internal microcode. The description of each command is as follows:

Read Data:

The operation of this command is similar to base Read Data command except that the buffer address counter is incremented after the data reading only when bit 1 = "0" (Inhibit Feature Step of I/O Address Counter) in the Visual/Sound Register.

Read Feature ID:

"79"H is returned which means color and no program symbol is supported.

Read Multiple:

If bit 5 of the Control Register is "1", TT/AR is returned and no other action is taken. If this bit is "0", the operation is similar to base Read Multiple command.

Write Alternate:

The data bytes following the command are written into the display data buffer and the EAB buffer alternately, starting with the data buffer. The writing of EAB buffer is "under mask" just like the Write Under Mask command. The address counter will increment by one after the byte is written into EAB if bit 1 of the Visual/Sound Register is "0".

Load EAB Mask:

This command stores the following data byte into the EAB Mask Register (One of the 15 working registers in the microcontroller). It is used in the base Clear command, feature Write Under Mask and Write Alternate commands.

Write Under Mask:

The operation of this command is "NEW EAB = ( NOT (MASK) AND (OLD EAB) ) OR (DATA BYTE)". A "1" bit in the data byte (The data frame that follows the command) always sets the corresponding EAB bit. The New EAB bit will be "0" only under two conditions: 1) Mask bit = "1" and the corresponding data bit is "0". 2) Mask bit = "0", Old EAB bit is "0" and the corresponding data bit is "0". At the completion of the writing, the buffer address counter will increment by one if bit 1 of the Visual/Sound Register is "0".

Read Status:

"20"H is returned for the decoding of this command.
### Table 4

<table>
<thead>
<tr>
<th>Command Name</th>
<th>Command Code b6-b9</th>
<th>R/W</th>
<th>CUT Mode Display</th>
<th>CUT Mode Printer</th>
<th>DFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read Data</td>
<td>0011</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Load EAB Mask</td>
<td>0101</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Feature ID</td>
<td>01X1</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Write Alternate</td>
<td>1010</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Multiple</td>
<td>1011</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Write Under Mask</td>
<td>1100</td>
<td>W</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Read Status</td>
<td>1101</td>
<td>R</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
</tbody>
</table>
### 82C570 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>( V_{CC} )</td>
<td>7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>( V_I )</td>
<td>-0.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>( V_O )</td>
<td>-0.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>( T_{OP} )</td>
<td>-25</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>( T_{STG} )</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

### 82C570 Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>( V_{CC} )</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>( T_A )</td>
<td>0</td>
<td>70</td>
<td>°C</td>
</tr>
</tbody>
</table>

### 82C570 DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Current</td>
<td>( I_{CC} )</td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>( V_{IL} )</td>
<td>-0.5</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Input High Voltage (except X1)</td>
<td>( V_{IH} )</td>
<td>2.0</td>
<td>( V_{CC}+0.5 )</td>
<td>V</td>
</tr>
<tr>
<td>Input High Voltage for X1</td>
<td>( V_{IH} )</td>
<td>3.5</td>
<td>( V_{CC}+0.5 )</td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage (note 1)</td>
<td>( V_{OL} )</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output High Voltage (note 1)</td>
<td>( V_{OH} )</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>( I_{IL} )</td>
<td>-10</td>
<td>10</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>For ( V_{IN} = 0 ) to ( V_{CC} )</td>
<td>( I_{OL} )</td>
<td>-10</td>
<td>10</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

**Note 1:**
- \( I_{OL} \) = 12mA \( I_{OH} \) = -4mA for pins IRQ READY.
- \( I_{OL} \) = 24mA \( I_{OH} \) = -4mA for IRQ1 pin.
- \( I_{OL} \) = 4mA \( I_{OH} \) = -2mA for all other pins.

### Capacitance (\( T_A = 25^\circ \text{C}, V_{CC} = 0 \))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance</td>
<td>( C_{IN} )</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>For ( f_C = 1 ) MHz</td>
<td>( C_{OUT} )</td>
<td>20</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>I/O Capacitance</td>
<td>( C_{I/O} )</td>
<td>20</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>
### 82C570 AC Characteristics

(T<sub>A</sub> = 0° C to 70° C, V<sub>CC</sub> = 5V ± 5%, C<sub>L</sub> = 60 pF for all the outputs)

<table>
<thead>
<tr>
<th>Sym</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Processor Interface Timing</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t1</td>
<td>Address Set-Up to Command Active</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t2</td>
<td>AEN Set-Up to Command Active</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t3</td>
<td>AEN Hold from Command Inactive</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t4</td>
<td>Address Hold from Command Active</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t5</td>
<td>I/O Command Pulse Width</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t6</td>
<td>Data Read Delay time</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t7</td>
<td>Data Hold from IORD Inactive</td>
<td>8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t8</td>
<td>BCS Asserts Delay time</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t9</td>
<td>BCS Deasserts Delay time</td>
<td>10</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t10</td>
<td>Data Set-Up to IOWR Inactive</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t11</td>
<td>Data Hold from IOWR Inactive</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t12</td>
<td>READY Asserts Delay from MEMRD/MEMWR Active</td>
<td>220</td>
<td>460</td>
<td>ns</td>
</tr>
<tr>
<td>t13</td>
<td>Data Valid before Ready Asserts</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t14</td>
<td>Data Hold from MEM RD Inactive</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t15</td>
<td>READY Deasserts Delay from MEMRD/MEMWR Active</td>
<td></td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t16</td>
<td>READY Tri-state Delay from MEMRD/MEMWR Inactive</td>
<td></td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t17</td>
<td>Data Set-Up to READY Active</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t18</td>
<td>Data Hold from MEM WR Inactive</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

|     | **Buffer RAM Interface timing**              |     |     |       |
| t21 | RAM Write cycle time                         | 135 |     | ns    |
| t22 | RAM Write cycle Address Hold from MCS1/MCS2 Inactive |     | 10  | ns    |
| t23 | RAM Write cycle Address Hold from RAMWR Inactive |     | 10  | ns    |
| t24 | RAMWR Pulse Width                            | 85  |     | ns    |
| t25 | Address Valid to RAMWR Active                | 20  |     | ns    |
| t26 | Data Valid to End of Write                   | 60  |     | ns    |
| t27 | Data Hold from End of Write                  | 5   |     | ns    |
### 82C570 AC Characteristics (Continued)

(T<sub>D</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ± 5%, C<sub>L</sub> = 60 pF for all the outputs)

<table>
<thead>
<tr>
<th>Sym</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Buffer RAM Interface timing (Continued)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t28</td>
<td>MCS1/MCS2 Active to End of Write</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t29</td>
<td>Address Valid to End of Write</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t30</td>
<td>RAM Read cycle time</td>
<td>135</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t31</td>
<td>Address Access time</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t32</td>
<td>Data Valid from MCS1/MCS2 Active</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t33</td>
<td>Data Valid from RAMRD Active</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t34</td>
<td>Output Hold from Address changes</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td><strong>Serial interface timing</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t41</td>
<td>TXDLY Delay time from TXD</td>
<td>100</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td>t42</td>
<td>Transmit Data bit cell time</td>
<td>423.92</td>
<td>424.0048</td>
<td>ns</td>
</tr>
<tr>
<td>t43</td>
<td>Transmit Data half bit cell time</td>
<td>209</td>
<td>215</td>
<td>ns</td>
</tr>
<tr>
<td>t44</td>
<td>TXD first high going Delay from TXACT Active</td>
<td>205</td>
<td>220</td>
<td>ns</td>
</tr>
<tr>
<td>t45</td>
<td>Maximum Receive Input Data</td>
<td>±35</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Jitter DPLL can tolerate</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Miscellaneous timing</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t51</td>
<td>X1 Rise time</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t52</td>
<td>X1 Fall time</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t53</td>
<td>X1 High time</td>
<td>20</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t54</td>
<td>X1 Low time</td>
<td>20</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>t55</td>
<td>X1 Cycle time</td>
<td>52.9899</td>
<td>53.0005</td>
<td>ns</td>
</tr>
<tr>
<td>t56</td>
<td>RESET Active time</td>
<td>1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t57</td>
<td>IRQ Pulse Width</td>
<td>100</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>t58</td>
<td>IRQ1 Deasserts from iOWR Inactive</td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Notes:** AC measurements are done at: TTL output: High level = 2.0 V Low level = 0.8 V. Input swing is at least 0.4 V to 2.4 V with 3-10 ns rise and fall times. High time is measured at 3.0V Low time is measured at 0.6V.
Crystal Specification

The crystal required in the X1, X2 inputs should meet the following requirements.

Resonant Frequency
(\(CL = 20 \text{ pF}\)) ............... 18.8696 MHz
Type .................. Fundamental Mode
Circuit .................. Parallel Resonance
Load Capacitance (CL) .............. 20 pF
Shunt Capacitance (CO) ........ 7 pF Max.

Equivalent
Series Resistance (R1) .......... 25 Ohm Max.
Motional Capacitance (C1) ... 0.02 pF Max.
Drive Level ...................... 2 mW
Accuracy .. at 18.8696MHz ±0.002% at 25°C
........... at 18.8696MHz ±0.005%
for 0-70°C

Also, instead of the crystal at the X1, X2 inputs, an alternate TTL input may be connected at X1 input and floating X2.
82C570 Timing Diagrams

Processor Interface Timing

I/O Read

I/O Write
Memory Read

\[\text{AEN}\]

\[\text{A0-19}\]

\[\text{MEMRD}\]

\[\text{D0-7}\]

\[\text{READY}\]

\[\text{BCS}\]

\[\text{MA0-12}\]

\[\text{MCS}_1 / \text{MCS}_2\]

\[\text{RAMRD}\]

\[\text{MD0-15}\]
Memory Write

82C570 Timing Diagrams (Continued)
82C570 Timing Diagrams (Continued)

Buffer RAM Interface Timing

**Write Cycle**

- **MA0-12**: VALID (21)
- **MCS1 / MCS2**: (22)
- **RAMWR**: (23)
- **MD0-15**: VALID (24)

**Read Cycle**

- **MA0-12**: VALID (25)
- **MCS1 / MCS2**: (26)
- **RAMRD**: (27)
- **MD0-15**: VALID (28)
**82C570 Timing Diagrams** (Continued)

**Serial Interface Timing**

**Transmit**

- **TXD**
- **TXDLY**
- **TXACT**

**Receive**

- **RXD**

**Miscellaneous Timing**

- **X1**
- **RESET**
- **IRQ₁**
- **IOWR**
- **IRQ₂**
84-PIN PLASTIC LEADED CHIP CARRIER

Ordering Information

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>P82C570</td>
<td>PLCC-84</td>
</tr>
</tbody>
</table>

Note:
1. PLCC = Plastic Leaded Chip Carrier
CANADA DISTRIBUTORS

Electro Source Inc.
39 Robertson Rd., Ste. 233
The Bell Mews Mall
Nepean, Ontario
Canada K2H 8R2
Phone: 613-726-1452
Fax: 613-726-8834

Electro Source, Inc.
230 Galaxy Blvd.
Rexdale, Ontario
Canada M9W 5R8
Phone: 416-675-4490
Telex: 6-989271

Electro Source Inc.
6600 TransCanada Hwy.
Suite 510
Pointe Claire, Quebec
Canada H9R 4S2
Phone: 514-694-0404
Fax: 514-694-8501

U.S. DISTRIBUTORS

ALABAMA

Quality Components
4900 University Square
Suite 20
Huntsville, AL 35816
Phone: 205-830-1881

Hall-Mark
4900 Bradford Drive
Huntsville, AL 35816
Phone: 205-837-8700

ARIZONA

Anthem
1727 East Webber Drive
Tempe, AZ 85281
Phone: 602-966-6600

Hall-Mark
4040 E. Raymond
Phoenix, AZ 85040
Phone: 602-437-1200

CALIFORNIA

Anthem
20640 Bahama Street
Chatsworth, CA 91311
Phone: 818-700-1000

CONNECTICUT

Lionex
170 Research Parkway
Meriden, CT 06450
Phone: 203-237-2282

Hall-Mark
33 Village Lane
Wallingford, CT 06492
Phone: 203-269-0100

FLORIDA

Hall-Mark
15302 Roosevelt Blvd.
Suite 303
Clearwater, FL 33752
Phone: 813-530-4543

Hall-Mark
7648 Southland Blvd.
Suite 100
Orlando, FL 32809
Phone: 305-855-4020

ILLINOIS

Hall-Mark/N.C. Regional Systems Warehouse
210 Mittel Drive
Wood Dale, IL 60191
Phone: 312-680-3800

INDIANA

Hall-Mark
4275 W. 96th Street
Indianapolis, IN 46268
Phone: 317-872-8875
800-423-6638 (INDIANA)
800-772-0112 (KENTUCKY)
KANSAS
Hall-Mark/Kansas City
10809 Lakeview Drive
Lenexa, KS 66215
Phone: 913-888-4747

Lionex
311 Route 46 West
Fairfield, NJ 07006
Phone: 201-227-7960

Hall-Mark
107 Fairfield Road Ste. 1B
Fairfield, NJ 07006
Phone: 201-575-4415

Hall-Mark
1000 Midlantic Drive
Mt. Laurel, NJ 08054
Phone: 609-235-1900

Lionex
36 Jonspin Road
Wilmington, MA 01887
Phone: 617-657-5170

MASSACHUSETTS
Hall-Mark
6 Cook Street
Billerica, MA 01821
Boston 617-935-9777
Phone: 617-667-0902

Lionex
36 Jonspin Road
Wilmington, MA 01887
Phone: 617-657-5170

MARYLAND
Hall-Mark/Baltimore
10240 Old Columbia Road
Columbia, MD 21046
Phone: 301-988-9800

Lionex
9020A Mendenhall Court
Columbia, MD 21045
Phone: 301-964-0040

MICHIGAN
Hall-Mark
10300 Valley View
Eden Prairie, MN 55344
Phone: 612-941-2600

Missouri
Hall-Mark
10240 Old Columbia Road
Columbia, MD 21046
Phone: 301-988-9800

Lionex
9020A Mendenhall Court
Columbia, MD 21045
Phone: 301-964-0040

MINNESOTA
Hall-Mark
10300 Valley View
Eden Prairie, MN 55344
Phone: 612-941-2600

Lionex
9020A Mendenhall Court
Columbia, MD 21045
Phone: 301-964-0040

MISSOURI
Hall-Mark/St. Louis
13750 Shoreline Drive
Earth City, MO 63045
Phone: 314-291-5350

Lionex
9020A Mendenhall Court
Columbia, MD 21045
Phone: 301-964-0040

NEW JERSEY
Lionex
311 Route 46 West
Fairfield, NJ 07006
Phone: 201-227-7960

Hall-Mark
107 Fairfield Road Ste. 1B
Fairfield, NJ 07006
Phone: 201-575-4415

Hall-Mark
1000 Midlantic Drive
Mt. Laurel, NJ 08054
Phone: 609-235-1900

Lionex
36 Jonspin Road
Wilmington, MA 01887
Phone: 617-657-5170

NEW YORK
Hall-Mark
101 Comac Loop
RonKoKoMa, NY 11779
Phone: 516-737-0600

Lionex
400 Oser Avenue
Hauppauge, NY 11787
Phone: 516-273-1660

OHIO
Hall-Mark
5821 Harper Road
Solon, OH 44139
Phone: 216-349-4632

Hall-Mark
400 E. Wilson Bridge Road
Suite 5
Worthington, OH 43085
Phone: 614-888-3313

OKLAHOMA
Hall-Mark
2265 S. 1300 West
West Valley, UT 84119
Phone: 801-972-1008

OREGON
Anthem
1615 West 2200 South
Salt Lake City, UT 84119
Phone: 801-973-8555

Quality Components
5020 148th Avenue N.E.
Redmond, WA 98052
Phone: 206-881-0850

WISCONSIN
Hall-Mark
16255 W. Lincoln Avenue
New Berlin, WI 53151
Phone: 414-797-7844
FAR EAST DISTRIBUTORS
American MITAC Corporation
3385 Visa Court
Santa Clara, CA 95054
U.S.A.
Phone: 408-988-0258
Telex: 910382201 MECTEL
Fax: 408-980-9742

AUSTRALIA
R&D Electronics
4 Florence Street
Burwood, Victoria
Australia 3125
Phone: 61-3-288 8911
Fax: 61-3-2889168

HONG KONG
Wong's Kong King Ltd.
8/F Sime Darby Ind. Bldg.
420 Kwun Tong Road
Kwun Tong, Hong Kong
Phone: 852 3-450121
Telex: 36810 WKKL HX
Fax: 852 3-7551128

ISRAEL
Hitek Ltd.
45, Basel St.
TEL-AVIV, ISRAEL
Phone: 972 03/457917
Telex: 922361HTK1

JAPAN
ASCII Corporation
SAT-1 Bldg., 3F
2-20-4, Minami Aoyama
Minato-ku
Tokyo 107 Japan
Phone: 03-470-0486
Telex: J28764ASCII
Fax: 03-470-0522

KOREA
Kortronics Enterprises
Rm. 307 9-Dong B-Block
#604-1 Guro-Dong, Guro-Gu
Seoul, Korea
Phone: 82 2 635-1043
Fax: 82 2 675-0514

SINGAPORE
Computer Engineering Systems PTE, Ltd.
73 Ayer Rajah Crescent
#02-14/21
Ayer Rajah Industrial Estate
Singapore 0513
Phone: 7797377
Telex: RS25223 CESPL
Fax: 657787142

TAIWAN, R.O.C.
Micro Electronic Inc.
(Head Office)
8th Fl., 585 Ming Sheng E. Rd.
Taipei, Taiwan
R.O.C.
Phone: 886(02)5018231
Telex: 11942 TAIAUTO
Fax: 886-2-5014265

EUROPEAN DISTRIBUTORS
BELGIUM
Auriema Belgium S.A./N.V.
Rue Brogniezstraat 172-A
B-1070 Bruxelles
Brussels
Phone: (02) 523-62-95
Telex: 21646

FINLAND
OY Fintronic AB
Melkonkatu 24A
SF-00210
Helsinki, Finland
Phone: 358 06926022
Telex: 857124224 FTRON SF
Fax: 358 0 674886

FRANCE
A2M
6, Av. du General de Gaulle
78150 Le Chesnay
France
Phone: 33 39.54.91.13
Telex: 842698376 F
Fax: 331 39.54.30.61

GERMANY
Rein Elektronik GmbH
Loetscher Weg 66
Postfach 5160
D-4054 Nettetal 1
West Germany
Phone: 49 (02153) 733-0
Telex: 84185423B REIN D
Fax: 49 02153-733110

ITALY
Eledra S.p.A.
Via G. Watt 37
20143 Milano
Viale Elvezia 18
Italy
Phone: 39 (02) 81.82.1
Telex: 843332332
Fax: 39 (02) 81.82.211

NETHERLANDS
Auriema Nederland B.V.
Doornakkersweg 26
5642 MP Eindhoven
Netherlands
Phone: 31 (0) 40-816565
Telex: 84451992
Fax: 31 (0) 40-811815

SPAIN
Compania Electronica de Tecnicas Aplicadas, S.A.
(Comella) (Main Branch)
Emilio Munoz, num. 41
nave 1-1-2
28037 Madrid, Spain
Phone: 34 754 30 01
Telex: 83142007 CETA E
Compania Electronica de Tecnicas Aplicadas, S.A.
(Comella)
Pedro IV, num. 84-5 planta
08005 Barcelona, Spain
Phone: 300 77 12 (8 lineas)
Telex: 8315934 CETA E
SWEDEN (Nordic Countries)
Nordisk Elektronik A.B.
(Main Branch)
Box 1409
S-171 27 Solna
Sweden
Phone: 46 08-734 97 70
Fax: 46 08-27 22 04
Telex: 85410547 NORTRON S
Nordisk Elektronik A/S
P.O. Box 123
Smedsvingen 4
1364 Hvalstad
Norway
Phone: 47 02 84 62 10
Fax: 47 02 84 65 45
Telex: 85677546 NENASN
Nordisk Elektronik A/S
Transformervej 17
DK-2730 Herlev
Denmark
Telex: 85535200 NORDEL DK

SWITZERLAND
DataComp
Silbernstrasse 10
CH-9853 Dietikon
Switzerland
Phone: 41 01 740 51 40
Telex: 827750 DACO
Fax: 41 1-7413423

UNITED KINGDOM
Katakana Limited
Manhattan House
Bridge Road
Maidenhead, Berkshire
SL6 8DB
United Kingdom
Phone: Maidenhead 44
(0628) 75641
Telex: 846775 KATKAN
Fax: 44 (0628) 782812

CANADA SALES REPRESENTATIVES
Electro Source Inc.
39 Robertson Rd., Ste. 233
The Bell Mews Mall
Nepean, Ontario
Canada K2H 8R2
Phone: 613-726-1452
Fax: 613-726-8834
Electro Source Inc.
215 Carlingview Drive
Suite 303
Rexdale, Ontario, Canada
M9W 5X8
Phone: 416-675-4490
Fax: 416-694-0404
Fax: 514-694-8501

REGIONAL SALES OFFICES
NORTHEAST REGION:
SALES OFFICE
Chips & Technologies, Inc.
One Wall Street
Burlington Office Park
Burlington, MA 01803
Phone: 617-273-3500
Fax: 617-273-5394

MID-AMERICA REGION:
SALES OFFICE
Chips & Technologies, Inc.
15415 Katy Freeway
Suite 209
Houston, TX 77094
Phone: 713-579-9633
Fax: 713-579-9557

WESTERN REGION:
SALES OFFICE
Chips & Technologies, Inc.
18201 Von Karman Ave.
Suite 310
Irvine, CA 92715
Phone: 714-852-8721
Fax: 714-852-8912
U.S. SALES REPRESENTATIVES

ALABAMA
The Novus Group, Inc.
2905 Westcorp Blvd.
Suite 120
Huntsville, AL 35805
Phone: 205-534-0044

ARIZONA
Reptronix
1729 E. McLellan Road
Mesa, AZ 85203
Phone: 602-964-2362

CALIFORNIA
Magna Sales
3333 Bowers Avenue
Suite 251
Santa Clara, CA 95054
Phone: 408-727-8753

S.C. Cubed
468 Pensfield Place
Suite 101A
Thousand Oaks, CA 91360
Phone: 805-496-7307

COLORADO
Wescom Marketing, Inc.
4851 Independence Street
Suite 159
Wheat Ridge, CO 80033
Phone: 303-422-8957

FLORIDA
Dyne-A-Mark Corporation
573 South Duncan Avenue
Clearwater, FL 33756
Phone: 813-441-4702
Tampa: 813-223-7969

New Jersey
T.A.I.
12 South Blackhorse Pike
Bellmawr, New Jersey 08031
Phone: NJ: 609-933-2600
PA: 215-627-6615

NEW MEXICO
Reptronix
237-C Eubank Blvd. NE
Albuquerque, NM 87123
Phone: 505-292-1718

NEW YORK
ERA, Incorporated
351 Veterans Memorial Hwy.
Commack, NY 11725
Phone: 516-543-0510

L-Mar Associates
349 W. Commercial St.
Suite 2285
E. Rochester, NY 14445
Phone: 716-381-9100

MASSACHUSETTS
Mill-Bern Associates, Inc.
2 Mack Road
Woburn, MA 01801
Phone: 617-932-3311

MICHIGAN
Giesting & Associates
5654 Wendzel Drive
Coloma, MI 49038
Phone: 616-468-4200

MINNESOTA
High Technology Sales Assoc.
11415 Valley View Road
Eden Prairie, MN 55344
Phone: 612-944-7274

NEW CAROLINA
The Novus Group, Inc.
5337 Trestlewood Lane
Raleigh, NC 27610
Phone: 919-833-7771
OHIO
Giesting & Associates
2854 Blue Rock Road
P.O. Box 39398
Cincinnati, OH 45239
Phone: 513-385-1105

Giesting & Associates
26250 Euclid Avenue
Suite 525
Cleveland, OH 44132
Phone: 216-261-9705

Giesting & Associates
8843 Washington Colony Drive
Dayton, OH 45459
Phone: 513-433-5832

OREGON
L-Squared Limited
15234 NW Greenbrier Pkwy.
Beaverton, OR 97006
Phone: 503-629-8555

PENNSYLVANIA
Giesting & Associates
471 Walnut Street
Pittsburgh, PA 15238
Phone: 412-963-5832

TEXAS
OM Sales
13915 Burnet Road
Suite 301
Austin, TX 78728
Phone: 512-388-1151

OM Sales
10500 Richmond Ave.
Suite 115
Houston, TX 77042
Phone: 713-789-4426

OM Sales
2323 N. Central Expwy.
Suite 150
Richardson, TX 76080
Phone: 214-690-6746

UTAH
Wescom Marketing, Inc.
3499 S. Main
Salt Lake City, UT 84115
Phone: 801-269-0419

WASHINGTON
L-Squared Limited
105 Central Way
Suite 203
Kirkland, WA 98033
Phone: 206-827-8555

WISCONSIN
Micro-Tex, Inc.
22660 Broadway
Suite 3B
Waukesha, WI 53186
Phone: 414-542-5352