Acer Laboratories Inc. M1541/M1542 Preliminary Datasheet

Please contact ALi applications department at 408-467-7456 to verify that all information is current before beginning a design using this datasheet.

AIADDiN™ V

M1541/M1542

Socket 7
North Bridge -

Version 1.20
M1541 : AGP, CPU-to-PCI bridge, Memory, Cache and Buffer Controller

1.1 Features

- **Supports all Socket 7 processors.** Host bus at 100MHz, 83.3MHz, 75MHz, 66 MHz, 60 MHz and 50MHz at 3.3V/2.5V.
  - Supports linear wrap mode for Cyrix M1 & M2
  - Supports Write Allocation feature for K6
  - Supports Pseudo Synchronous AGP and PCI bus access
    - (CPU bus 75MHz - AGP bus 66MHz, PCI bus 30MHz,
    - CPU bus 83.3MHz - AGP bus 66MHz, PCI bus 33MHz,
    - CPU bus 100MHz - AGP bus 66MHz, PCI bus 33MHz)

- **Supports Pipelined-Burst SRAM/Memory Cache**
  - Direct mapped, 256KB/512KB/1MB
  - Write-Back/Dynamic-Write-Back cache policy
  - Built-in 16K*2 bit SRAM for MESI protocol to reduce cost and enhance performance
  - Built-in 16K*10 bit SRAM for TAG data to reduce cost and enhance performance (reserved)
  - Cacheable memory up to 128MB with 8-bit Tag SRAM when using 512KB L2 cache, 256MB when using 256KB L2 cache.
  - Cacheable memory up to 512MB with 10-bit Tag SRAM when using 512KB L2 cache, 1GB when using 256KB L2 cache
  - 3-1-1-1-1-1-1 for Pipelined Burst SRAM/Memory Cache at back-to-back burst read and write cycles.
  - Supports 3.3V/5V SRAMs for Tag Address.
  - Supports CPU Single Read Cycle L2 Allocation.

- **Supports FPM/EDO/SDRAM DRAMS**
  - 64 RAS Lines up to 4G Byte support
  - 64-bit data path to Memory
  - Symmetrical/Asymmetrical DRAMs
  - 3.3V or 5V DRAMs
  - No buffer needed for RASJ and CASJ and MA
  - CBR and RAS-only refresh for FPM
  - CBR and RAS-only refresh and Extended refresh and self refresh for EDO
  - CBR and Self refresh for SDRAM
  - 32 QWORD deep merging buffer for 3-1-1-1-1-1-1-1-1 posted write cycle to enhance high speed CPU burst access
  - 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit
  - 5-2-2-2-2-2-2 for back-to-back EDO read page hit
  - 6-1-1-1-1-1-1-1 for back-to-back SDRAM read page hit

- **Synchronous/Pseudo Synchronous**
  - 25/30/33MHz 3.3V/5V tolerance PCI interface
  - Concurrent PCI architecture
  - PCI bus arbiter: Five PCI masters and M1533/ M1543 (ISA Bridge) and AGP Master supported
  - 6 DWORDs for CPU-to-PCI Memory write posted buffers
  - Converts back-to-back CPU to PCI memory write to PCI burst cycle
  - 30/22 DWORDs for PCI-to-DRAM Write-posted/ Read-prefetching buffers
  - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write back)
  - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
  - Supports PCI mechanism #1 only
  - PCI spec. 2.1 support, (N(32/16/8)+8 rule, passive release, fair arbitration)
  - Enhanced performance for Memory-Read-Link and Memory-Read-Multiple and Memory-write-Invalidate PCI commands.

- **Enhanced Power Management**
  - ACPI support
  - Supports PCI bus CLKRUN function
  - Supports Dynamic Clock Stop
  - Supports Power On Suspend
  - Supports Suspend to Disk
  - Supports Suspend to DRAM
  - Self Refresh during Suspend
- **Accelerated Graphics Port (AGP) Interface**
  - Supports AGP specification V1.0
  - Supports up to 64 entries table look aside buffer for Graphic Address Remapping Table (GART)
  - AGP 86MHz protocol
  - AGP 1X and 2X sideband address function
  - 28 entries Request queue
  - 32 QWORDs Read buffer
  - 16 QWORDs Write buffer

- 35x35 mm 456-pin BGA package
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1.2 Introduction

Aladdin-V is the succeeding generation chipset of ALADDIN-IV from Acer Labs. It maintains the best system architecture (2-chip solution) to achieve the best system performance with the lowest system cost (TTL-free). ALADDIN-V consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for the most engaging multimedia/multithreading OS and software applications. It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and makes the system manufacturing easier.

M1541 includes the higher CPU bus frequency (up to 100 MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and Memory Cache L2 controller, internal MESI tag bits (16Kx2) and TAG RAM (16Kx10) to reduce cost and enhance performance, high performance FPM/EDO/SDRAM DRAM controller, PCI 2.1 compliant bus interface, smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance, and also the highly efficient PCI fair arbiter. M1541 also provides the most flexible 64-bit memory bus interface for the best DRAM upgrade ability and ECC/Parity design to enhance the system reliability.

With the AGP interface design, the dedicated PCI_66 AGP interface is concurrent with CPU and PCI interface. The deep buffer of the read and write buffer design makes the utilization of memory bandwidth more efficient. The interface supports AGP specification V1.0. Supports up to 64 entries of table look aside buffer for Graphic Address Remapping Table (GART). The interface not only supports the AGP 66MHz protocol, but also the AGP 1X and 2X sideband address function.

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access. PCI-to-DRAM access can run concurrently with CPU-to-L2 access. M1541 also supports the snoop ahead feature to achieve the PCI master full bandwidth access (133MBytes). M1541 also provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support Microsoft On Now technology OS.

M1533 provides the best power management system solution. M1533 integrates ACPI support, deep green function, 2-channel dedicated Ultra-33 IDE master controller, 2-port USB controller, SMBus controller, and PS2 Keyboard/Mouse controller. (see figure 1-1)

M1543 provides the best desktop system solution. M1543 integrates ACPI support, green function, 2-channel dedicated Ultra-33 IDE Master controller, 2-port USB controller, SMBus controller, PS/2 Keyboard/Mouse controller and the Super I/O (Floppy Disk Controller, 2 serial port/1 parallel port) support. (see figure 1-2)

In the following diagram, ALADDIN-V gives a highly integrated system solution and a most up-to-date architecture, which provides the best cost/performance system solution for Desktop and also for Notebook vendors.
Figure 1-1

Aladdin V System Block Diagram with M1543

Figure 1-2

Aladdin V System Block Diagram with M1533
Section 2 : Pin Description

2.1 Pinout Diagram

M1541 for ATX, NLX, LPX form factor

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**TOP VIEW**

*Figure 2-1. M1541 Pin Diagram*
Figure 2-2. M1541 Pin Diagram
### M1542

**M1542 for Baby AT form factor**

#### Pinout Diagram

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</table>

Acer Laboratories, Inc., USA, 1830B Bering Drive, San Jose, CA 95112; Tel: 408-467-7456; Fax: 408-467-7474

www.acerlabs.com
### Figure 2-3. M1542 Pin Diagram

- **T**
  - HD: 2
  - HD: 1
  - HD: 0
  - HD: 18
  - SMA: CTJ

- **U**
  - HD: 7
  - HD: 6
  - HD: 5
  - HD: 4
  - HA: 3

- **V**
  - HD: 12
  - HD: 11
  - HD: 10
  - HD: 9
  - HA: 8

- **W**
  - HD: 17
  - HD: 16
  - HD: 15
  - HD: 14
  - HA: 13

- **Y**
  - HD: 21
  - HD: 20
  - HD: 19
  - HD: 18
  - HA: 17

- **AA**
  - HD: 24
  - HD: 23
  - HD: 22
  - HD: 25
  - HA: A

- **AB**
  - HD: 27
  - HD: 26
  - HD: 28
  - HD: 29
  - HA: A

- **AC**
  - HD: 30
  - HD: 31
  - NC: 32
  - HD: 47
  - HD: 51
  - HD: 56
  - HD: 61

- **AD**
  - HD: 33
  - HD: 36
  - HD: 42
  - HD: 44
  - HA: 48

- **AE**
  - NC: 34
  - HD: 39
  - HD: 42
  - HD: 49
  - HD: 53
  - HD: 58
  - HD: 63

- **AF**
  - HD: 35
  - HD: 37
  - HD: 40
  - HD: 46
  - HA: 50

---

**TOP VIEW**
## M1542

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<thead>
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<th>B</th>
<th>C</th>
<th>D</th>
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### Pin Assignments

- **A** (Address)
- **B** (Control)
- **C** (Function)
- **D** (IO)
- **E** (Function)
- **F** (Power)
- **G** (Configuration)
- **H** (Clock)
- **J** (Junction)
- **K** (Logic)
- **L** (Cas)
- **M** (DPL)
- **N** (DPL)
- **P** (MPD)
- **R** (CLK)

### Diagram

![Diagram](image-url)
Figure 2-4. M1542 Pin Diagram
### 2.2. Pin Description Table:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
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<tr>
<td>Host Interface</td>
<td></td>
<td>3.3V/(2.5)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HA[31:3]</th>
<th>I/O</th>
<th>Group A</th>
<th>Host Address Bus Lines. HA[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1541 drives them during inquiry cycles on behalf of PCI masters.</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEJ[7:0]</td>
<td>I</td>
<td>Group A</td>
<td>Byte Enables. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte while BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1541.</td>
</tr>
<tr>
<td>ADSJ</td>
<td>I</td>
<td>Group A</td>
<td>Address Strobe. The CPU will start a new cycle by asserting ADSJ first. The M1541 will not precede to execute a cycle until it detects ADSJ active.</td>
</tr>
<tr>
<td>BRDYJ</td>
<td>O</td>
<td>Group A</td>
<td>Burst Ready. The assertion of BRDYJ means the current transaction is complete. The CPU will terminate the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.</td>
</tr>
<tr>
<td>NAJ</td>
<td>O</td>
<td>Group A</td>
<td>Next Address. It is asserted by the M1541 to inform the CPU that pipelined cycles are ready for execution.</td>
</tr>
<tr>
<td>AHOJ</td>
<td>O</td>
<td>Group A</td>
<td>CPU Ahold Request Output. It connects to the input of CPU AHOJ pin and is actively driven for inquiry cycles.</td>
</tr>
<tr>
<td>EADSJ</td>
<td>O</td>
<td>Group A</td>
<td>External Address Strobe. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1541 will assert this signal to proceed snooping.</td>
</tr>
<tr>
<td>BOFFJ</td>
<td>O</td>
<td>Group A</td>
<td>CPU Back-Off. If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1541 will assert this signal to request CPU floating all its output buses.</td>
</tr>
<tr>
<td>HITMJ</td>
<td>I</td>
<td>Group A</td>
<td>Primary Cache Hit and Modified. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.</td>
</tr>
<tr>
<td>MIOJ</td>
<td>I</td>
<td>Group A</td>
<td>Host Memory or I/O. This bus definition pin indicates the current bus cycle is either memory or input/output.</td>
</tr>
<tr>
<td>DCJ</td>
<td>I</td>
<td>Group A</td>
<td>Host Data or Code. This bus definition pin is used to distinguish data access cycles from code access cycles.</td>
</tr>
<tr>
<td>WRJ</td>
<td>I</td>
<td>Group A</td>
<td>Host Write or Read. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.</td>
</tr>
<tr>
<td>Pin</td>
<td>Group</td>
<td>Description</td>
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<tr>
<td>HLOCKJ</td>
<td>I</td>
<td><strong>Host Lock.</strong> When HLOCKJ is asserted by the CPU, the M1541 will recognize the CPU is locking the current cycles.</td>
<td></td>
</tr>
<tr>
<td>CACHEJ</td>
<td>I</td>
<td><strong>Host Cacheable.</strong> This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.</td>
<td></td>
</tr>
<tr>
<td>KENJ/INV</td>
<td>O</td>
<td><strong>Cache Enable Output.</strong> This signal is connected to the CPU KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1541 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.</td>
<td></td>
</tr>
<tr>
<td>SMIACTJ</td>
<td>I</td>
<td><strong>SMM Interrupt Active.</strong> This signal is asserted by the CPU to inform the M1541 that SMM mode is being entered.</td>
<td></td>
</tr>
<tr>
<td>HD[63:0]</td>
<td>I/O</td>
<td><strong>Host Data Bus Lines.</strong> These signals are connected to the CPU data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.</td>
<td></td>
</tr>
<tr>
<td>MPD[7:0]</td>
<td>I/O</td>
<td><strong>DRAM Parity /ECC check bits.</strong> These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit when MPD[7:0] serves as parity bits.</td>
<td></td>
</tr>
<tr>
<td>Pin Name</td>
<td>Type</td>
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<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>RASJ[7:0] / SCSJ[7:0]</td>
<td>O</td>
<td><strong>Row Address Strobe</strong> (FPM/EDO) of DRAM row</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td><strong>SDRAM Chip Select Strobe (SDRAM)</strong>. These are multifunction pins</td>
<td></td>
</tr>
<tr>
<td>CASJ[7:0] / SDQM[7:0]</td>
<td>O</td>
<td><strong>Column Address Strobes or Synchronous DRAM Input/Output Data Mask</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].</td>
<td></td>
</tr>
<tr>
<td>ECASJ[5/1] / ESDQM[5/1]</td>
<td>O</td>
<td><strong>Extra Column Address Strobes 5 and 1 or Extra Synchronous DRAM Input/Output Data Mask</strong> and 1. These are copies of CASJ[5/1] or SDQM[5/1] signals. These are used to balance the loading at ECC memory configurations mode because these signals are double-loaded.</td>
<td></td>
</tr>
<tr>
<td>MA[14:0]</td>
<td>O</td>
<td><strong>DRAM Address</strong>. These signals are the address lines[14:0] of all DRAMs. The M1541 supports DRAM types ranging from 256K to 256Mbits.</td>
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</tr>
<tr>
<td>SRASJ[3:0]</td>
<td>O</td>
<td><strong>SDRAM Row Address Strobe</strong> The SRASJ[3:0] are multiple copies of SDRAM row address strobe for the loading purpose. When SRASJ[3:0] is sampled active at the rising edge of the SDRAM clock the row address is latched into the SDRAMS.</td>
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</tr>
<tr>
<td>SCASJ[3:0]</td>
<td>O</td>
<td><strong>SDRAM Column Address Strobe</strong> The SCASJ[3:0] are multiple copies of SDRAM column address strobe for the loading purpose. When SCASJ[3:0] is sampled active at the rising edge of the SDRAM clock the Column address is latched into the SDRAMS.</td>
<td></td>
</tr>
<tr>
<td>MWEJ[3:0]</td>
<td>O</td>
<td><strong>DRAM Write Enable</strong>. These are the DRAM write enable signals and behave according to the early-write mechanism, i.e., they activate before the CASJs do. For refresh cycles, it will remain deasserted. For sharing load purpose, the MWEJ[3:0] are multiple copies of the same Memory Write Enable signal.</td>
<td></td>
</tr>
<tr>
<td>MD[63:0]</td>
<td>I/O</td>
<td><strong>Memory Data</strong>. These pins are connected to DRAM data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.</td>
<td></td>
</tr>
<tr>
<td>CLKEN[7:0]</td>
<td>O</td>
<td><strong>SDRAM Clock Enable</strong>. These signals are used as SDRAM clock enable to do self refresh during suspend. For sharing load purposes, the CLKEN[7:0] are multiple copies of the same SDRAM clock enable signal.</td>
<td></td>
</tr>
<tr>
<td>DPLLO</td>
<td>O</td>
<td><strong>DRAM PLL output</strong>. The Clock output sent to external clock buffer then sent to SDRAM as clock source.</td>
<td></td>
</tr>
<tr>
<td>DPLL[1:0]</td>
<td>I</td>
<td><strong>DRAM PLL input</strong>. There are two Feedback clocks. One to compensate the write circuit. One to compensate the read circuit.</td>
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### Secondary Cache Interface

<table>
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<th>Signal</th>
<th>Group</th>
<th>Description</th>
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<tr>
<td>CADVJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Advance.</strong> This signal makes PBSRAM/Memory Cache internal burst address counter advance.</td>
</tr>
<tr>
<td>CADSJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Address Strobe.</strong> This signal connects to PBSRAM/Memory Cache ADSCJ.</td>
</tr>
<tr>
<td>CCSJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Chip Select.</strong> This signal connects to PBSRAM/Memory Cache CE1J to mask ADSPJ and enable ADSCJ sampling.</td>
</tr>
<tr>
<td>GWEJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Global Write Enable.</strong> This signal will write all the byte lanes data into PBSRAM/Memory Cache.</td>
</tr>
<tr>
<td>COEJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Output Enable.</strong> This signal enables the data output driving of PBSRAM/Memory Cache.</td>
</tr>
<tr>
<td>BWEJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Byte-Write Enable.</strong> This signal connects to byte write enable of PBSRAM/Memory Cache.</td>
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Pin Description Table (continued)

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<th>Pin Name</th>
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<td>MKREFRQJ</td>
<td>I/O</td>
<td>Memory Cache REFresh ReQuest /Acknowledge MKREFRQJ connected to DRAM Cache. This signal is normally driven by the Memory cache and will be sampled by M1541 on each rising clock edge. The high state indicates no refresh request by Memory cache. Memory cache will signal a refresh request by driving this signal low for one clock, then driving high for one clock, then tri-state until M1541 grants the request. The M1541 signals refresh acknowledge by driving the signal low for one clock, then driving high for one clock then tri-state until the next request by Memory cache. Upon detecting that M1541 has driven this signal low, DRAM cache will begin a twenty clock refresh cycle and will let the signal float for one clock then drive the signal high until another refresh cycle is required.</td>
</tr>
</tbody>
</table>

TAG Interface 3.3V/5V Tolerance

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIO[9:0]</td>
<td>I/O</td>
<td>SRAM Tag[9:0]. These signals are SRAM tag address bit 10. If only one TAG SRAM is used, it should connect to TIO[7:0]. If system requires more cacheable memory range, another TAG SRAM will be required. The connect sequence is from TIO[8] to TIO[9].</td>
</tr>
<tr>
<td>TAGWEJ</td>
<td>O</td>
<td>Tag Write Enable. This signal, when asserted, will write into the external tag new state and tag addresses.</td>
</tr>
</tbody>
</table>

PCI Interface 3.3V/5V Tolerance

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD[31:0]</td>
<td>I/O</td>
<td>PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions. During Configuration cycle, M1541 will use AD11 as IDSEL and AD12 for PCI-to-PCI bridge IDSEL internally. The AD11 and AD12 should not connect to any PCI device IDSEL pin.</td>
</tr>
<tr>
<td>CBEJ[3:0]</td>
<td>I/O</td>
<td>PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.</td>
</tr>
<tr>
<td>FRAMEJ</td>
<td>I/O</td>
<td>Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1541 on behalf of CPU, or as an input during PCI master access.</td>
</tr>
<tr>
<td>DEVSELJ</td>
<td>I/O</td>
<td>Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.</td>
</tr>
<tr>
<td>IRDYJ</td>
<td>I/O</td>
<td>Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.</td>
</tr>
<tr>
<td>TRDYJ</td>
<td>I/O</td>
<td>Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.</td>
</tr>
<tr>
<td>STOPJ</td>
<td>I/O</td>
<td>Stop. This signal indicates the target is requesting the master to stop the current transaction.</td>
</tr>
<tr>
<td>Pin</td>
<td>Type</td>
<td>Group</td>
</tr>
<tr>
<td>-------</td>
<td>------</td>
<td>-------</td>
</tr>
<tr>
<td>LOCKJ</td>
<td>I/O</td>
<td>Group B</td>
</tr>
<tr>
<td>REQJ[4:0]</td>
<td>I</td>
<td>Group B</td>
</tr>
<tr>
<td>GNTJ[4:0]</td>
<td>O</td>
<td>Group B</td>
</tr>
<tr>
<td>PHLDJ</td>
<td>I</td>
<td>Group B</td>
</tr>
<tr>
<td>PHLDAJ</td>
<td>O</td>
<td>Group B</td>
</tr>
<tr>
<td>PAR</td>
<td>I/O</td>
<td>Group B</td>
</tr>
<tr>
<td>SERRJ/CLKRUNJ</td>
<td>I/O</td>
<td>Group B</td>
</tr>
<tr>
<td>PCIMRQJ</td>
<td>O</td>
<td>Group B</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>-------------</td>
</tr>
<tr>
<td><strong>HCLKIN</strong></td>
<td>I Group B</td>
<td><strong>CPU bus Clock Input.</strong> This signal is used by all of the M1541 logic that is in the Host clock domain.</td>
</tr>
<tr>
<td><strong>RSTJ</strong></td>
<td>I Group B</td>
<td><strong>System Reset.</strong> This pin, when asserted, resets the M1541 state machine, and sets the register bits to their default values. When SUSPENDJ active, the suspend survival circuit will not be reset. When SUSPENDJ is de-asserted, the suspend survival circuit will be reset too.</td>
</tr>
<tr>
<td><strong>PCICLK</strong></td>
<td>I Group B</td>
<td><strong>PCI bus Clock Input.</strong> This signal is used by all of the M1541 logic that is in the PCI clock domain.</td>
</tr>
<tr>
<td><strong>SUSPENDJ</strong></td>
<td>I Group C</td>
<td><strong>Suspend.</strong> When actively sampled, the M1541 will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled. When SUSPENDJ active, the suspend survival circuit will not be reset. When SUSPENDJ is de-asserted, the suspend survival circuit will be reset too.</td>
</tr>
<tr>
<td><strong>CLK32KI</strong></td>
<td>I Group C</td>
<td><strong>32KHz clock</strong> The refresh reference clock of frequency 32KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.</td>
</tr>
<tr>
<td><strong>TESTJ</strong></td>
<td>I Group C</td>
<td><strong>NAND tree test input</strong> Test mode setting input. When setting this signal to Low, M1541 will be at NAND tree test mode. For normal operation, this signal should be pulled high to VDD_C the same power plane supporting DRAM suspend logic.</td>
</tr>
<tr>
<td><strong>AGP interface</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| **ST[2:0]** | O Group B | **Status bus** provides information from the arbiter to a Master on what it may do. ST[2:0] only have meaning to AGP master when its GGNTJ is asserted, otherwise these signals have no meaning and must be ignored. ST[2:0] :  
000 Indicates that previously requested low priority read or flush data is being returned to the master  
001 indicates that previously requested high priority read data is being returned to the master  
010 indicates that the master is to provide low priority write data for a previous enqueued write command  
011 indicates that the master is to provide high priority write data for a previous enqueued write command  
100-110 Reserved  
111 Indicates that the master has been given permission to start a bus transaction. The master may enqueue A.G.P. requests by asserting PIPEJ or start a PCI transaction by asserting FRAMEJ. ST[2:0] are always an output from M1541 and an input to the AGP graphic controller master. |
<table>
<thead>
<tr>
<th>Signal</th>
<th>Type</th>
<th>Group</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBA[7:0]</td>
<td>O</td>
<td>B</td>
<td><strong>Sideband address port</strong> provides an additional bus to pass address and command to the target from the master. SBA[7:0] are outputs from a master and an input to the target. This port is ignored by the target until enabled.</td>
</tr>
<tr>
<td>PIPEJ</td>
<td>I</td>
<td>B</td>
<td><strong>Pipelined</strong> request is asserted by the current master to indicated a full width request is to be enqueued by the target. The master enqueues one request each rising edge of CLK while PIPEJ is asserted. When PIPEJ is deasserted no new requests are across the AD bus. PIPEJ is a sustained tri-state signal from graphics controller and is an input to M1541.</td>
</tr>
<tr>
<td>RBFJ</td>
<td>I</td>
<td>B</td>
<td><strong>Read Buffer Full</strong> indicates if the master is ready to accept previously requested low priority read data or not. When RBFJ is asserted the arbiter is not allow to initiate the return of low priority read data to the master.</td>
</tr>
<tr>
<td>AD_STB0</td>
<td>I/O</td>
<td>B</td>
<td><strong>AD bus Strobe 0</strong> provides timing for 2X data transfer mode on the GAD[15:0] . The agent that is providing data drives this signal.</td>
</tr>
<tr>
<td>AD_STB1</td>
<td>I/O</td>
<td>B</td>
<td><strong>AD bus Strobe 1</strong> provides timing for 2X data transfer mode on the GAD[31:15] . The agent that is providing data drives this signal.</td>
</tr>
<tr>
<td>SB_STB</td>
<td>I</td>
<td>B</td>
<td><strong>Sideband probe</strong> provides timing for SBA[7:0] and is always driven by the A.G.P. compliant master.</td>
</tr>
</tbody>
</table>
### Pin Description Table (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI 66 Interface 3.3V/5V Tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GAD[31:0] I/O Group B</td>
<td>A.G.P. PCI Address and Data Bus Lines. These lines are connected to the A.G.P. PCI bus. AD[31:0] contain the information of address or data for PCI transactions.</td>
<td></td>
</tr>
<tr>
<td>GCBEJ[3:0] I/O Group B</td>
<td>A.G.P. PCI Bus Command and Byte Enables. There are different meanings. Provided command information( Different command than PCI) by the master when requests are being enqueued using PIPEJ. Provides valid byte information during A.G.P&gt; write transactions and is driven by the master. The M1541 drives to “0000” during the return of A.G.P. read data and is ignored by the A.G.P. compliant master.</td>
<td></td>
</tr>
<tr>
<td>GFRAMEJ I/O Group B</td>
<td>Cycle Frame of PCI Buses. Not used at A.G.P. mode. FRAMEJ remains deasserted by its own pull up resistor Only used during PCI operation on A.G.P. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1541 when a PCI transaction is initiated by M1541 or as an input during A.G.P master access.</td>
<td></td>
</tr>
<tr>
<td>GDEVSELJ I/O Group B</td>
<td>Device Select. Not used by A.G.P. Only used during PCI operation on A.G.P. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.</td>
<td></td>
</tr>
<tr>
<td>GIRDYJ I/O Group B</td>
<td>New meaning. GIRDYJ indicates the A.G.P. compliant master is ready to provided all write data for the current transaction. Once GIRDYJ is asserted for a write operation, the master is not allowed to insert wait states. The assertion of GIRDYJ for reads, indicates that the master is ready to transfer a subsequent block of read data. The master is never allowed to insert a wait state during the initial block of read transaction. However, it may insert wait states after each block transfer. There is no GFRAMEJ IRDYJ relationship for A.G.P. transactions. When a PCI transaction is proceeded at AGP bus, this signal is the same definition of PCI spec.V2.1.</td>
<td></td>
</tr>
<tr>
<td>GTRDYJ I/O Group B</td>
<td>New meaning. GTRDYJ indicates the A.G.P. compliant target is ready to provide read data for the entire transaction (When transaction can complete within four clocks) a block or is ready to transfer a (initial or subsequent) block of data, when the transfer required more than four clocks to complete. The target is allowed to insert wait states after each block transfer on both read and write transactions.</td>
<td></td>
</tr>
<tr>
<td>GSTOPJ I/O Group B</td>
<td>Stop. Not used by A.G.P. Only used during PCI operation on A.G.P. This signal indicates the target is requesting the master to stop the current transaction.</td>
<td></td>
</tr>
<tr>
<td>Bus Request signals of PCI Masters. Same as PCI. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter. As AGP signal, it is used to request bus ownership when PIPEJ (not SBA[7:0]) is used to enqueue AGP request.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Group B</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Grant signals to PCI Masters. Same meaning as PCI. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus. Additional information is provided on ST[2:0]. The additional information indicates that the master is the recipient of previously requested read data (high or low priority), it is to provide write data (high or low priority), for a previously enqueued write command or has been given permission to start a bus transaction (A.G.P. or PCI) |
| Group B |

| Parity bit of PCI bus. Not used by A.G.P. Used during PCI operation on A.G.P.. It is the even parity bit across GAD[31:0] and GCBEJ[3:0]. |
| Group B |

| System Error. Same as PCI. Maybe used by an A.G.P. compliant master to report a catastrophic error when the core logic supports a GSERRJ pin for the A.G.P. port. |
| Group B |

| Parity Error. Not used by A.G.P. For PCI operation per exception granted by PCI 2.1 specification. |
| Group B |

| Clock provides timing for A.G.P and PCI operation on A.G.P. |
| Group B |
## Pin Description Table (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Pins</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD_A</td>
<td>P</td>
<td><strong>VDD 3.3V or 2.5V Power for CPU interface Group_A.</strong> This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.</td>
</tr>
<tr>
<td>VDD_B</td>
<td>P</td>
<td><strong>VDD 3.3V Power for Group_B.</strong> This power is used for AGP interface, PCI interface, Tag interface, L2 cache control signals and internal core circuit. It must connect to 3.3V.</td>
</tr>
<tr>
<td>VDD_C</td>
<td>P</td>
<td><strong>VDD 3.3V Power for Memory interface for Group_C.</strong> This power is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.</td>
</tr>
<tr>
<td>VDD_5</td>
<td>P</td>
<td><strong>VDD 5.0V Power for Group B.</strong> This pin supplies the 5V input tolerance circuit.</td>
</tr>
<tr>
<td>VDD_5S</td>
<td>P</td>
<td><strong>VDD 5.0V Power for Group C.</strong> This pin supplies the memory interface 5V input tolerance circuit.</td>
</tr>
<tr>
<td>VDD_P</td>
<td>P</td>
<td><strong>PLL analog 3.3V VDD : for internal PLL VDD 3.3V.</strong></td>
</tr>
<tr>
<td>VSS_P</td>
<td>P</td>
<td><strong>PLL analog 3.3V VSS : for internal PLL VSS.</strong></td>
</tr>
<tr>
<td>Vref</td>
<td>P</td>
<td><strong>Reference voltage for A.G.P. interface :</strong> Input reference voltage for differential input. It equals to 0.4VDD_B.</td>
</tr>
<tr>
<td>Vss</td>
<td>P</td>
<td><strong>Ground.</strong></td>
</tr>
</tbody>
</table>
## 2.3 Numerical Pin List

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>HD35</td>
<td>I/O</td>
</tr>
<tr>
<td>A2</td>
<td>HD37</td>
<td>I/O</td>
</tr>
<tr>
<td>A3</td>
<td>HD40</td>
<td>I/O</td>
</tr>
<tr>
<td>A4</td>
<td>HD43</td>
<td>I/O</td>
</tr>
<tr>
<td>A5</td>
<td>HD46</td>
<td>I/O</td>
</tr>
<tr>
<td>A6</td>
<td>HD50</td>
<td>I/O</td>
</tr>
<tr>
<td>A7</td>
<td>HD54</td>
<td>I/O</td>
</tr>
<tr>
<td>A8</td>
<td>HD59</td>
<td>I/O</td>
</tr>
<tr>
<td>A9</td>
<td>WRJ</td>
<td>I</td>
</tr>
<tr>
<td>A10</td>
<td>NAJ</td>
<td>O</td>
</tr>
<tr>
<td>A11</td>
<td>ADSJ</td>
<td>I</td>
</tr>
<tr>
<td>A12</td>
<td>BEJ5</td>
<td>I</td>
</tr>
<tr>
<td>A13</td>
<td>BEJ0</td>
<td>I</td>
</tr>
<tr>
<td>A14</td>
<td>GWEJ</td>
<td>O</td>
</tr>
<tr>
<td>A15</td>
<td>CADVJ</td>
<td>O</td>
</tr>
<tr>
<td>A16</td>
<td>CADSJ</td>
<td>O</td>
</tr>
<tr>
<td>A17</td>
<td>TIO5</td>
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</tr>
<tr>
<td>A18</td>
<td>TIO8</td>
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</tr>
<tr>
<td>A19</td>
<td>TAGWEJ</td>
<td>O</td>
</tr>
<tr>
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<td>MD5</td>
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</tr>
<tr>
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<td>MD7</td>
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</tr>
<tr>
<td>A22</td>
<td>MD9</td>
<td>I/O</td>
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<tr>
<td>A23</td>
<td>MD11</td>
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<tr>
<td>A24</td>
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<td>I/O</td>
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<tr>
<td>A25</td>
<td>MD46</td>
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</tr>
<tr>
<td>A26</td>
<td>NC</td>
<td>-</td>
</tr>
<tr>
<td>B1</td>
<td>HD34</td>
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</tr>
<tr>
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<tr>
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<tr>
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<td>BEJ6</td>
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<tr>
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</tr>
<tr>
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<td>BWEJ</td>
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</tr>
<tr>
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<tr>
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</tr>
<tr>
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<tr>
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<tr>
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<tr>
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Section 3 : Function Description

3.1 System Architecture

In the following illustration, ALADDIN-V gives a highly integrated system solution and a most up-to-date system architecture, which includes the Accelerated Graphics Port, Parity/ECC, PBSRAM/Memory Cache, SDRAM, ACPI, Ultra-33 IDE Master, USB, PS2 Keyboard/Mouse, and highly concurrent multi-bus with smart deep FIFO between the buses, such as the HOST/ A.G.P./ DRAM/ PCI/ ISA/ DEDICATED IDE/USB buses. Using ALADDIN-V, you can achieve a TTL free solution and provide the best system performance.

As the North bridge, the M1541 provides a complete integrated solution for the system controller and data path components in a socket-7 processor system. It provides a 64-bit CPU bus interface, AGP bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Memory Cache, PCI master to DRAM interface, and 5 PCI masters, CPU, and M1533/M1543 arbiter. The following figure shows the highly efficient data path in the M1541. The M1541 bus interfaces are designed to interface with 2.5V, 3.3V and 5V buses. It directly connects to 3.3V or 2.5V CPU bus, 3.3V or 5V Tag, 3.3V or 5V DRAM bus, and 3.3V or 5V PCI bus.

Figure 3-1. Aladdin V System Block Diagram with M1533
The M1533 provides a highly integrated PCI-to-ISA bridge solution for the best Notebook system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, and Enhanced Green function.
The M1543 provides a highly integrated PCI-to-ISA bridge solution for the best Desktop system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, Green function, and the Super I/O function.

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**Figure 3-2. Aladdin V System Block Diagram with M1543**
3.2 Data Path and Buffer Architecture

Figure 3-3. Data Path and Buffer Architecture

1 : CPU to PCI – 6 DWORDs memory write buffer
2 : CPU to Memory – 32 QWORDs write buffer
3 : PCI to Memory – 80 DWORDs write posted buffer & 22 DWORDs read pre-fetch buffer
4 : CPU to AGP – 8 DWORDs posted write buffer
5 : PCI_66 to Memory – 40 QWORDs write buffer and 32 QWORDs read buffer
6 : PCI to AGP - 8 DWORDs write posted buffer
7 : PCI_66 to PCI - 2 DWORDs write posted buffer
8 : AGP to Memory – 16 QWORDs write buffer and 32 QWORDs read buffer

3.3 CPU Interface

The M1541 supports all Pentium-class CPUs including Intel P54C/P55C, Cyrix M1/M2, AMD K5/K6. Furthermore, M1541 supports a high performance CPU interface with bus frequency up to 100 MHz to achieve the Pentium II-class system performance. M1541 also supports Cyrix Linear Wrap mode for M1 and M2 to gain the best system performance. M1541 can also interface to 2.5V CPU I/O interface for Notebook use. In higher CPU bus frequency interface, M1541 will do the so-called pseudo-synchronous design instead of the asynchronous design. When 75/83.3/100 MHz CPU bus is used, the PCI bus will be running at 30/33/33 MHz (divide CPU bus by 2/2.5/3). The pseudo-synchronous clock design is a better solution than the pure
asynchronous clock design, it eliminates the performance degradation to synchronize two asynchronous buses and helps the chip reliability to resolve the chip testing issue.
3.4 Clock Design Philosophy

The system provides 4 clocks (HCLKIN, PCICLK, CLK32KI, GCLKIN) for M1541. HCLKIN has the same frequency with the CPUCLK, Cache clock, and SDRAM clock. PCICLK has the same frequency with the PCI bus clock, and CLK32KI is a 32.768KHz frequency clock from M1533/M1543 CLK32KO or from the system board clock source. GCLKIN provides the clock source of A.G.P. and PCI operation on A.G.P.

System designer should minimize the clock skew between CPUCLK, Cache clock, SDRAM clock, and HCLKIN, and also the skew between PCICLK and PCI bus clock. Regarding the skew between M1541 HCLKIN and PCICLK, PCICLK should lag HCLKIN for 1 ~ 4 ns. The internal clock design philosophy uses the HCLKIN running the state machine of CPU interface, L2 controller, and DRAM controller, and uses the PCICLK running the PCI state machine, and automatically takes good care of the internal signal interface between different clock frequency state machines. Also M1541 will support the internal smart clock control, it will shut off the internal clock when the CPU or PCI bus is idle to save the power consumption. CLK32KI clock is used for the DRAM Suspend refresh clock. It is a clock input and not necessarily relative to HCLKIN or PCICLK.

3.5 Cache Memory Timing/Configuration

The M1541 integrates a high performance L2 write back/dynamic-write-back direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag 16K2 bits built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for Memory Cache or Pipelined Burst SRAM with cache size ranging from 256KB, 512KB to 1MB. The cacheable region can be up to 1GB under 256KB L2 cache memory configuration, by using 8K10 tag RAM or two 8K8 tag RAM option. When using an 8K8 tag RAM under 256KB L2 cache, the cacheable region of the system is 256MB. The controller can perform a dynamic-write-back cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution. Also M1541 can support the CPU single read cycle L2 allocation feature, M1541 will do the L2 line fill even when the CPU issues only a single read cycle to improve the L2 hit rate for some special application. The following table shows the best performance for the L2 Read/Write access.
The timing of cache memory system is shown in following table:

Table 3-1

<table>
<thead>
<tr>
<th>PBSRAM and Memory cache</th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>

The following L2 Cache Table shows the different configurations supported by M1541.

Table 3-2

<table>
<thead>
<tr>
<th>Config Size</th>
<th>DATA SRAM</th>
<th>External TAG SRAM</th>
<th>Internal MESI 8K1×4</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cacheable</td>
<td>Ext. Tag Size</td>
<td>Cacheable DRAM Size</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Size Bank Address lines</td>
<td>Address lines</td>
<td>Data Lines</td>
<td>Size</td>
</tr>
<tr>
<td>256K</td>
<td>(32K32)*2 or (32K64)*4</td>
<td>1 A3-A17</td>
<td>A5-A17</td>
<td>A18-A25</td>
</tr>
<tr>
<td>512K</td>
<td>(64K32)*2 or (64K64)*4</td>
<td>1 A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
</tr>
<tr>
<td>512K</td>
<td>(32K64)*2 (32K32)*4</td>
<td>2 A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
</tr>
<tr>
<td>1M</td>
<td>(64K32)*4 or (64K64)*2</td>
<td>2 A3-A19</td>
<td>A5-A19</td>
<td>A20-A26</td>
</tr>
<tr>
<td>256K</td>
<td>(32K32)*2 or (32K64)*4</td>
<td>1 A3-A17</td>
<td>A5-A17</td>
<td>A18-A27</td>
</tr>
<tr>
<td>512K</td>
<td>(64K32)*2 or (64K64)*4</td>
<td>1 A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>512K</td>
<td>(32K64)*2 (32K32)*4</td>
<td>2 A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>1M</td>
<td>(64K32)*4 or (64K64)*2</td>
<td>2 A3-A19</td>
<td>A5-A19</td>
<td>A20-A28</td>
</tr>
</tbody>
</table>

The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.
Table 3-3.

<table>
<thead>
<tr>
<th>CPU Bus Frequency (MHz)</th>
<th>PBSRAM/Memory cache Clock-to-Output Access Time (ns)</th>
<th>Tag RAM Access Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>13.5</td>
<td>20</td>
</tr>
<tr>
<td>60</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>66</td>
<td>8.5</td>
<td>15</td>
</tr>
<tr>
<td>75</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>83</td>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>100</td>
<td>5</td>
<td>8</td>
</tr>
</tbody>
</table>
Table 3-4

The following table shows different L2 timings supported by M1541

<table>
<thead>
<tr>
<th>PBSRAM and Memory cache</th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>

In the following figures, two recommended cache subsystems are shown as follows:

Figure 3-4. Pipelined Burst SRAM L2 with single bank 256K & 8-bit Tag RAM (256M cacheable region, upgrade to 1G)
Figure 3-5. Pipelined Burst SRAM L2 with single bank 512K & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)
Figure 3-6. Pipelined Burst SRAM L2 with Double bank 1M & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)

3.6 Internal TAG SRAM

The M1541 integrates a high speed TAG SRAM the size is 16K10. With the built in TAG RAM at 83MHz hot bus frequency system, the timing will keep at 3-1-1-1 to meet the best performance. When using internal TAG RAM only, M1541 can not support 1M L2 size. When the system needs 1M L2, it must use external TAG mode.

The timing of cache memory system use internal TAG RAM at 83 or 100 MHz hot bus frequency is shown in following table:

<table>
<thead>
<tr>
<th>PBSRAM and Memory cache</th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>
The following L2 Cache Table shows the different configurations supported by M1541 by using the internal TAG RAM (Not every version of M1541 supports internal TAG solution, please add external TAG solution on your motherboard design)

Table 3-7.

<table>
<thead>
<tr>
<th>Config Cache Size</th>
<th>DATA SRAM</th>
<th>Internal TAG RAM</th>
<th>Internal MESI 8K1x4</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Size</td>
<td>Bank Address lines</td>
<td>Address lines Data Lines Int. Tag Size</td>
<td>Cacheable DRAM Size</td>
</tr>
<tr>
<td>256K (32K32)*2 or (32K64)*1</td>
<td>1</td>
<td>A3-A17</td>
<td>A5-A17</td>
<td>A18-A27</td>
</tr>
<tr>
<td>512K (64K32)*2 or (64K64)*1</td>
<td>1</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>512K (32K32)*4 or (32K64)*2</td>
<td>2</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>1M (64K32)*4 or (64K64)*2</td>
<td>2</td>
<td>A3-A19</td>
<td>A5-A19</td>
<td>A20-A27 Ext. TAG A28-A31 Int. TAG</td>
</tr>
</tbody>
</table>

3.7 SYSTEM MEMORY TIMING/CONFIGURATION

The DRAM controller of the M1541 supports a 64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs, and also supports the 64-bit memory bus for 8 banks of single-sided DIMMs or 4 banks of double sided DIMMs.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size ranging from 2MB to 4GB (with 256Mbits technology). It also supports a programmable driving capability of MA/CAS and MD/MPD to optimize the access timing and the system cost in certain system memory configurations. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip. M1541 supports a high performance SDRAM controller to push the new DRAM performance to the high edge. M1541 also enhances the DRAM page miss access timing for multithreading and multitasking application. For the best DRAM performance, M1541 has integrated a 32-QWORD deep merging DRAM write buffer. The deep buffer can post the CPU write data and also the PCI master write data and do byte merge to relief the DRAM bus access.
Although M1541 can support up to 8 banks of SDRAM (up to 4 DIMMs), the system is designed for 100 MHz CPU Front Side Bus frequency. Consider the loading of data bus, only three DIMM solution will be available at 100 MHz FSB design. M1541 achieves the best Performance/cost system solution.

As to the System Management RAM (SMRAM), the M1541 allows several optional non-cacheable spaces to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.
3.7.1 Memory Types Supported

Table 3-8. EDO/FP Memory Structure Supported

<table>
<thead>
<tr>
<th>Memory Structure</th>
<th>Address mode</th>
<th>Address size</th>
<th>Memory Structure</th>
<th>Address mode</th>
<th>Address size</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mbits</td>
<td></td>
<td></td>
<td>2Mx8</td>
<td>Asymmetric</td>
<td>11x10</td>
</tr>
<tr>
<td>512Kx8</td>
<td>Asymmetric</td>
<td>10x9</td>
<td>4Mx4</td>
<td>Symmetric</td>
<td>11x11</td>
</tr>
<tr>
<td>1Mx4</td>
<td>Symmetric</td>
<td>10x10</td>
<td>4Mx4</td>
<td>Asymmetric</td>
<td>12x10</td>
</tr>
<tr>
<td>16Mbits</td>
<td></td>
<td></td>
<td>64Mbits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Mx16</td>
<td>Asymmetric</td>
<td>11x9</td>
<td>4Mx16</td>
<td>Symmetric</td>
<td>11x11</td>
</tr>
<tr>
<td>1Mx16</td>
<td>Asymmetric</td>
<td>12x8</td>
<td>8Mx8</td>
<td>Asymmetric</td>
<td>12x11</td>
</tr>
<tr>
<td>1Mx16</td>
<td>Symmetric</td>
<td>10x10</td>
<td>16Mx4</td>
<td>Symmetric</td>
<td>12x12</td>
</tr>
<tr>
<td>2Mx8</td>
<td>Asymmetric</td>
<td>12x9</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.7.2 MA Mapping Table Supported

In the following table, ALADDIN-V supports a versatile memory MA mapping table to accommodate many different approaches of DRAM populated banks.

DRAM Address translation supported for some specific purpose

Table 3-9. Normal EDO/FP DRAM Address Translation

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Row      | -  | A16| A15| A24| A23| A14| A13| A12| A21| A20| A19| A18| A17| A16| A15|

Address Size = 10 x 9, 10 x 10, 11 x 10, 11 x 11, 12 x 10

Table 3-10. 1M x 16, 2M x 8 EDO/FP DRAM Address Translation

Specific DRAM Address Translation Table for Asymmetric 1M x 16

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Row      | -  | A16| A15| A11| A22| A14| A13| A12| A21| A20| A19| A18| A17| A16| A15|
| Column   | -  | A4 | A3 |    |    | A23| A10| A9 | A8 | A7 | A6 | A5 | A4 | A3 |    |

Address Size = 1Mx16(12 x 8), 2Mx8(12 x 9)

Table 3-11. 1Mx16, 64M bit EDO/FP DRAM Address Translation

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Row      | -  | A16| A15| A25| A22| A14| A13| A12| A21| A20| A19| A18| A17| A16| A15|

Address Size = 4Mx16(11 x 11), 8Mx8(12 x 11), 16Mx4(12 x 12)
Address Size = 1Mx16 (11x9)

Synchronous DRAM Address Translation Table:

Table 3-12. The connection from MA[14:0] to DIMMs

<table>
<thead>
<tr>
<th>M1541 signal</th>
<th>MA0</th>
<th>MA1</th>
<th>MA2</th>
<th>MA3</th>
<th>MA4</th>
<th>MA5</th>
<th>MA6</th>
<th>MA7</th>
<th>MA8</th>
<th>MA9</th>
<th>MA10</th>
<th>MA11</th>
<th>MA12</th>
<th>MA13</th>
<th>MA14</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIMM signal</td>
<td>A0</td>
<td>A1</td>
<td>A2</td>
<td>A3</td>
<td>A4</td>
<td>A5</td>
<td>A6</td>
<td>A7</td>
<td>A8</td>
<td>A9</td>
<td>A10/AP</td>
<td>NC(A11)</td>
<td>NC(A13),</td>
<td>BA0</td>
<td>NC(A12)</td>
</tr>
<tr>
<td>DIMM pin no.</td>
<td>33</td>
<td>117</td>
<td>34</td>
<td>118</td>
<td>35</td>
<td>119</td>
<td>36</td>
<td>120</td>
<td>37</td>
<td>121</td>
<td>38</td>
<td>123</td>
<td>132, 39</td>
<td>122</td>
<td>126</td>
</tr>
</tbody>
</table>
### SDRAM type to MA table 3-13

<table>
<thead>
<tr>
<th>DRAM type</th>
<th>Bank</th>
<th>Row address x Column address</th>
<th>MA Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>256Mb</td>
<td>4</td>
<td>13 x 9</td>
<td>3-15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 10</td>
<td>3-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 11</td>
<td>3-19</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>14 x 9</td>
<td>3-15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14 x 10</td>
<td>3-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14 x 11</td>
<td>3-19</td>
</tr>
<tr>
<td>128Mb</td>
<td>4</td>
<td>12 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 11</td>
<td>3-20</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>13 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 10</td>
<td>3-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 11</td>
<td>3-20</td>
</tr>
<tr>
<td>64Mb</td>
<td>4</td>
<td>11 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>13 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td>16Mb</td>
<td>2</td>
<td>11 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 10</td>
<td>3-18</td>
</tr>
</tbody>
</table>

### Table 3-14. Synchronous DRAM Address Translation:

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Row       | A23| A11| A23| A24| A22| A14| A13| A12| A21| A20| A19| A18| A17| A16| A15|

Address Size = 11 x 8, 12 x 8, 13 x 8,

### Table 3-15. Synchronous DRAM Address Translation:

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Row       | A23| A11| A23| A24| A22| A14| A13| A12| A21| A20| A19| A18| A17| A16| A15|
Address Size = 13 x 9, 14 x 9

Table 3-16. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column</td>
<td>-</td>
<td>A12</td>
<td>A24</td>
<td>-</td>
<td>AP</td>
<td>-</td>
<td>A11</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
</tr>
</tbody>
</table>

Address Size = 11 x 9, 12 x 9, 13 x 9,

Table 3-17. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

Address Size = 13 x 10, 14x10
Table 3-18. Synchronous DRAM Address Translation:

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

Address Size = 11 x 10, 12 x 10, 13 x 10

Table 3-19. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

Address Size = 13 x 11, 14 x 11

Table 3-20. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

Address Size = 12 x 11, 13 x 11

3.7.3 Outstanding DRAM timing

Table 3-21. CPU to DRAM read performance Summary for EDO/FPM DRAMs

<table>
<thead>
<tr>
<th>DRAM speed</th>
<th>DRAM type</th>
<th>50 MHz</th>
<th>60 MHz</th>
<th>66 MHz</th>
<th>75 MHz</th>
<th>83 MHz</th>
<th>100 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read (Burst rate)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50 ns</td>
<td>EDO</td>
<td>x-222</td>
<td>x-222</td>
<td>x-222</td>
<td>x-333</td>
<td>x-333</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FPM</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td></td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>x-222</td>
<td>x-222</td>
<td>x-222</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
</tr>
<tr>
<td></td>
<td>FPM</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td>x-444</td>
<td>x-444</td>
<td>x-444</td>
</tr>
<tr>
<td>70 ns</td>
<td>EDO</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
<td>x-333</td>
</tr>
<tr>
<td></td>
<td>FPM</td>
<td>x-333</td>
<td>x-444</td>
<td>x-444</td>
<td>x-444</td>
<td>x-444</td>
<td>x-444</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Page hit</th>
<th>50/60/66 MHz</th>
<th>75/83/100 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>5</td>
</tr>
<tr>
<td>Row Miss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>8</td>
</tr>
<tr>
<td>Page Miss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>11</td>
</tr>
<tr>
<td>Back-to-back Burst Reads with Page hit</td>
<td>50/60/66 MHz</td>
<td>75 MHz</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-------------</td>
<td>--------</td>
</tr>
<tr>
<td>60 ns EDO</td>
<td>5-222-2222</td>
<td>6-222-2222</td>
</tr>
<tr>
<td>60 ns FPM</td>
<td>5-333-3333</td>
<td>6-333-3333</td>
</tr>
</tbody>
</table>
### Table 3-22. CPU to DRAM Write Performance Summary

<table>
<thead>
<tr>
<th>DRAM speed</th>
<th>DRAM type</th>
<th>Performance (in Host CLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 MHz</td>
<td>60/66 MHz</td>
<td>75/83 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>3</td>
</tr>
</tbody>
</table>

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | EDO/FPM   | 3-111     | 3-111   | 3-111   | 3-111   |

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | EDO       | 3         | 3       | 3       | 4       |

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | FPM       | 3         | 4       | 4       | 5       |

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | EDO       | 5         | 5       | 5       | 6       |

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | FPM       | 5         | 6       | 6       | 7       |

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | EDO       | 8         | 8       | 8       | 8       |

| 50 MHz     | 60/66 MHz | 75/83 MHz | 100 MHz |
| 60 ns      | FPM       | 8         | 9       | 9       | 9       |

| 50/60 MHz  | 66 MHz    | 75/83 MHz | 100 MHz |
| 60 ns      | EDO       | x-222     | x-222   | x-333   | x-444   |

### Table 3-23. SDRAM Performance Summary

<table>
<thead>
<tr>
<th>Cycle Type</th>
<th>100/83/75 MHz</th>
<th>66/60/50 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAS Latency</td>
<td>CL=3</td>
<td>CL=2</td>
</tr>
<tr>
<td>Burst Read Page Hit</td>
<td>8-1-1-1</td>
<td>7-1-1-1</td>
</tr>
<tr>
<td>Read Bank Miss</td>
<td>11-1-1-1</td>
<td>9-1-1-1</td>
</tr>
<tr>
<td>Read Page Miss</td>
<td>14-1-1-1</td>
<td>11-1-1-1</td>
</tr>
<tr>
<td>Back-to-back Burst Read Page Hit</td>
<td>8-1-1-1-1</td>
<td>7-1-1-1-1</td>
</tr>
<tr>
<td>Write Page Hit</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Write Row Miss</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>Write Page Miss</td>
<td>10</td>
<td>8</td>
</tr>
</tbody>
</table>
### 3.7.4 EDO/FPM DRAM Configuration

ALADDIN-V supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. The following diagram shows some possible applications.
Figure 3-7. Two Double-Sided DRAM Banks (EDO/FPM)

M1541

RASJ[1:0]  RASJ[3:2]

32-bit SIMM  32-bit SIMM

MD[31:0]  MD[63:32]


Figure 3-8. Four Double-Sided DRAM Banks (EDO/FPM)

M1541


32-bit SIMM  32-bit SIMM  32-bit SIMM  32-bit SIMM

MD[31:0]  MD[63:32]


Buffer

3.7.5 SDRAM Support

Aladdin V supports the most popular synchronous DRAM (SDRAM) at technology of 16Mb, 64Mb, 128Mb, and 256Mb with extra performance and flexibility. Interleaved and linear wrap type for both CAS latency 2 and 3 with burst length 4 are supported. Users are permitted to use pure SDRAM up to 8 banks single sided or 4 banks of double sided, or mix with FPM/EDO DRAM on a row-by-row basis without any constraint. Furthermore, M1541 supports Enhanced Page mode which not only minimizes the effect of CAS latency (CL) and RAS Precharge time (Trp) but also largely enhances the overall performance of the system. JEDEC standard for SDRAM including 2n rule are supported too.

ALADDIN-V utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are:

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)
- Device Deselect (DESL)

The following Table shows the command truth table M1541 supports.

**Table 3-24. Command Truth Table**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode Register Set</td>
<td>MRS</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>V</td>
</tr>
<tr>
<td>Self-Refresh</td>
<td>SEFR</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Precharge All Banks</td>
<td>PALL</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>K</td>
<td>H</td>
<td>K</td>
</tr>
<tr>
<td>Precharge Selected</td>
<td>PRCH</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>K</td>
</tr>
<tr>
<td>Row Active</td>
<td>RACT</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>V</td>
<td>*3</td>
<td>V</td>
</tr>
<tr>
<td>Write</td>
<td>WRITE</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>V</td>
</tr>
<tr>
<td>Read</td>
<td>READ</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>V</td>
<td>L</td>
<td>V</td>
</tr>
<tr>
<td>No Operation</td>
<td>NOP</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>Device Deselect</td>
<td>DESL</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>CAS-before-RAS</td>
<td>CBR</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**

1. V = Valid, L = Logic Low, H = Logic High. K = Keep the value in previous cycle.

2. Please refer to Table 3-25.

In terms of Wrap Type of SDRAM, ALADDIN-V supports both Interleave mode and Linear (Sequential) mode. The following table shows the Mode Register Set Table supported by M1541.
ALADDIN-V supports one set of SDRAM control signals. Following figure show the topological configuration when supporting SDRAM. The following figure shows 8-bank support of SDRAM.

Figure 3-9. Four DIMMs Architecture
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MD[63:0]</td>
<td>MPD[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MWEJ0</td>
<td>SRASJ0</td>
<td>SCASJ0</td>
<td>64-bit DIMM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRASJ0</td>
<td>SCASJ0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCASJ1</td>
<td>SCSJ[3:2]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLKEN[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MWEJ1</td>
<td>SRASJ1</td>
<td>SCASJ1</td>
<td>64-bit DIMM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRASJ1</td>
<td>SCSJ[3:2]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCASJ2</td>
<td>SCSJ[5:4]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLKEN[3:2]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MWEJ2</td>
<td>SRASJ2</td>
<td>SCASJ2</td>
<td>64-bit DIMM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRASJ2</td>
<td>SCSJ[5:4]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCASJ3</td>
<td>SCSJ[7:6]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLKEN[5:4]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MWEJ3</td>
<td>SRASJ3</td>
<td>SCASJ3</td>
<td>64-bit DIMM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRASJ3</td>
<td>SCSJ[7:6]</td>
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<td></td>
<td></td>
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<tr>
<td>SCASJ4</td>
<td>SCSJ[9:8]</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>CLKEN[7:6]</td>
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<td></td>
</tr>
<tr>
<td>MD[63:0]</td>
<td>MPD[7:0]</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3.7.6 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-V is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING. If only 4 banks of single sided DRAM SIMMs or 2 banks of double sided DRAM SIMMs or 8 banks of single sided DRAM DIMMs or 4 banks of double sided DRAM DIMMs are designed in motherboard, M1541 is designed to be TTL free for the DRAM control signals buffer.

3.8 CPU-to-PCI Posted Write Buffer

The M1541 integrates a 6-DWORD CPU-to-PCI posted write buffer to enhance the CPU-to-PCI performance. With this buffer, the M1541 can minimize the latency of CPU-to-PCI write cycles and maximize the concurrency of CPU bus and PCI bus when CPU writes data to PCI bus. The PCI burst write cycles and fast back-to-back cycles for CPU-to-PCI access are also supported by this buffer.

In addition, the M1541 CPU-to-PCI posted write buffer supports data merge, it can improve the CPU-to-PCI non-32 bits access performance.

3.9 PCI MASTER Latency and Throughput Analysis

The M1541 includes a smart PCI-to-DRAM interface, including a smart deep PCI-to-DRAM buffer and the enhanced PCI arbiter. All these components are designed to optimize the system performance and maximize the PCI bus bandwidth.

3.9.1 Smart Deep Post Write & Pre-fetch Buffer

The smart deep PCI-to-DRAM buffer of M1541 plays the key role to boost PCI master read/write performance. It consists of 80 DWORDs posted write buffer and 22 DWORDs pre-fetch buffer.

The 80 DWORDs PCI-to-DRAM posted write buffers enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 write back merge and smart buffer management, the M1541 can sustain the ultimate 133-Mbytes/sec bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and write back cycle, the DRAM types and L2 types.

On the other hand, to optimize the PCI master read performance when accessing DRAM, the M1541 includes 22 DWORDs PCI-to-DRAM read pre-fetch buffers. With the implementation of L1/L2 write back and smart buffer management, the M1541 can sustain the ultimate 133 Mbytes/sec bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, write back cycle and L2 types.
Considering the performance and concurrency of multi-master systems, for example the MPEG/Multimedia applications, the PCI-to-DRAM read pre-fetch buffer of M1541 is configured as two independent units. Each unit pre-fetches and keeps data independently with the other one. With this configuration, the M1541 minimizes the PCI master read latency and reduces the overhead of snooping and pre-fetching.

3.9.2 PCI 2.1 Compliant

The M1541 is fully compliant to the PCI 2.1 Specification. The M1541 supports Passive Release and programmable latency control timers for the first and subsequent data transaction. With the flexible PCI latency control, it can achieve the best system performance.

3.9.3 Pipelined Snoop Ahead

The M1541 utilizes an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. While snooping L1 & L2, the M1541 also performs speculative read to DRAM such that the latency of master read cycle can be minimized. It combines with the deep smart read/write buffer to optimize PCI master performance.
3.9.4 PCI Arbiter

The M1541 integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism. The arbitration algorithm is also designed to minimize the snoop overhead. Besides the M1533/M1543 ISA bridge and AGP master, the M1541 supports up to 5 PCI masters to make the system motherboard design more flexible and engaging.

To balance the bandwidth of ISA masters and PCI masters and utilize the most bandwidth of PCI bus, the M1541 also supports passive release of PCI 2.1 latency requirements, which makes PCI master access possible when ISA master is active. By this way, the ALADDIN-V can target the best system performance and the most concurrency between PCI bus and ISA bus.

3.9.5 ACPI Support

The M1541 provides the scheme to support ACPI relative functions. By means of PM2_BASE_ADDRESS register (Index-E8h - Index-E9h ) and PM2_CONTROL register (Index-EAh bits[1:0]), software can easily enable/disable PCI arbiter as ACPI requirement. In addition, PCIMRQJ signal makes ISA Bridge aware of PCI master bus request to generate SMI/SCI.

3.10 Low Power Features

The ALADDIN-V supports sophisticated power saving features, called Power On Suspend (Sleeping), Suspend to DRAM (Suspend), and Suspend to Disk. Under Power On Suspend state, the system will turn off the signal event of host and keep the DRAM refresh active through the M1541 DRAM interface that is triggered by a 32.768KHz clock source. After the Power On suspend event is triggered, by programming a bit of M1533/M1543 internal register, the M1533/M1543 will initiate a handshake with the M1541. During the handshake, the M1533/M1543 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH circuit to sustain the DRAM data. Theoretically, the only power request under the Power On suspend is the circuit of DRAM suspend refresh. M1541 core has two different power planes, one for the Suspend Refresh circuit, the other is for the other circuit except Suspend Refresh circuit. During Suspend to DRAM state, the system designer can shut off the power except the DRAM suspend refresh circuit to save more system power. Under the Suspend to Disk, only the M1533/M1543 resume circuit is powered and get the minimized system power consumption.

The M1541 and the M1533/M1543 are designed with a very sophisticated I/O circuit and to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the Power On suspend can provide the system a very efficient STAND-ON feature that is more demanding in future home PC systems for Microsoft On Now technology OS.

In the M1533/M1543 of ALADDIN-V, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one
might design a dedicated PMU device to accompany the Power On suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-V provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

3.11 DRAM Refresh

The M1541 provides CAS-before-RAS (CBR) refresh and RAS-only refresh for FPM DRAM, CAS-before-RAS (CBR) refresh and RAS-only refresh and Extended refresh and self refresh for EDO DRAM, and CAS-before-RAS (CBR) refresh and Self refresh for SDRAMs. FPM/EDO refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h Bits[2:0].
3.12 ECC/Parity Algorithm

The M1541 provides an ECC DRAM data integrity feature. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. The M1541 will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1541. The M1541 will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read cycle is performed. The M1541 also corrects all single-bit errors and the corrected data is then transferred to the requester (CPU or PCI). This corrected data will not be written back to DRAM in the current M1541 version. The ECC errors are latched until cleared by software. The software programmer also can detect 64 from 72-bit wide SIMMs or check ECC circuit operations via the ECC (parity) test mode. The ECC check bits (or parities) can be forced to any value during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLKIN when the ECC feature is enabled.

The M1541 also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 50h bit0 is set to '0'. The DRAM parity checking error reporting condition and status also are defined in Index 50h-51h. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode. The conventional Parity check will not degrade the system performance.

3.13 AGP and PCI-to-PCI bridge

The M1541 has a built in PCI-to-PCI bridge device to support the AGP interface. The Device ID is M5247. Behind the PCI to PCI bridge is an 66MHz PCI bus which meets the PCI revision 2.1 specification to support the AGP interface. The interface provides three significant performance extensions to the PCI specification which are intended to optimize the AGP for high performance 3D graphics applications. These extensions are:

1. Deep pipeline memory read buffer (32 QWORDs) and memory write buffer (16 QWORDs), fully hiding memory access latency

2. Demultiplexing of address and data on the bus use the “IDLE band” signals, allowing almost 100% bus efficiency

3. AC timing for 133 MHz data transfer rate, up to 533 Mbytes/sec data throughput

The M1541 supports a physically, logically and electrically independent AGP interface. Support both the PIPEJ and SBA[7-0] addressing method and RBFJ flow control. The design is following the AGP revision 1.0 specification. The interface will support the PCI 66 mode, AGP 1X mode and 2X modes.

When at PCI 66 mode, the FRAMEJ protocol will be followed.
When at 1X transfer mode, the operation is similar to the PCI. All timings are referenced to the AGP clock. It will provide a peak bandwidth of 266Mbyte/sec.

When at 2X transfer mode, the data transfer rate of the AD, C/BEJ and SBA signals are double. With 2X transfer, QWORD transfers only require one clock cycle, and sideband commands only require one clock per 16-bit command.

For maximum software compatibility, two-level GART (Graphics Address Re-mapping Table) is set up and maintained by mini-port driver supported by ALI. So the actual table implementation is abstracted to a common API.

Besides, the 8 DWORDs PCI to PCI_66 posted write buffer and the 2 DWORDs PCI_66 to PCI posted write buffer make M1541 perform outstanding multi-master system performance. Especially when AGP 3D engine on AGP bus and video processor like MPEG2 accelerator on 33 MHz PCI bus.
Section 3 : Function Description

3.1 System Architecture

In the following illustration, ALADDIN-V gives a highly integrated system solution and a most up-to-date system architecture, which includes the Accelerated Graphics Port, Parity/ECC, PBSRAM/Memory Cache, SDRAM, ACPI, Ultra-33 IDE Master, USB, PS2 Keyboard/Mouse, and highly concurrent multi-bus with smart deep FIFO between the buses, such as the HOST/ A.G.P./ DRAM/ PCI/ ISA/ DEDICATED IDE/USB buses. Using ALADDIN-V, you can achieve a TTL free solution and provide the best system performance.

![Figure 3-1. Aladdin V System Block Diagram with M1533](image)

As the North bridge, the M1541 provides a complete integrated solution for the system controller and data path components in a socket-7 processor system. It provides a 64-bit CPU bus interface, AGP bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Memory Cache, PCI master to DRAM interface, and 5 PCI masters, CPU, and M1533/M1543 arbiter. The following figure shows the highly efficient data path in the M1541. The M1541 bus interfaces are designed to interface with 2.5V, 3.3V and 5V buses. It directly connects to 3.3V or 2.5V CPU bus, 3.3V or 5V Tag, 3.3V or 5V DRAM bus, and 3.3V or 5V PCI bus.
The M1533 provides a highly integrated PCI-to-ISA bridge solution for the best Notebook system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, and Enhanced Green function.
The M1543 provides a highly integrated PCI-to-ISA bridge solution for the best Desktop system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, Green function, and the Super I/O function.

Figure 3-2. Aladdin V System Block Diagram with M1543
3.2 Data Path and Buffer Architecture

![Diagram of Data Path and Buffer Architecture]

**Figure 3-3. Data Path and Buffer Architecture**

1 : CPU to PCI – 6 DWORDs memory write buffer
2 : CPU to Memory – 32 QWORDs write buffer
3 : PCI to Memory – 80 DWORDs write posted buffer & 22 DWORDs read pre-fetch buffer
4 : CPU to AGP – 8 DWORDs posted write buffer
5 : PCI_66 to Memory – 40 QWORDs write buffer and 32 QWORDs read buffer
6 : PCI to AGP - 8 DWORDs write posted buffer
7 : PCI_66 to PCI - 2 DWORDs write posted buffer
8 : AGP to Memory – 16 QWORDs write buffer and 32 QWORDs read buffer

3.3 CPU Interface

The M1541 supports all Pentium-class CPUs including Intel P54C/P55C, Cyrix M1/M2, AMD K5/K6. Furthermore, M1541 supports a high performance CPU interface with bus frequency up to 100 MHz to achieve the Pentium II-class system performance. M1541 also supports Cyrix Linear Wrap mode for M1 and M2 to gain the best system performance. M1541 can also interface to 2.5V CPU I/O interface for Notebook use. In higher CPU bus frequency interface, M1541 will do the so-called pseudo-synchronous design instead of the asynchronous design. When 75/83.3/100 MHz CPU bus is used, the PCI bus will be running at 30/33/33 MHz (divide CPU bus by 2/2.5/3). The pseudo-synchronous clock design is a better solution than the pure
asynchronous clock design, it eliminates the performance degradation to synchronize two asynchronous buses and helps the chip reliability to resolve the chip testing issue.
3.4 Clock Design Philosophy

The system provides 4 clocks (HCLKIN, PCICLK, CLK32KI, GCLKIN) for M1541. HCLKIN has the same frequency with the CPUCLK, Cache clock, and SDRAM clock. PCICLK has the same frequency with the PCI bus clock, and CLK32KI is a 32.768KHz frequency clock from M1533/M1543 CLK32KO or from the system board clock source. GCLKIN provides the clock source of A.G.P. and PCI operation on A.G.P.

System designer should minimize the clock skew between CPUCLK, Cache clock, SDRAM clock, and HCLKIN, and also the skew between PCICLK and PCI bus clock. Regarding the skew between M1541 HCLKIN and PCICLK, PCICLK should lag HCLKIN for 1 ~ 4 ns. The internal clock design philosophy uses the HCLKIN running the state machine of CPU interface, L2 controller, and DRAM controller, and uses the PCICLK running the PCI state machine, and automatically takes good care of the internal signal interface between different clock frequency state machines. Also M1541 will support the internal smart clock control, it will shut off the internal clock when the CPU or PCI bus is idle to save the power consumption. CLK32KI clock is used for the DRAM Suspend refresh clock. It is a clock input and not necessarily relative to HCLKIN or PCICLK.

3.5 Cache Memory Timing/Configuration

The M1541 integrates a high performance L2 write back/dynamic-write-back direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag 16K2 bits built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for Memory Cache or Pipelined Burst SRAM with cache size ranging from 256KB, 512KB to 1MB. The cacheable region can be up to 1GB under 256KB L2 cache memory configuration, by using 8K10 tag RAM or two 8K8 tag RAM option. When using an 8K8 tag RAM under 256KB L2 cache , the cacheable region of the system is 256MB. The controller can perform a dynamic-write-back cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution. Also M1541 can support the CPU single read cycle L2 allocation feature, M1541 will do the L2 line fill even when the CPU issues only a single read cycle to improve the L2 hit rate for some special application. The following table shows the best performance for the L2 Read/Write access.
The timing of cache memory system is shown in following table:

Table 3-1

<table>
<thead>
<tr>
<th>PBSRAM and Memory cache</th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>

The following L2 Cache Table shows the different configurations supported by M1541.

Table 3-2

<table>
<thead>
<tr>
<th>Config</th>
<th>DATA SRAM</th>
<th>External TAG SRAM</th>
<th>Internal MESA 8K1x4</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache Size</td>
<td>Bank</td>
<td>Address lines</td>
<td>Address lines</td>
<td>Data Lines</td>
</tr>
<tr>
<td>256K (32K32)*2</td>
<td>1</td>
<td>A3-A17</td>
<td>A5-A17</td>
<td>A18-A25</td>
</tr>
<tr>
<td>or (32K64)*1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512K (64K32)*2</td>
<td>1</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
</tr>
<tr>
<td>or (64K64)*1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512K (32K64)*2</td>
<td>2</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
</tr>
<tr>
<td>or (32K32)*4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1M (64K32)*4</td>
<td>2</td>
<td>A3-A19</td>
<td>A5-A19</td>
<td>A20-A26</td>
</tr>
<tr>
<td>or (64K64)*2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256K (32K32)*2</td>
<td>1</td>
<td>A3-A17</td>
<td>A5-A17</td>
<td>A18-A27</td>
</tr>
<tr>
<td>or (32K64)*1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512K (64K32)*2</td>
<td>1</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>or (64K64)*1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512K (32K64)*2</td>
<td>2</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>or (32K32)*4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1M (64K32)*4</td>
<td>2</td>
<td>A3-A19</td>
<td>A5-A19</td>
<td>A20-A28</td>
</tr>
<tr>
<td>or (64K64)*2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.

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1541DS10.doc
Acer Laboratories, Inc., USA, 1830B Bering Drive, San Jose, CA 95112; Tel: 408-467-7456; Fax: 408-467-7474
www.acerlabs.com
<table>
<thead>
<tr>
<th>CPU Bus Frequency (MHz)</th>
<th>PBSRAM/Memory cache Clock-to-Output Access Time (ns)</th>
<th>Tag RAM Access Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>13.5</td>
<td>20</td>
</tr>
<tr>
<td>60</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>66</td>
<td>8.5</td>
<td>15</td>
</tr>
<tr>
<td>75</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>83</td>
<td>6</td>
<td>9</td>
</tr>
<tr>
<td>100</td>
<td>5</td>
<td>8</td>
</tr>
</tbody>
</table>
Table 3-4

The following table shows different L2 timings supported by M1541

<table>
<thead>
<tr>
<th></th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBSRAM and Memory cache</td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>

In the following figures, two recommended cache subsystems are shown as follows:

**Figure 3-4. Pipelined Burst SRAM L2 with single bank 256K & 8-bit Tag RAM (256M cacheable region, upgrade to 1G)**
Figure 3-5. Pipelined Burst SRAM L2 with single bank 512K & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)
3.6 Internal TAG SRAM

The M1541 integrates a high speed TAG SRAM the size is 16K10. With the built in TAG RAM at 83MHz hot bus frequency system, the timing will keep at 3-1-1-1 to meet the best performance. When using internal TAG RAM only, M1541 can not support 1M L2 size. When the system needs 1M L2, it must use external TAG mode.

The timing of cache memory system use internal TAG RAM at 83 or 100 MHz hot bus frequency is shown in following table:

Table 3-6.

<table>
<thead>
<tr>
<th></th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBSRAM and Memory cache</td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>
The following L2 Cache Table shows the different configurations supported by M1541 by using the internal TAG RAM (Not every version of M1541 supports internal TAG solution, please add external TAG solution on your motherboard design)

**Table 3-7.**

<table>
<thead>
<tr>
<th>Config</th>
<th>DATA SRAM</th>
<th>Internal TAG SRAM</th>
<th>Internal MESI 8K1x4</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Size</td>
<td>Bank</td>
<td>Address lines</td>
<td>Address lines</td>
</tr>
<tr>
<td>Cache Size</td>
<td>256K</td>
<td>(32K32)*2 or (32K64)*1</td>
<td>1</td>
<td>A3-A17</td>
</tr>
<tr>
<td></td>
<td>512K</td>
<td>(64K32)*2 or (64K64)*1</td>
<td>1</td>
<td>A3-A18</td>
</tr>
<tr>
<td></td>
<td>512K</td>
<td>(32K32)*4 or (32K64)*2</td>
<td>2</td>
<td>A3-A18</td>
</tr>
<tr>
<td></td>
<td>1M</td>
<td>64K32)*4 or (64K64)*2</td>
<td>2</td>
<td>A3-A19</td>
</tr>
</tbody>
</table>

**3.7 SYSTEM MEMORY TIMING/CONFIGURATION**

The DRAM controller of the M1541 supports a 64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs, and also supports the 64-bit memory bus for 8 banks of single-sided DIMMs or 4 banks of double sided DIMMs.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size ranging from 2MB to 4GB (with 256Mbits technology). It also supports a programmable driving capability of MA/CAS and MD/MPD to optimize the access timing and the system cost in certain system memory configurations. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip. M1541 supports a high performance SDRAM controller to push the new DRAM performance to the high edge. M1541 also enhances the DRAM page miss access timing for multithreading and multitasking application. For the best DRAM performance, M1541 has integrated a 32-QWORD deep merging DRAM write buffer. The deep buffer can post the CPU write data and also the PCI master write data and do byte merge to relief the DRAM bus access.
Although M1541 can support up to 8 banks of SDRAM (up to 4 DIMMs), the system is designed for 100 MHz CPU Front Side Bus frequency. Consider the loading of data bus, only three DIMM solution will be available at 100 MHz FSB design. M1541 achieves the best Performance/cost system solution.

As to the System Management RAM (SMRAM), the M1541 allows several optional non-cacheable spaces to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.
3.7.1 Memory Types Supported

Table 3-8. EDO/FP Memory Structure Supported

<table>
<thead>
<tr>
<th>Memory Structure</th>
<th>Address mode</th>
<th>Address size</th>
<th>Memory Structure</th>
<th>Address mode</th>
<th>Address size</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mbits</td>
<td></td>
<td></td>
<td>2Mx8</td>
<td>Asymmetric</td>
<td>11x10</td>
</tr>
<tr>
<td>512Kx8</td>
<td>Asymmetric</td>
<td>10x9</td>
<td>4Mx4</td>
<td>Symmetric</td>
<td>11x11</td>
</tr>
<tr>
<td>1Mx4</td>
<td>Symmetric</td>
<td>10x10</td>
<td>4Mx4</td>
<td>Asymmetric</td>
<td>12x10</td>
</tr>
<tr>
<td>16Mbits</td>
<td></td>
<td></td>
<td>64Mbits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Mx16</td>
<td>Asymmetric</td>
<td>11x9</td>
<td>4Mx16</td>
<td>Symmetric</td>
<td>11x11</td>
</tr>
<tr>
<td>1Mx16</td>
<td>Asymmetric</td>
<td>12x8</td>
<td>8Mx8</td>
<td>Asymmetric</td>
<td>12x11</td>
</tr>
<tr>
<td>1Mx16</td>
<td>Symmetric</td>
<td>10x10</td>
<td>16Mx4</td>
<td>Symmetric</td>
<td>12x12</td>
</tr>
<tr>
<td>2Mx8</td>
<td>Asymmetric</td>
<td>12x9</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.7.2 MA Mapping Table Supported

In the following table, ALADDIN-V supports a versatile memory MA mapping table to accommodate many different approaches of DRAM populated banks.

DRAM Address translation supported for some specific purpose

Table 3-9. Normal EDO/FP DRAM Address Translation

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>-</td>
<td>A16</td>
<td>A15</td>
<td>A24</td>
<td>A23</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
</tr>
</tbody>
</table>

Address Size = 10 x 9, 10 x 10, 11 x 10, 11 x 11, 12 x 10

Table 3-10. 1M x 16, 2M x 8 EDO/FP DRAM Address Translation

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>-</td>
<td>A16</td>
<td>A15</td>
<td>A11</td>
<td>A22</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
</tr>
<tr>
<td>Column</td>
<td>-</td>
<td>A4</td>
<td>A3</td>
<td></td>
<td></td>
<td>A23</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td></td>
</tr>
</tbody>
</table>

Address Size = 1Mx16(12 x 8), 2Mx8(12 x 9)

Table 3-11. 1Mx16, 64M bit EDO/FP DRAM Address Translation

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>-</td>
<td>A16</td>
<td>A15</td>
<td>A25</td>
<td>A22</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
</tr>
</tbody>
</table>

Address Size = 4Mx16(11 x 11), 8Mx8(12 x 11), 16Mx4(12 x 12)
Synchronous DRAM Address Translation Table:

<table>
<thead>
<tr>
<th>M1541 signal</th>
<th>MA0</th>
<th>MA1</th>
<th>MA2</th>
<th>MA3</th>
<th>MA4</th>
<th>MA5</th>
<th>MA6</th>
<th>MA7</th>
<th>MA8</th>
<th>MA9</th>
<th>MA10</th>
<th>MA11</th>
<th>MA12</th>
<th>MA13</th>
<th>MA14</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIMM signal</td>
<td>A0</td>
<td>A1</td>
<td>A2</td>
<td>A3</td>
<td>A4</td>
<td>A5</td>
<td>A6</td>
<td>A7</td>
<td>A8</td>
<td>A9</td>
<td>A10/AP</td>
<td>NC(A11)</td>
<td>NC(A13),</td>
<td>BA0</td>
<td>NC(A12)</td>
</tr>
<tr>
<td>DIMM pin no.</td>
<td>33</td>
<td>117</td>
<td>34</td>
<td>118</td>
<td>35</td>
<td>119</td>
<td>36</td>
<td>120</td>
<td>37</td>
<td>121</td>
<td>38</td>
<td>123</td>
<td>132, 39</td>
<td>122</td>
<td>126</td>
</tr>
</tbody>
</table>
### SDRAM type to MA table 3-13

<table>
<thead>
<tr>
<th>DRAM type</th>
<th>Bank</th>
<th>Row address x Column address</th>
<th>MA Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>256Mb</td>
<td>4</td>
<td>13 x 9</td>
<td>3-15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 10</td>
<td>3-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 11</td>
<td>3-19</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>14 x 9</td>
<td>3-15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14 x 10</td>
<td>3-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14 x 11</td>
<td>3-19</td>
</tr>
<tr>
<td>128Mb</td>
<td>4</td>
<td>12 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 11</td>
<td>3-20</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>13 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 10</td>
<td>3-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 11</td>
<td>3-20</td>
</tr>
<tr>
<td>64Mb</td>
<td>4</td>
<td>11 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>13 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13 x 10</td>
<td>3-18</td>
</tr>
<tr>
<td>16Mb</td>
<td>2</td>
<td>11 x 8</td>
<td>3-14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 9</td>
<td>3-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 x 10</td>
<td>3-18</td>
</tr>
</tbody>
</table>

### Table 3-14. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A23</td>
<td>A11</td>
<td>A23</td>
<td>A24</td>
<td>A22</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
</tr>
</tbody>
</table>

Address Size = 11 x 8, 12 x 8, 13 x 8,

### Table 3-15. Synchronous DRAM Address Translation:

| MA[14:0] | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
|           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
### Table 3-16. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column</td>
<td>-</td>
<td>A12</td>
<td>A24</td>
<td>-</td>
<td>AP</td>
<td>-</td>
<td>A11</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
</tr>
</tbody>
</table>

Address Size = 13 x 9, 14 x 9

### Table 3-17. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

Address Size = 13 x 10, 14 x 10
### Table 3-18. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A25</td>
<td>A13</td>
<td>A26</td>
<td>A22</td>
<td>A14</td>
<td>A24</td>
<td>A23</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td></td>
</tr>
</tbody>
</table>

Address Size = 11 x 10, 12 x 10, 13 x 10

### Table 3-19. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

Address Size = 13 x 11, 14 x 11

### Table 3-20. Synchronous DRAM Address Translation:

<table>
<thead>
<tr>
<th>MA[14:0]</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

Address Size = 12 x 11, 13 x 11

3.7.3 Outstanding DRAM timing

### Table 3-21. CPU to DRAM read performance Summary for EDO/FPM DRAMs

<table>
<thead>
<tr>
<th>DRAM speed Read (Burst rate)</th>
<th>DRAM type</th>
<th>Performance (in Host CLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>50 MHz</td>
</tr>
<tr>
<td>50 ns EDO</td>
<td>x-222</td>
<td>x-222</td>
</tr>
<tr>
<td>50 ns FPM</td>
<td>x-333</td>
<td>x-333</td>
</tr>
<tr>
<td>60 ns EDO</td>
<td>x-222</td>
<td>x-222</td>
</tr>
<tr>
<td>60 ns FPM</td>
<td>x-333</td>
<td>x-333</td>
</tr>
<tr>
<td>70 ns EDO</td>
<td>x-333</td>
<td>x-333</td>
</tr>
<tr>
<td>70 ns FPM</td>
<td>x-333</td>
<td>x-444</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Page hit</th>
<th>50/60/66 MHz</th>
<th>75/83/100 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 ns EDO</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>60 ns FPM</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Row Miss</th>
<th>60 ns EDO/FPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Page Miss</th>
<th>60 ns EDO/FPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>11</td>
</tr>
</tbody>
</table>
### Back-to-back Burst Reads

<table>
<thead>
<tr>
<th></th>
<th>50/60/66 MHz</th>
<th>75 MHz</th>
<th>83/100 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 ns EDO</td>
<td>5-222-2222</td>
<td>6-222-2222</td>
<td>6-333-3333</td>
</tr>
<tr>
<td>60 ns FPM</td>
<td>5-333-3333</td>
<td>6-333-3333</td>
<td>6-444-4444</td>
</tr>
</tbody>
</table>
### Table 3-22. CPU to DRAM Write Performance Summary

<table>
<thead>
<tr>
<th>DRAM speed</th>
<th>DRAM type</th>
<th>Performance (in Host CLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Posted Single Write with Write Buffer Empty</td>
<td>50 MHz</td>
<td>60/66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>3</td>
</tr>
<tr>
<td>Posted Burst Write with Write Buffer Empty</td>
<td>50 MHz</td>
<td>60/66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>3-111</td>
</tr>
<tr>
<td>Single Retire Hit</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>60 ns</td>
<td>FPM</td>
</tr>
<tr>
<td>Single Retire Row Miss with RAS-CAS = 2T</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>60 ns</td>
<td>FPM</td>
</tr>
<tr>
<td>Single Retire Page Miss with RAS-CAS = 2T</td>
<td>50/60 MHz</td>
<td>60/66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>60 ns</td>
<td>FPM</td>
</tr>
<tr>
<td>Retire Burst</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>x-222</td>
</tr>
<tr>
<td></td>
<td>60 ns</td>
<td>FPM</td>
</tr>
</tbody>
</table>

### Table 3-23. SDRAM Performance Summary

<table>
<thead>
<tr>
<th>Cycle Type</th>
<th>100/83/75 MHz</th>
<th>66/60/50 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAS Latency</td>
<td>CL=3</td>
<td>CL=2</td>
</tr>
<tr>
<td>Burst Read Page Hit</td>
<td>8-1-1-1</td>
<td>7-1-1-1</td>
</tr>
<tr>
<td>Read Bank Miss</td>
<td>11-1-1-1</td>
<td>9-1-1-1</td>
</tr>
<tr>
<td>Read Page Miss</td>
<td>14-1-1-1</td>
<td>11-1-1-1</td>
</tr>
<tr>
<td>Back-to-back Burst Read Page Hit</td>
<td>8-1-1-1-1-1-1</td>
<td>7-1-1-1-1-1-1</td>
</tr>
<tr>
<td>Write Page Hit</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Write Row Miss</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>Write Page Miss</td>
<td>10</td>
<td>8</td>
</tr>
</tbody>
</table>
### 3.7.4 EDO/FPM DRAM Configuration

ALADDIN-V supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. The following diagram shows some possible applications.
Figure 3-7. Two Double-Sided DRAM Banks (EDO/FPM)

Figure 3-8. Four Double-Sided DRAM Banks (EDO/FPM)
3.7.5 SDRAM Support

Aladdin V supports the most popular synchronous DRAM (SDRAM) at technology of 16Mb, 64Mb, 128Mb, and 256Mb with extra performance and flexibility. Interleaved and linear wrap type for both CAS latency 2 and 3 with burst length 4 are supported. Users are permitted to use pure SDRAM up to 8 banks single sided or 4 banks of double sided, or mix with FPM/EDO DRAM on a row-by-row basis without any constraint. Furthermore, M1541 supports Enhanced Page mode which not only minimizes the effect of CAS latency (CL) and RAS Precharge time (Trp) but also largely enhances the overall performance of the system. JEDEC standard for SDRAM including 2n rule are supported too.

ALADDIN-V utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are:

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)
- Device Deselected (DESL)

The following Table shows the command truth table M1541 supports.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode Register Set</td>
<td>MRS</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>V</td>
<td>*2</td>
</tr>
<tr>
<td>Self-Refresh</td>
<td>SEFR</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Precharge All Banks</td>
<td>PALL</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>K</td>
<td>H</td>
<td>K</td>
</tr>
<tr>
<td>Precharge Selected</td>
<td>PRCH</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>K</td>
</tr>
<tr>
<td>Bank</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Row Active</td>
<td>RACT</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>Write</td>
<td>WRITE</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>L</td>
<td>V</td>
</tr>
<tr>
<td>Read</td>
<td>READ</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>V</td>
<td>L</td>
<td>V</td>
</tr>
<tr>
<td>No Operation</td>
<td>NOP</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>Device Deselect</td>
<td>DESL</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>CAS-Before-RAS</td>
<td>CBR</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
</tbody>
</table>

Notes:

1. V = Valid, L = Logic Low, H = Logic High. K = Keep the value in previous cycle.
2. Please refer to Table 3-25.

In terms of Wrap Type of SDRAM, ALADDIN-V supports both Interleave mode and Linear (Sequential) mode. The following table shows the Mode Register Set Table supported by M1541.
Table 3-25. Mode Register Set

<table>
<thead>
<tr>
<th>A11</th>
<th>A10</th>
<th>A9</th>
<th>A8</th>
<th>A7</th>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CAS Latency</td>
<td>Burst Type</td>
<td>Burst Length</td>
<td>Mode Register</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>CAS Latency</th>
<th>Index-48h bit4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

A3 Burst Type Description

<table>
<thead>
<tr>
<th>A3</th>
<th>Burst Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Sequential</td>
<td>for M1/M2 Linear Wrap Mode</td>
</tr>
<tr>
<td>1</td>
<td>Interleave</td>
<td>for P54C/P55C/K5/K6 Interleave mode</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>Burst Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

Others Not Support

ALADDIN-V supports one set of SDRAM control signals. Following figure show the topological configuration when supporting SDRAM. The following figure shows 8-bank support of SDRAM.

Figure 3-9. Four DIMMs Architecture
M1541

<table>
<thead>
<tr>
<th></th>
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<th></th>
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<th></th>
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<tbody>
<tr>
<td>MWEJ0</td>
<td>SRASJ0</td>
<td>SCASJ0</td>
<td>SCSJ[1:0]</td>
<td>MD[63:0]</td>
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<td></td>
</tr>
<tr>
<td>CLKEN[1:0]</td>
<td></td>
<td></td>
<td></td>
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<td>MWEJ1</td>
<td>SRASJ1</td>
<td>SCASJ1</td>
<td>SCSJ[3:2]</td>
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<tr>
<td>CLKEN[3:2]</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>MWEJ2</td>
<td>SRASJ2</td>
<td>SCASJ2</td>
<td>SCSJ[5:4]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLKEN[5:4]</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>MWEJ3</td>
<td>SRASJ3</td>
<td>SCASJ3</td>
<td>SCSJ[7:6]</td>
<td></td>
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<tr>
<td>CLKEN[7:6]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CLKEN[1:0]  
CLKEN[3:2]  
CLKEN[5:4]  
CLKEN[7:6]  

64-bit DIMM
3.7.6 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-V is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING. If only 4 banks of single sided DRAM SIMMs or 2 banks of double sided DRAM SIMMs or 8 banks of single sided DRAM DIMMs or 4 banks of double sided DRAM DIMMs are designed in motherboard, M1541 is designed to be TTL free for the DRAM control signals buffer.

3.8 CPU-to-PCI Posted Write Buffer

The M1541 integrates a 6-DWORD CPU-to-PCI posted write buffer to enhance the CPU-to-PCI performance. With this buffer, the M1541 can minimize the latency of CPU-to-PCI write cycles and maximize the concurrency of CPU bus and PCI bus when CPU writes data to PCI bus. The PCI burst write cycles and fast back-to-back cycles for CPU-to-PCI access are also supported by this buffer.

In addition, the M1541 CPU-to-PCI posted write buffer supports data merge, it can improve the CPU-to-PCI non-32 bits access performance.

3.9 PCI MASTER Latency and Throughput Analysis

The M1541 includes a smart PCI-to-DRAM interface, including a smart deep PCI-to-DRAM buffer and the enhanced PCI arbiter. All these components are designed to optimize the system performance and maximize the PCI bus bandwidth.

3.9.1 Smart Deep Post Write & Pre-fetch Buffer

The smart deep PCI-to-DRAM buffer of M1541 plays the key role to boost PCI master read/write performance. It consists of 80 DWORDs posted write buffer and 22 DWORDs pre-fetch buffer.

The 80 DWORDs PCI-to-DRAM posted write buffers enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 write back merge and smart buffer management, the M1541 can sustain the ultimate 133-Mbytes/sec bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and write back cycle, the DRAM types and L2 types.

On the other hand, to optimize the PCI master read performance when accessing DRAM, the M1541 includes 22 DWORDs PCI-to-DRAM read pre-fetch buffers. With the implementation of L1/L2 write back and smart buffer management, the M1541 can sustain the ultimate 133 Mbytes/sec bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, write back cycle and L2 types.
Considering the performance and concurrency of multi-master systems, for example the MPEG/Multimedia applications, the PCI-to-DRAM read pre-fetch buffer of M1541 is configured as two independent units. Each unit pre-fetches and keeps data independently with the other one. With this configuration, the M1541 minimizes the PCI master read latency and reduces the overhead of snooping and pre-fetching.

3.9.2 PCI 2.1 Compliant

The M1541 is fully compliant to the PCI 2.1 Specification. The M1541 supports Passive Release and programmable latency control timers for the first and subsequent data transaction. With the flexible PCI latency control, it can achieve the best system performance.

3.9.3 Pipelined Snoop Ahead

The M1541 utilizes an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. While snooping L1 & L2, the M1541 also performs speculative read to DRAM such that the latency of master read cycle can be minimized. It combines with the deep smart read/write buffer to optimize PCI master performance.
3.9.4 PCI Arbiter

The M1541 integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism. The arbitration algorithm is also designed to minimize the snoop overhead. Besides the M1533/M1543 ISA bridge and AGP master, the M1541 supports up to 5 PCI masters to make the system motherboard design more flexible and engaging.

To balance the bandwidth of ISA masters and PCI masters and utilize the most bandwidth of PCI bus, the M1541 also supports passive release of PCI 2.1 latency requirements, which makes PCI master access possible when ISA master is active. By this way, the ALADDIN-V can target the best system performance and the most concurrency between PCI bus and ISA bus.

3.9.5 ACPI Support

The M1541 provides the scheme to support ACPI relative functions. By means of PM2_BASE_ADDRESS register (Index-E8h - Index-E9h ) and PM2_CONTROL register (Index-EAh bits[1:0]), software can easily enable/disable PCI arbiter as ACPI requirement. In addition, PCIMRQJ signal makes ISA Bridge aware of PCI master bus request to generate SMI/SCI.

3.10 Low Power Features

The ALADDIN-V supports sophisticated power saving features, called Power On Suspend (Sleeping), Suspend to DRAM (Suspend), and Suspend to Disk. Under Power On Suspend state, the system will turn off the signal event of host and keep the DRAM refresh active through the M1541 DRAM interface that is triggered by a 32.768KHz clock source. After the Power On suspend event is triggered, by programming a bit of M1533/M1543 internal register, the M1533/M1543 will initiate a handshake with the M1541. During the handshake, the M1533/M1543 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH circuit to sustain the DRAM data. Theoretically, the only power request under the Power On suspend is the circuit of DRAM suspend refresh. M1541 core has two different power planes, one for the Suspend Refresh circuit, the other is for the other circuit except Suspend Refresh circuit. During Suspend to DRAM state, the system designer can shut off the power except the DRAM suspend refresh circuit to save more system power. Under the Suspend to Disk, only the M1533/M1543 resume circuit is powered and get the minimized system power consumption.

The M1541 and the M1533/M1543 are designed with a very sophisticated I/O circuit and to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the Power On suspend can provide the system a very efficient STAND-ON feature that is more demanding in future home PC systems for Microsoft On Now technology OS.

In the M1533/M1543 of ALADDIN-V, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one
might design a dedicated PMU device to accompany the Power On suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-V provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

3.11 DRAM Refresh

The M1541 provides CAS-before-RAS (CBR) refresh and RAS-only refresh for FPM DRAM, CAS-before-RAS (CBR) refresh and RAS-only refresh and Extended refresh and self refresh for EDO DRAM, and CAS-before-RAS (CBR) refresh and Self refresh for SDRAMs. FPM/EDO refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h Bits[2:0].
3.12 ECC/Parity Algorithm

The M1541 provides an ECC DRAM data integrity feature. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. The M1541 will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1541. The M1541 will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read cycle is performed. The M1541 also corrects all single-bit errors and the corrected data is then transferred to the requester (CPU or PCI). This corrected data will not be written back to DRAM in the current M1541 version. The ECC errors are latched until cleared by software. The software programmer also can detect 64 from 72-bit wide SIMMs or check ECC circuit operations via the ECC (parity) test mode. The ECC check bits (or parities) can be forced to any value during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLKIN when the ECC feature is enabled.

The M1541 also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 50h bit0 is set to '0'. The DRAM parity checking error reporting condition and status also are defined in Index 50h-51h. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode. The conventional Parity check will not degrade the system performance.

3.13 AGP and PCI-to-PCI bridge

The M1541 has a built in PCI-to-PCI bridge device to support the AGP interface. The Device ID is M5247. Behind the PCI to PCI bridge is an 66MHz PCI bus which meets the PCI revision 2.1 specification to support the AGP interface. The interface provides three significant performance extensions to the PCI specification which are intended to optimize the AGP for high performance 3D graphics applications. These extensions are

1. Deep pipeline memory read buffer (32 QWORDs) and memory write buffer (16 QWORDs), fully hiding memory access latency
2. Demultiplexing of address and data on the bus use the “IDLE band” signals, allowing almost 100% bus efficiency
3. AC timing for 133 MHz data transfer rate, up to 533 Mbytes/sec data throughput

The M1541 supports a physically, logically and electrically independent AGP interface. Support both the PIPEJ and SBA[7-0] addressing method and RBFJ flow control. The design is following the AGP revision 1.0 specification. The interface will support the PCI 66 mode, AGP 1X mode and 2X modes.

When at PCI 66 mode, the FRAMEJ protocol will be followed.
When at 1X transfer mode, the operation is similar to the PCI. All timings are referenced to the AGP clock. It will provide a peak bandwidth of 266Mbyte/sec.

When at 2X transfer mode, the data transfer rate of the AD, C/BEJ and SBA signals are double. With 2X transfer, QWORD transfers only require one clock cycle, and sideband commands only require one clock per 16-bit command.

For maximum software compatibility, two-level GART (Graphics Address Re-mapping Table) is set up and maintained by mini-port driver supported by ALi. So the actual table implementation is abstracted to a common API.

Besides, the 8 DWORDs PCI to PCI_66 posted write buffer and the 2 DWORDs PCI_66 to PCI posted write buffer make M1541 perform outstanding multi-master system performance. Especially when AGP 3D engine on AGP bus and video processor like MPEG2 accelerator on 33 MHz PCI bus.
### Section 4: Configuration Registers

#### 4.1 Register Summary:

**Configuration Cycle Ports**

<table>
<thead>
<tr>
<th>IO address</th>
<th>Attribute</th>
<th>Name</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0CF8h</td>
<td>Read/Write</td>
<td>CFGADR - Configuration Address Register</td>
<td>00000000h</td>
</tr>
<tr>
<td>0CFCh</td>
<td>Read/Write</td>
<td>CFGDAT - Configuration Data Register</td>
<td>00000000h</td>
</tr>
</tbody>
</table>

**M1541 PCI Configuration Space Mapped Registers**

<table>
<thead>
<tr>
<th>Index</th>
<th>Attribute</th>
<th>Name</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>01h-00h</td>
<td>Read only</td>
<td>VID - Vendor Identification Register</td>
<td>10B9h</td>
</tr>
<tr>
<td>03h-02h</td>
<td>Read only</td>
<td>DID - Device Identification Register</td>
<td>1541h</td>
</tr>
<tr>
<td>05h-04h</td>
<td>Read/Write</td>
<td>COM - Command Register</td>
<td>0006h</td>
</tr>
<tr>
<td>07h-06h</td>
<td>Read Only,</td>
<td>DS - Device Status Register</td>
<td>0410h</td>
</tr>
<tr>
<td></td>
<td>Read/Write Clear</td>
<td></td>
<td></td>
</tr>
<tr>
<td>08h</td>
<td>Read Only</td>
<td>RI - Revision ID Register</td>
<td>00h</td>
</tr>
<tr>
<td>09h</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>0Ah</td>
<td>Read Only</td>
<td>SCC - Sub-Class Code Register</td>
<td>00h</td>
</tr>
<tr>
<td>0Bh</td>
<td>Read Only</td>
<td>CC - Class Code Register</td>
<td>06h</td>
</tr>
<tr>
<td>0Ch</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>0Dh</td>
<td>Read/Write</td>
<td>LT - PCI Latency Timer value</td>
<td>20h</td>
</tr>
<tr>
<td>0Fh</td>
<td>Read only</td>
<td>Device 0 Head Type Register</td>
<td>00h</td>
</tr>
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<td></td>
<td>Read only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>13h-10h</td>
<td>Read only</td>
<td>Device 0 Aperture Base Configuration Register</td>
<td>00000000h</td>
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<td>28h-14h</td>
<td>Read only</td>
<td>Reserved Registers</td>
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<td>2Dh-2Ch</td>
<td>Locked Read/Write</td>
<td>SVID - Sub-Vendor Identification</td>
<td>10B9h</td>
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<tr>
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<td>SDID - Sub-Device Identification</td>
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<td>L2CCI - L2 Cache Configuration-1</td>
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<td>PLCTL - Pipe Line Control</td>
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<td>SDRAM Configuration-2</td>
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<td>DRAM Controller Configuration</td>
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<td>Read/Write</td>
<td>DRAM Sequencing Configuration</td>
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<td>DRAM Master Latency-1</td>
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<td>4Dh</td>
<td>Read/Write</td>
<td>DRAM Master Latency-2</td>
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<tr>
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<td>Read/Write</td>
<td>DRAM Master Slice-1</td>
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<td>Read/Write</td>
<td>DRAM Master Slice-2</td>
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<td>51h</td>
<td>Read/Write</td>
<td>ECCE - ECC or Parity Error Status.</td>
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<td>DRAM Posted Write Buffer Control.</td>
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<td>Memory Hole.</td>
<td>00h</td>
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<td>55h</td>
<td>Read/Write</td>
<td>SMRM - SMRAM Mapping.</td>
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<td>Read/Write</td>
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<td>Read/Write</td>
<td>DRAM Refresh Control</td>
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<td>DRAM Page Mode Counter Control</td>
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<td>DB0CII - DRAM Row0 Configuration - 2</td>
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<td>6Fh</td>
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<td>DB7CII - DRAM Row7 Configuration - 2</td>
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<td>Read/Write</td>
<td>SDM256MB[7:0] - 256Mbit SDRAM select</td>
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<td>Read/Write</td>
<td>SDM4MBANK[7:0] - SDRAM internal 2/4 Banks select</td>
<td>00h</td>
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<td>72h</td>
<td>Read/Write</td>
<td>SDRAM100 - SDRAM 100 MHz timing select</td>
<td>00h</td>
</tr>
<tr>
<td>73h</td>
<td>Read/Write</td>
<td>SDRAM100 - SDRAM 100 MHz timing select</td>
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</tr>
<tr>
<td>83h-74h</td>
<td>Read only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>85h-84h</td>
<td>Read/Write</td>
<td>PCI Programmable Frame Buffer Memory Region</td>
<td>00h</td>
</tr>
<tr>
<td>86h</td>
<td>Read/Write</td>
<td>CPU to PCI Write Buffer Option</td>
<td>00h</td>
</tr>
<tr>
<td>87h</td>
<td>Read/Write</td>
<td>H2PO - CPU to PCI Option</td>
<td>00h</td>
</tr>
</tbody>
</table>
### PCI 33 to Host Interface

<table>
<thead>
<tr>
<th>Index</th>
<th>Attribute</th>
<th>Name</th>
<th>Default value</th>
</tr>
</thead>
<tbody>
<tr>
<td>88h</td>
<td>Read/write</td>
<td>P2HO - PCI to Main Memory / PCI Arbiter Option</td>
<td>00h</td>
</tr>
<tr>
<td>89h</td>
<td>Read/write</td>
<td>PCI Arbiter Time Slice</td>
<td>20h</td>
</tr>
<tr>
<td>8Ah</td>
<td>Read/write</td>
<td>CPU Arbiter Time Slice</td>
<td>20h</td>
</tr>
<tr>
<td>8Bh</td>
<td>Read/write</td>
<td>PCIRC - PCI Retry Control for P2H cycle</td>
<td>00h</td>
</tr>
<tr>
<td>8Ch</td>
<td>Read/write</td>
<td>PCI to Main Memory Option</td>
<td>00h</td>
</tr>
<tr>
<td>8Dh</td>
<td>Read/write</td>
<td>PCI Clock Control</td>
<td>00h</td>
</tr>
<tr>
<td>8Eh</td>
<td>Read/write</td>
<td>Internal Arbiter Write Control</td>
<td>00h</td>
</tr>
<tr>
<td>8Fh</td>
<td>Read/write</td>
<td>Internal Arbiter P2H Read Control</td>
<td>00h</td>
</tr>
<tr>
<td>90h</td>
<td>Read/write</td>
<td>LRWCTL – Lock Read/Write Control</td>
<td>00h</td>
</tr>
<tr>
<td>91h</td>
<td>Read/write</td>
<td>BRSYCTL - Broadcast and Synchronous Cycle Control</td>
<td>00h</td>
</tr>
<tr>
<td>0AFh-92h</td>
<td>Read only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
</tbody>
</table>

### AGP Interface Registers

<table>
<thead>
<tr>
<th>Index</th>
<th>Attribute</th>
<th>Name</th>
<th>Default value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0B3h-0B0h</td>
<td>Read only</td>
<td>AGP Capability Identifier Registers</td>
<td>00100020h</td>
</tr>
<tr>
<td>0B7h-0B4h</td>
<td>Locked Read/write</td>
<td>AGP Status Registers</td>
<td>1C000003h</td>
</tr>
<tr>
<td>0BBh-0B8</td>
<td>Read/write</td>
<td>AGP Command/Enable Registers</td>
<td>00000000h</td>
</tr>
<tr>
<td>0BFh-0BCh</td>
<td>Read/write</td>
<td>Aperture Control Register</td>
<td>00000000h</td>
</tr>
<tr>
<td>0C3h-0C0h</td>
<td>Read/write</td>
<td>GTLB Control Register</td>
<td>00000000h</td>
</tr>
<tr>
<td>0D3h-0D0h</td>
<td>Read/write</td>
<td>AGP Command/Enable Registers</td>
<td>00000000h</td>
</tr>
<tr>
<td>0D8h</td>
<td>Read/write</td>
<td>AGP Control Register I</td>
<td>0BFh</td>
</tr>
<tr>
<td>0C9h</td>
<td>Read/write</td>
<td>AGP Control Register II</td>
<td>0Ah</td>
</tr>
<tr>
<td>0C7h-0C4h</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
</tbody>
</table>

### Green Function Registers

<table>
<thead>
<tr>
<th>Index</th>
<th>Attribute</th>
<th>Name</th>
<th>Default value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0E0h</td>
<td>Locked Read/write</td>
<td>Power Management Capability Identifier Register</td>
<td>01h</td>
</tr>
<tr>
<td>0E1h</td>
<td>Locked Read/write</td>
<td>Power Management Next Item Pointer Register</td>
<td>00h</td>
</tr>
<tr>
<td>0E3h-0E2h</td>
<td>Locked Read/write</td>
<td>Power Management Capabilities Register</td>
<td>0000h</td>
</tr>
<tr>
<td>0E5h-0E4h</td>
<td>Locked Read/write</td>
<td>Power Management Control and Status Register</td>
<td>0000h</td>
</tr>
<tr>
<td>0E6h</td>
<td>Locked Read/write</td>
<td>PMCSR PCI to PCI Bridge Support Extensions</td>
<td>0000h</td>
</tr>
<tr>
<td>0E7h</td>
<td>Locked Read/write</td>
<td>Data Register</td>
<td>00h</td>
</tr>
<tr>
<td>0E9h-0E8h</td>
<td>Locked Read/write</td>
<td>Base Address of ACPI PM2_CNTL Port</td>
<td>00000h</td>
</tr>
<tr>
<td>0EAh</td>
<td>Read/Write</td>
<td>PM2C - ACPI PM2_CNTL Function</td>
<td>00h</td>
</tr>
<tr>
<td>0EBh</td>
<td>Read/Write</td>
<td>GCKCTL - Gated Clock Control Register</td>
<td>00h</td>
</tr>
<tr>
<td>0ECh</td>
<td>Read/Write</td>
<td>POD - Programmable Output Driving Strength</td>
<td>00h</td>
</tr>
<tr>
<td>0EDh</td>
<td>Read/Write</td>
<td>Hardware Setting Register</td>
<td>00h</td>
</tr>
<tr>
<td>0EEh</td>
<td>Read/Write</td>
<td>Miscellaneous - 1</td>
<td>00h</td>
</tr>
<tr>
<td>0EFh</td>
<td>Read/Write</td>
<td>Miscellaneous - 2</td>
<td>00h</td>
</tr>
<tr>
<td>0F3h</td>
<td>Read/Write</td>
<td>Predict the next SDM Control Signal</td>
<td>00h</td>
</tr>
<tr>
<td>0F5h</td>
<td>Read/Write</td>
<td>DMRDPL Status Register</td>
<td>00h</td>
</tr>
<tr>
<td>0F6h</td>
<td>Read/Write</td>
<td>GDPL Status Register</td>
<td>00h</td>
</tr>
<tr>
<td>0F7h</td>
<td>Read/write</td>
<td>GCLK PLL Control Register</td>
<td>00h</td>
</tr>
<tr>
<td>0FFh-0EEh</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
</tbody>
</table>

### ACPI PM2_CNTL I/O Port

<table>
<thead>
<tr>
<th>IO address</th>
<th>Attribute</th>
<th>Name</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000h-0FFFFh</td>
<td>Read/Write</td>
<td>PM2_CNTL - ACPI PM2_CNTL I/O Port</td>
<td>The address is defined by M1541 index 0E9h-0E8h</td>
</tr>
</tbody>
</table>
### M5243 Configuration Space Mapped Registers

<table>
<thead>
<tr>
<th>Index</th>
<th>Attribute</th>
<th>Name</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>01h-00h</td>
<td>Read Only</td>
<td>VID - Vendor Identification Register</td>
<td>10B9h</td>
</tr>
<tr>
<td>03h-02h</td>
<td>Locked Read/Write</td>
<td>DID - Device Identification Register</td>
<td>5243h</td>
</tr>
<tr>
<td>05h-04h</td>
<td>Read/Write</td>
<td>COM - Command Register</td>
<td>0006h</td>
</tr>
<tr>
<td>07h-06h</td>
<td>R Only, R/W Clear</td>
<td>DS - PCI_66 Device Status Register</td>
<td>0400h</td>
</tr>
<tr>
<td>08h</td>
<td>Read Only</td>
<td>RI - Revision ID Register</td>
<td>00h</td>
</tr>
<tr>
<td>09h</td>
<td>Read Only</td>
<td>Reserved Register</td>
<td>00h</td>
</tr>
<tr>
<td>0Ah</td>
<td>Read Only</td>
<td>SCC - Sub-Class Code Register</td>
<td>04h</td>
</tr>
<tr>
<td>0Bh</td>
<td>Read Only</td>
<td>CC - Class Code Register</td>
<td>06h</td>
</tr>
<tr>
<td>0Ch</td>
<td>Read Only</td>
<td>Reserved Register</td>
<td>00h</td>
</tr>
<tr>
<td>0Dh</td>
<td>Read Only</td>
<td>LT - PCI Latency Timer value</td>
<td>20h</td>
</tr>
<tr>
<td>18h-0Eh</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>19h</td>
<td>Read/Write</td>
<td>Secondary Bus Number Register</td>
<td>00h</td>
</tr>
<tr>
<td>1Ah</td>
<td>Read/Write</td>
<td>Subordinate Bus Number Register</td>
<td>00h</td>
</tr>
<tr>
<td>1Bh</td>
<td>Read/Write</td>
<td>Secondary Master Latency Timer Value</td>
<td>20h</td>
</tr>
<tr>
<td>1Ch</td>
<td>Read/Write</td>
<td>I/O Base Address Register</td>
<td>0F0h</td>
</tr>
<tr>
<td>1Dh</td>
<td>Read/Write</td>
<td>I/O Limit Address Register</td>
<td>00h</td>
</tr>
<tr>
<td>1Fh-1Eh</td>
<td>Read/Write</td>
<td>Secondary PCI-to-PCI Status Register</td>
<td>00h</td>
</tr>
<tr>
<td>21h-20h</td>
<td>Read/Write</td>
<td>Memory Base Address Register</td>
<td>0FFF0h</td>
</tr>
<tr>
<td>23h-22h</td>
<td>Read/Write</td>
<td>Memory Limit Address Register</td>
<td>0000h</td>
</tr>
<tr>
<td>25h-24h</td>
<td>Read/Write</td>
<td>Pre-fetchable Memory Base Address Register</td>
<td>0FFF0h</td>
</tr>
<tr>
<td>27h-26h</td>
<td>Read/Write</td>
<td>Pre-fetchable Memory Limit Address Register</td>
<td>0000h</td>
</tr>
<tr>
<td>33h-28h</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>34h</td>
<td>Locked Read/Write</td>
<td>Capability Pointer Register</td>
<td>0E0h</td>
</tr>
<tr>
<td>3Dh-35h</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>3Fh-3Eh</td>
<td>Read/Write</td>
<td>PCI-to-PCI Bridge Control Register</td>
<td>0000h</td>
</tr>
<tr>
<td>83h-40h</td>
<td>Read Only</td>
<td>Reserved Registers</td>
<td>00h</td>
</tr>
<tr>
<td>85h-84h</td>
<td>Read/Write</td>
<td>PCI_66 Programmable Frame Buffer Memory Region</td>
<td>0000h</td>
</tr>
<tr>
<td>86h</td>
<td>Read/Write</td>
<td>CPU to PCI_66 Write Buffer Option</td>
<td>00h</td>
</tr>
<tr>
<td>87h</td>
<td>Read/Write</td>
<td>CPU to PCI_66 Option</td>
<td>00h</td>
</tr>
</tbody>
</table>

**PCI_66 to Host Interface**

<table>
<thead>
<tr>
<th>Index</th>
<th>Attribute</th>
<th>Name</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>88h</td>
<td>Read/Write</td>
<td>PCI_66 to Main Memory /PCI_66 Arbiter Option</td>
<td>00h</td>
</tr>
<tr>
<td>89h</td>
<td>Read/Write</td>
<td>PCI_66 Arbiter Time Slice</td>
<td>20h</td>
</tr>
<tr>
<td>8Ah</td>
<td>Read/Write</td>
<td>CPU Arbiter Time Slice</td>
<td>20h</td>
</tr>
<tr>
<td>8Bh</td>
<td>Read/Write</td>
<td>PCI_66 Retry Control for PCI-66 to Host Cycle</td>
<td>00h</td>
</tr>
<tr>
<td>Offset</td>
<td>Access</td>
<td>Description</td>
<td>Value</td>
</tr>
<tr>
<td>--------</td>
<td>----------</td>
<td>--------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>8Ch</td>
<td>Read/Write</td>
<td>PCI_66 to Main Memory Option</td>
<td>00h</td>
</tr>
<tr>
<td>8Dh</td>
<td>Read Only</td>
<td>Reserved Register</td>
<td>00h</td>
</tr>
<tr>
<td>8Eh</td>
<td>Read/Write</td>
<td>AGP Write/AGP Read Arbiter Time Slice</td>
<td>20h</td>
</tr>
<tr>
<td>8Fh</td>
<td>Read/Write</td>
<td>PCI_33 to PCI_66 Write Arbiter Time Slice</td>
<td>20h</td>
</tr>
<tr>
<td>0DFh-90h</td>
<td>Read Only</td>
<td>Reserved Register</td>
<td>00h</td>
</tr>
</tbody>
</table>

**PCI_66 Green Function Support**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Access</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0E0h</td>
<td>Locked Read/write</td>
<td>PCI_66 Power Management Capability Identifier Register</td>
<td>01h</td>
</tr>
<tr>
<td>0E1h</td>
<td>Locked Read/write</td>
<td>PCI_66 Power Management Next Item Pointer Register</td>
<td>00h</td>
</tr>
<tr>
<td>0E3h-0E2h</td>
<td>Locked Read/write</td>
<td>PCI_66 Power Management Capabilities Register</td>
<td>0000h</td>
</tr>
<tr>
<td>0E5h-0E4h</td>
<td>Locked Read/write</td>
<td>PCI_66 Power Management Control and Status Register</td>
<td>0000h</td>
</tr>
<tr>
<td>0E6h</td>
<td>Locked Read/write</td>
<td>PCI_66 PMCSR PCI-to-PCI Bridge Support extensions</td>
<td>00h</td>
</tr>
<tr>
<td>0E7h</td>
<td>Locked Read/write</td>
<td>Data Register</td>
<td>00h</td>
</tr>
<tr>
<td>0FFh-E8h</td>
<td>Read Only</td>
<td>Reserved Register</td>
<td>00h</td>
</tr>
</tbody>
</table>
4.2 Configuration Cycle Ports

I. M1541 PCI Mechanism #1 Configuration Cycle Ports

I/O Address : 0CF8h
Register Name : CFGADR - Configuration Address Register
Default Value : 00000000h
Attribute : Read/Write
Size : This register must be 32-bit I/O access in PCI configuration access mechanism #1. An 8-bit or 16-bit access will pass through the Configuration Address Register onto the PCI bus.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 31 (0)     | PCI Configuration Space Access.  
0 : Configuration Disable.  
1 : Configuration Enable.  
When this bit is set to 1, accesses to PCI configuration space are enabled. Otherwise, accesses to PCI configuration space are disabled. |
| 30-24 (00h) | Reserved. |
| 23-16 (00h) | Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to the M1541 and a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on the PCI bus. |
| 15-11 (00h) | Device Number. It is used by M1541 to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when Bus Number is 0h. As for the others, the M1541 will send the configuration to a PCI or PCI bridge device. |
| 10-8 (0h)   | Function Number. It is used to select a specific device function during initialization. |
| 7-2 (00h)   | Register Number. It is used to select a specific register during initialization. |
| 1-0 (0h)    | Reserved. Fixed at '00'. |

I/O Address : 0CFCh
Register Name : CFGDAT - Configuration Data Register
Default Value : 00000000h
Attribute : Read/Write
Size : This register may be 8-bit or 16-bit or 32-bit I/O access in configuration access mechanism #1.
Description : This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU access of 8, 16 or 32-bit wide to this register are supported.

Note : M1541 only supports PCI mechanism #1 access.
4.3 M1541 PCI Configuration Space Mapped Registers

The M1541 will respond to CPU/PCI configuration access for which AD11=IDSEL is high during the address phase.

Register Index: 01h-00h
Register Name: VID - Vendor Identification Register
Default Value: 10B9h
Attribute: Read Only
Size: 16 bits
Description: This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index: 03h-02h
Register Name: DID - Device Identification Register
Default Value: 1541h
Attribute: Read Only
Size: 16 bits
Description: This is a 16-bit value assigned to the M1541.
Register Index : 05h-04h  
Register Name : COM - Command Register  
Default Value : 0006h  
Attribute : Read/Write  
Size : 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-9 (000h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
| 8 (0) | Enable the SERRJ Output Driver.  
0 : Disable.  
1 : Enable.  
SERRJ uses an o/d (Open Drain) pad in M1541. The motherboard design should use a pull-up resistor (2.2KΩ) to keep this pin logic high. When the DRAM ECC/Parity check or the PCI Parity check is enabled and an error is found, the M1541 will drive SERRJ low to M1533/M1543 generate NMI when this bit is enabled. Disabling the SERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 once memory has been scrubbed by BIOS in systems that wish to report DRAM ECC/Parity error. |
| 7 (0) | Enable Address/Data Stepping. M1541 does not support this feature. Write to this bit has no effect. |
| 6 (0) | Respond to Parity Errors.  
0 : Disable.  
1 : Enable.  
The M1541 will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M1541 will assert SERRJ and set the Parity Error Bit in the DS register. |
| 5 (0) | Enable VGA Palette Snooping. M1541 does not support this feature. Write to this bit has no effect. |
| 4 (0) | Enable Postable Memory Write Command. M1541 does not support this feature. Write to this bit has no effect. |
| 3 (0) | Enable Special Cycle. M1541 does not support this feature. Write to this bit has no effect. |
| 2 (1) | Control to Act As a PCI Bus Master. M1541 does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect. |
| 1 (1) | Enable Response to Memory Access. M1541 always accepts PCI master accesses to local memory. This bit is read only and always set to 1. Write to this bit has no effect. |
| 0 (0) | Enable Response to I/O Access. M1541 does not respond to any PCI master I/O accesses. Write to this bit has no effect. |
Register Index: 07h-06h
Register Name: DS - Device Status Register
Default Value: 0410h
Attribute: Read Only, Read/Write Clear
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 (0)</td>
<td>Detected Parity Error. This bit is set by the M1541 whenever it detects a parity error in a PCI transaction even if parity error handling is disabled (as controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.</td>
</tr>
<tr>
<td>14 (0)</td>
<td>Signaled System Error. The M1541 will set this bit whenever it asserts SERRJ. Software can reset this bit to 0 by writing a 1 to it.</td>
</tr>
<tr>
<td>13 (0)</td>
<td>Received Master Abort. This bit is set by M1541 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>12 (0)</td>
<td>Received Target Abort. This bit is set by the M1541 whenever its initiated transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>11 (0)</td>
<td>Send Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M1541 never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.</td>
</tr>
<tr>
<td>10-9 (10)</td>
<td>DEVSELJ Timing. 00: Fast. 01: Medium. 10: Slow. The M1541 timing for DEVSELJ assertion. Slow timing is selected.</td>
</tr>
<tr>
<td>8-5 (0h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>4 (1)</td>
<td>Capability List (CAP_LIST) 1: The configuration space implements a list of capabilities (Read Only)</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Register Index: 08h
Register Name: RI - Revision ID Register
Default Value: 00h (A0 Stepping)
Attribute: Read Only
Size: 8 bits
Description: This register contains the version number of M1541. The value 00 means A0 stepping. This register will be different at different versions of M1541.
Register Index: 09h
Register Name: Reserved Registers
Default Value: 00h
Attribute: Read Only

Register Index: 0Ah
Register Name: SCC - Sub-Class Code Register
Default Value: 00h: Host Bridge
Attribute: Read Only
Size: 8 bits
Description: These registers contain the sub-Class Codes of the M1541.

Register Index: 0Bh
Register Name: CC - Class Code Register
Default Value: 06h, Bridge device
Attribute: Read Only
Size: 8 bits
Description: These registers contain the Class Codes of the M1541.
Register Index : 0Ch
Register Name : Reserved Registers
Default Value : 00h
Attribute : Read Only

Register Index : 0Dh
Register Name : LT - PCI Latency Timer value
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3 (04h)</td>
<td>Master Latency Timer Count Value. LT is used to control the amount of time the M1541, as a bus master, can burst data to the PCI Bus. It can be used to guarantee a minimum amount of the system resources.</td>
</tr>
<tr>
<td>2-0 (0h)</td>
<td>Reserved. They are assumed to be 0 when determining the Count Value.</td>
</tr>
</tbody>
</table>

Register Index : 0Eh
Register Name : Device 0 Head Type Register
Default Value : 00h
Attribute : Read Only

Register Index : 0Fh
Register Name : Reserved Registers
Default Value : 00h
Attribute : Read Only

Register Index : 13h-10h
Register Name : Device 0 Aperture Base Configuration Register
Default Value : 00000000h
Attribute : Read Only
Size : 32 bits

Description :

<table>
<thead>
<tr>
<th>Index 0BCh bit[3-0]</th>
<th>Index 13h-10h = D[31-0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0MB</td>
<td>D[31-0] = '0'</td>
</tr>
<tr>
<td>0001 1MB</td>
<td>D[31-20] R/W</td>
</tr>
<tr>
<td></td>
<td>D[19:0] = '0'</td>
</tr>
<tr>
<td>0010 2MB</td>
<td>D[31-21] R/W</td>
</tr>
<tr>
<td></td>
<td>D[20:0] = '0'</td>
</tr>
</tbody>
</table>
### Register Index:
- **2Bh-14h**

### Register Name:
- **Reserved Registers**

### Default Value:
- **00h**

### Attribute:
- **Read Only**

<table>
<thead>
<tr>
<th>Register</th>
<th>Size</th>
<th>Memory Address</th>
<th>Access</th>
<th>Default Value</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>0011</td>
<td>4MB</td>
<td>D[31:22] R/W</td>
<td>D[21:0]=0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0100</td>
<td>8MB</td>
<td>D[31:23] R/W</td>
<td>D[22:0]=0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0110</td>
<td>16MB</td>
<td>D[31:24] R/W</td>
<td>D[23:0]=0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0111</td>
<td>32MB</td>
<td>D[31:25] R/W</td>
<td>D[24:0]=0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>64MB</td>
<td>D[31:26] R/W</td>
<td>D[25:0]=0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1001</td>
<td>128MB</td>
<td>D[31:27] R/W</td>
<td>D[26:0]=0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1010</td>
<td>256MB</td>
<td>D[31:28] R/W</td>
<td>D[27:0]=0'</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register Index : 2Dh-2Ch
Register Name : SVID - Sub-Vendor Identification
Default Value : 10B9h (for Acer Labs Inc)
Attribute : Locked Read/Write
Size : 16 bits
Description : If Index-90h bit0 = 1, then this port can be Read or Written.

Register Index : 2Fh-2Eh
Register Name : SDID - Sub-Device Identification
Default Value : 1541h
Attribute : Locked Read/Write
Size : 16 bits
Description : If Index-90h bit0 = 1, then this port can be Read or Written.

Register Index : 33h-30h
Register Name : Reserved Registers
Default Value : 00h
Attribute : Read Only

Register Index : 34h
Register Name : Device 0 Capabilities Pointer
Default Value : 0B0h
Attribute : Locked Read/Write
Size : 8 bits
Description : Pointer to the start of AGP standard register block
If index-90h bit 1=1, then this port can be Read or Written

Register Index : 3Fh-35h
Register Name : Reserved Registers
Default Value : 00h
Attribute : Read Only
Register Index: 40h
Register Name: L12CP - L1, L2 Cache Performance
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Reserved</td>
</tr>
<tr>
<td>6 (0/1)</td>
<td>Use M1541 as internal TAG RAM</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Use M1541 as internal MESI</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Supports Cyrix M1/M2 &quot;1+4&quot; Burst Mode &amp; K6 Write Allocation Feature.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Supports M1/M2 Linear Burst Order.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>L1 Snoop HITMJ Check Point.</td>
</tr>
</tbody>
</table>

When powering on, this value will be decided by the HA[23]. The default is pull low and set 0 to Disable the internal TAG. If pull high HA[23], the power on value will set to 1 to enable the TAG.

After powering on, this bit can be read and written.

This bit is used to support the internal MESI RAMs. When system uses the internal MESI RAMs, this bit must set to 0 (Power on default) to enable internal MESI RAMs for best performance.

When disabling this bit, the MESI circuit will use External TAG SRAM as MESI SRAM.

This bit is used to support the Cyrix M1/M2 "1+4" mode to toggle cache address, DRAM Memory address, and issues the correct KENJ disregarding CPU CACHEJ if it is a local memory cycle.

This bit is also used to support K6 Write Allocation Feature. If this bit is enabled, M1541 will assert KENJ during CPU single local memory write cycle.

This bit is used to support the Cyrix M1/M2 linear burst mode to toggle cache address and DRAM Memory address. When it is disabled, Intel toggle mode (interleaved burst) is selected.

This bit controls the HITMJ strobe point during L1 snoop cycle. Value 0 is recommended during normal operation.
### L2 Cache Hit/Miss Check Point (L2 Hit/Miss)

- **0**: T3end (3rd CPU Clock after Sampling ADSJ).
- **1**: T2end (2nd CPU Clock after Sampling ADSJ).

This bit controls the cycle checkpoint of L2 access. When using internal TAG, the Value can be set to 1 for best performance. For external TAGs, the value is decided by the Host frequency and TAG RAM speed.

When set to T2end and L2 cache hit, the first BRDYJ sent to CPU will be at the third clock from ADSJ. When set to T3end and L2 cache hit, the first BRDYJ sent to CPU will be at the fourth clock from ADSJ.

### L1 Cache ON/OFF

- **0**: Disable Internal Cache
- **1**: Enable Internal Cache

This bit is used to disable or enable L1 cache. When this bit is reset to 0, the M1541 will negate KENJ to prevent either L1 or L2 line fill. When this bit is set to '1', the M1541 will assert KENJ for cacheable memory cycles.
Register Index: 41h
Register Name: L2CCI - L2 Cache Configuration-1
Default Value: Hardware Strobe Value
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7(0)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 6(0)       | CPU read DRAM command mode  
0: Synchronous mode  
1: Bypass mode  
When this bit is set to bypass mode, DRAM cycle will start at the same cycle assigned by host bus check point defined by index 40h bit 1. Otherwise, one additional clock is added to synchronize for decoding usage. |
| 5 (0/1)    | L2 Cache Bank Select.  
0: 1-bank Pipelined Burst SRAM / Memory Cache.  
1: 2-bank Pipelined Burst SRAM / Memory Cache.  
The default value is determined by power on hardware strobe from HA[19]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache. |
| 4 (0/1)    | L2 Cache Type Select.  
0: Pipelined Burst SRAM.  
1: MOSYS DRAM Cache.  
The default value is determined by hardware strobe from HA[22]. The system must implement the correct hardware strobe for Memory Cache use. |
| 3-2 (0/1,0/1) | L2 Cache Size.  
00: 256  
01: 512K.  
10: 1M.  
11: None.  
The default value is determined by hardware strobe from HA[21:20]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache. |
<table>
<thead>
<tr>
<th>1 (0)</th>
<th>TAG[9-8] Configuration.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 : TAG[9-8] are disabled.</td>
<td></td>
</tr>
<tr>
<td>1 : TAG[9-8] are enabled.</td>
<td></td>
</tr>
<tr>
<td>'1' means TAG[9-8] are used to extend cacheable region. When using external TAG SRAM and only one 8-bit wide SRAM is used, then the user must set to disable this bit. If using two 8-bit wide SRAMs or one 10-bit wide SRAM, then enable this bit. The more TAG width, the more cacheable memory range. To enable this bit, the index 41h bit 0 must set to 0.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>0 (0)</th>
<th>External TAG Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 : Enable</td>
<td></td>
</tr>
<tr>
<td>1 : Disable</td>
<td></td>
</tr>
<tr>
<td>This bit is used to choose the external TAG. When enabling this bit, at least one 8-bit wide SRAM should be connected to TAG[7-0].</td>
<td></td>
</tr>
</tbody>
</table>
The following L2 Cache Table shows the different configurations supported by M1541.

Table 4-1.  
Index 40h bit6=0 Disable internal TAG at all cache size
index 40h bit5=1 Enable internal MESI support

<table>
<thead>
<tr>
<th>Config</th>
<th>DATA SRAM</th>
<th>External TAG SRAM</th>
<th>Internal</th>
<th>Index</th>
<th>Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache Size</td>
<td>Size</td>
<td>Bank</td>
<td>Address lines</td>
<td>Address lines</td>
<td>Data Lines</td>
</tr>
<tr>
<td>256K</td>
<td>(32K32)*2 or (32K64)*1</td>
<td>1</td>
<td>A3-A17</td>
<td>A5-A17</td>
<td>A18-A25</td>
</tr>
<tr>
<td>512K</td>
<td>(64K32)*2 or (64K64)*1</td>
<td>1</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
</tr>
<tr>
<td>512K</td>
<td>(32K64)*2 or (32K32)*4</td>
<td>2</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
</tr>
<tr>
<td>1M</td>
<td>(64K32)*4 or (64K64)*2</td>
<td>2</td>
<td>A3-A19</td>
<td>A5-A19</td>
<td>A20-A26</td>
</tr>
<tr>
<td>256K</td>
<td>(32K32)*2 or (32K64)*1</td>
<td>1</td>
<td>A3-A17</td>
<td>A5-A17</td>
<td>A18-A27</td>
</tr>
<tr>
<td>512K</td>
<td>(64K32)*2 or (64K64)*1</td>
<td>1</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>512K</td>
<td>(32K64)*2 or (32K32)*4</td>
<td>2</td>
<td>A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
</tr>
<tr>
<td>1M</td>
<td>(64K32)*4 or (64K64)*2</td>
<td>2</td>
<td>A3-A19</td>
<td>A5-A19</td>
<td>A20-A28</td>
</tr>
</tbody>
</table>
Table 4-2. Index 40h bit6=1 Enable internal TAG at all cache size

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Config</th>
<th>DATA SRAM</th>
<th>Internal TAG SRAM</th>
<th>Internal MESI 8K1x4</th>
<th>Index 41h Bit[3-2]</th>
<th>Index 41h Bit[1-0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>256K</td>
<td>(32K32)*2 or (32K64)*1</td>
<td>1 A3-A17 A5-A17 A18-A27 8K10 256M</td>
<td>8K2 MESI</td>
<td>00</td>
<td>01</td>
<td></td>
</tr>
<tr>
<td>512K</td>
<td>(64K32)*2 or (64K64)*1</td>
<td>1 A3-A18 A5-A18 A19-A28 16K10 512M</td>
<td>16K2 MESI</td>
<td>01</td>
<td>01</td>
<td></td>
</tr>
<tr>
<td>512K</td>
<td>(32K32)*4 or (32K64)*2</td>
<td>2 A3-A18 A5-A18 A19-A28 16K10 512M</td>
<td>16K2 MESI</td>
<td>01</td>
<td>01</td>
<td></td>
</tr>
<tr>
<td>1M</td>
<td>64K32)*4 or (64K64)*2</td>
<td>2 A3-A19 A5-A19 A28-A31 (A20-A27 will use external TAG) 32K4 4G</td>
<td>32K2 MESI (one 32K1 is from internal TAG) External 32K8 TAG required</td>
<td>10</td>
<td>00</td>
<td></td>
</tr>
</tbody>
</table>
Register Index: 42h
Register Name: L2CCII - L2 Cache Configuration-2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>L2 TAG Output Delay.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to increase L2 Tag data hold time when M1541 wants to update the L2 Tag content. The M1541 will delay the Tag data output floating timing by one half CPU clock when this bit is enabled. A '1' is recommended during normal operation.</td>
</tr>
</tbody>
</table>

| 6 (0)      | CPU Single Read Cycle L2 Cache Allocation. |
|            | 0 : Enable.   |
|            | 1 : Disable.  |
|            | When this bit is disabled, the M1541 will only do the L2 Cache allocation after it decodes the CPU burst line-fill cycle. The CPU single read cycle will start a DRAM single read cycle if this cycle is a DRAM cycle and not hit the L2 Cache. When this bit is enabled, the M1541 will also do the L2 Cache allocation after it decodes the CPU single read cycle. The M1541 will issue the A HOLD to hold CPU cycle, start a burst DRAM read cycle to get the whole line data, write the date to the L2 Cache, and then de-assert A HOLD and return the BRDYJ to CPU. This feature is used to increase the L2 hit rate when CPU issues the single cycle instead of the line-fill cycle in some special application. A '0' is recommended in normal operation. |

| 5 (0)      | Cache-ability of Address Region from A0000h to BFFFFh. |
|            | 0 : Disable.  |
|            | 1 : Enable.   |
|            | This bit is used to enable the cache-ability of address region from A0000h to BFFFFh if this region is programmed as local memory (Index-54h bit3 =1). If Index-54h bit3 = 0, this bit must be 0. |

<p>| 4 (0)      | L2 Dirty Bit Setting. |
|            | 0 : Normal.      |
|            | 1 : Force Non-dirty (Dirty Bit =0). |</p>
<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3 (0) | L2 force Cache Hit  
0 : Disable  
1 : Enable  
When this bit is set to 1, it will force the read memory cycle all are L2 cache hit. This bit is used to initialize L2 cache. |
| 2 (0) | L2 Cache Miss or Invalidate.  
0 : Normal.  
1 : Force L2 Cache Miss or Invalidate. This will force non-dirty also.  
When this bit is set to 1, all tag lookups result in a miss. This bit is used to initialize L2 cache. This bit also forces all non-dirty situations. |
| 1 (0) | L2 Dirty Bit Setting.  
0 : Normal.  
1 : Force Dirty (Dirty Bit =1).  
When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force dirty. This bit can be used to flush L2 cache in green application. Software can set this bit and then read all L2 cache tag address to flush the cache data to DRAM. |
| 0 (0) | L2 Cache ON/OFF.  
0 : Disable External Cache.  
1 : Enable External Cache.  
This bit is used to disable or enable L2 cache. |
Register Index : 43h  
Register Name : PLCTL-Pipe Line Control  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Force Snoop INV</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>When set to enable, all the snoop cycles will be</td>
</tr>
<tr>
<td></td>
<td>forced INV sent to CPU no matter what the other</td>
</tr>
<tr>
<td></td>
<td>snoop cycle is read or write to memory.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Dynamic Write Back enable</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>This feature is used to optimize DRAM buffer</td>
</tr>
<tr>
<td></td>
<td>usage. When CPU issues a write cycle and hits</td>
</tr>
<tr>
<td></td>
<td>to the L2 Cache, the data will write to L2 cache</td>
</tr>
<tr>
<td></td>
<td>and also the DRAM Posted Write Buffer if the</td>
</tr>
<tr>
<td></td>
<td>feature is enabled and the buffer is not full.</td>
</tr>
<tr>
<td></td>
<td>It can keep L2 cache clean to speed up later L2</td>
</tr>
<tr>
<td></td>
<td>cache accesses. If this feature is disabled, the</td>
</tr>
<tr>
<td></td>
<td>CPU hit L2 Cache write cycle will directly write</td>
</tr>
<tr>
<td></td>
<td>to L2 Cache and make the hit line as dirty in L2</td>
</tr>
<tr>
<td></td>
<td>Tag.</td>
</tr>
<tr>
<td>5-4(00)</td>
<td>DRAM Read Pipe Mode</td>
</tr>
<tr>
<td></td>
<td>00 : disable</td>
</tr>
<tr>
<td></td>
<td>01 : NA slow timing</td>
</tr>
<tr>
<td></td>
<td>10 : NA assert Middle timing</td>
</tr>
<tr>
<td></td>
<td>11 : NA assert Fast timing</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable the assertion of NAJ</td>
</tr>
<tr>
<td></td>
<td>when the cycle is a DRAM access cycle. When this</td>
</tr>
<tr>
<td></td>
<td>bit is disabled, the M1541 will not assert NAJ</td>
</tr>
<tr>
<td></td>
<td>during DRAM access. When set to ‘11’, NAJ will</td>
</tr>
<tr>
<td></td>
<td>assert when internal host interface send the read</td>
</tr>
<tr>
<td></td>
<td>control signal to DRAM controller. When set to</td>
</tr>
<tr>
<td></td>
<td>‘10’, NAJ will assert when DRAM controller</td>
</tr>
<tr>
<td></td>
<td>receives the read control signal. When set to</td>
</tr>
<tr>
<td></td>
<td>‘01’, NAJ will assert when DRAM controller reads</td>
</tr>
<tr>
<td></td>
<td>the data from DRAM.</td>
</tr>
<tr>
<td>3(0)</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>0 is recommended for normal operation.</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>2(0)</td>
<td>Single Write Pipe enable</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>This feature is used to optimize pipeline performance. When CPU issues a single write cycle and NAJ will assert to CPU. The assert will be at T2 when bit1 is set to 1.</td>
</tr>
<tr>
<td>1(0)</td>
<td>Fast NAJ asserted in single write cycle</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>This bit controls the NAJ assertion point during CPU single write cycle. When enabled, NAJ will assert at T2 to achieve the best CPU single write performance. If set to disable, then NAJ will not send to CPU.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>L2 Pipeline Function Option</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable the assertion of NAJ when the cycle is an L2 access cycle. When this bit is disabled, the M1541 will not assert NAJ during L2 access.</td>
</tr>
</tbody>
</table>
Register Index: 44h
Register Name: FPM/EDO DRAM Timing Configuration - 1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>EDO/FPM DRAM to CAS Delay: Trcd</td>
</tr>
<tr>
<td></td>
<td>ROW Address Hold Time: Trow</td>
</tr>
<tr>
<td></td>
<td>1st COL Address Setup Time: Tcol</td>
</tr>
<tr>
<td></td>
<td>Trcd=Trow+Tcol</td>
</tr>
<tr>
<td></td>
<td>Trcd  Trow  Tcol</td>
</tr>
<tr>
<td>00:</td>
<td>5T   2T   3T</td>
</tr>
<tr>
<td>01:</td>
<td>4T   2T   2T</td>
</tr>
<tr>
<td>10:</td>
<td>3T   1T   2T</td>
</tr>
<tr>
<td>11:</td>
<td>2T   1T   1T</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>FPM/EDO DRAM Write Timing</td>
</tr>
<tr>
<td>00:</td>
<td>X-5-5-5</td>
</tr>
<tr>
<td>01:</td>
<td>X-4-4-4</td>
</tr>
<tr>
<td>10:</td>
<td>X-3-3-3</td>
</tr>
<tr>
<td>11:</td>
<td>X-2-2-2</td>
</tr>
</tbody>
</table>

This bit is used to control the FPM/EDO DRAM write timing. Please refer to lead off table in Section 3.5.3 for the X value.

| 3-2 (00)   | EDO DRAM Read Timing                                                        |
| 00:        | X-5-5-5                                                                     |
| 01:        | X-4-4-4                                                                     |
| 10:        | X-3-3-3                                                                     |
| 11:        | X-2-2-2                                                                     |

This bit is used to control the EDO DRAM read timing. Please refer to lead off table in Section 3.5.3 for the X value.
<table>
<thead>
<tr>
<th>1-0 (00)</th>
<th>Fast Page Mode DRAM Read Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>00: X-6-6-6</td>
<td></td>
</tr>
<tr>
<td>01: X-5-5-5</td>
<td></td>
</tr>
<tr>
<td>10: X-4-4-4</td>
<td></td>
</tr>
<tr>
<td>11: X-3-3-3</td>
<td></td>
</tr>
</tbody>
</table>

This bit is used to control the Fast Page Mode DRAM Read timing. Please refer to lead off table in Section 3.5.3 for the X value.
Register Index: 45h
Register Name: FPM/EDO DRAM Timing Configuration -2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>EDO/FPM Cycle Time</td>
</tr>
<tr>
<td></td>
<td>00: 13T</td>
</tr>
<tr>
<td></td>
<td>01: 11T</td>
</tr>
<tr>
<td></td>
<td>10: 10T</td>
</tr>
<tr>
<td></td>
<td>11: 9T</td>
</tr>
<tr>
<td></td>
<td>These two bits control the minimum duration of the consecutive RASJ in row miss and refresh cycle.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>EDO/FPM RAS Pulse Width</td>
</tr>
<tr>
<td></td>
<td>00: 7T</td>
</tr>
<tr>
<td></td>
<td>01: 6T</td>
</tr>
<tr>
<td></td>
<td>10: 5T</td>
</tr>
<tr>
<td></td>
<td>11: 4T</td>
</tr>
<tr>
<td></td>
<td>These two bits control the minimum duration of every RASJ active time.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>EDO/FPM Command to command Interval</td>
</tr>
<tr>
<td></td>
<td>0: 3T</td>
</tr>
<tr>
<td></td>
<td>1: 2T</td>
</tr>
<tr>
<td></td>
<td>This bit controls the duration of the consecutive command in page hit cycle.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>EDO/FPM CAS Pre-charge Time</td>
</tr>
<tr>
<td></td>
<td>0: 2T</td>
</tr>
<tr>
<td></td>
<td>1: 1T</td>
</tr>
<tr>
<td></td>
<td>This bit controls the CASJ pre-charge high time.</td>
</tr>
<tr>
<td>1-0 (00)</td>
<td>EDO/FPM RAS Pre-charge Time</td>
</tr>
<tr>
<td></td>
<td>00: 6T</td>
</tr>
<tr>
<td></td>
<td>01: 5T</td>
</tr>
<tr>
<td></td>
<td>10: 4T</td>
</tr>
<tr>
<td></td>
<td>11: 3T</td>
</tr>
<tr>
<td></td>
<td>These two bits control the RASJ pre-charge high time in row miss and refresh cycle.</td>
</tr>
</tbody>
</table>
Register Index : 46h
Register Name : FPM/EDO DRAM Timing Configuration-3
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Fast Back-to-Back</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to enable, the EDO performance is X-2-2-2-2-2-2-2 when index 44h bit[3-2] (EDO DRAM read timing) is set to ‘11’. There is no additional turnaround cycle between two cascade pipeline cycles.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>EDO Detect Mode</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>For the EDO detection procedure, please refer to the DRAM type detection figure in the Hardware and Software programming section.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>EDO Detection Timer</td>
</tr>
<tr>
<td></td>
<td>00 : 128 to 256 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>01 : 256 to 512 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>10 : 512 to 1024 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>11 : 1024 to 2048 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>These two bits combined with bit 6 (EDO Detection Mode) are used to do the EDO detection. When bit 6=1, M1541 will latch DRAM data after the EDO detect timer timeout. If the DRAM is EDO then the data will be correct. If it is FPM DRAM, the latch data is error.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
Register Index: 47h
Register Name: FPM/EDO DRAM Timing Configuration-4
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3 (00h)</td>
<td>Reserved</td>
</tr>
<tr>
<td>2 (0)</td>
<td>FPM/EDO Bank Miss Insert 1 wait</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, FPM/EDO RASJ active will delay 1T to increase MA to RASJ Setup time for row miss cycle.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>FPM/EDO Enhanced Page Mode</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, all of the FPM/EDO pages will be closed after N memory clocks of idle cycle on DRAM bus. The N is defined at index 5h bit[7-6].</td>
</tr>
<tr>
<td>0 (0)</td>
<td>FPM/EDO Bank Miss Detection</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, the FPM/EDO RASJ pre-charge cycle will be skipped and M1541 will assert RASJ active directly at ROW miss cycle.</td>
</tr>
</tbody>
</table>
Register Index : 48h
Register Name : SDRAM Configuration-1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (00)</td>
<td>SDRAM operation mode selection</td>
</tr>
<tr>
<td></td>
<td>000 : normal operation</td>
</tr>
<tr>
<td></td>
<td>001 : NOP(no operation) command enable</td>
</tr>
<tr>
<td></td>
<td>010 : PALL(pre-charge all banks) command enable</td>
</tr>
<tr>
<td></td>
<td>011 : MRS(mode register set) command enable</td>
</tr>
<tr>
<td></td>
<td>100 : CBR(CAS before RAS refresh) enable</td>
</tr>
<tr>
<td></td>
<td>111 : Auto Initialization : only 1 MDR with HA = Mode is needed</td>
</tr>
<tr>
<td>others :</td>
<td>reserved</td>
</tr>
</tbody>
</table>

Note:
(1) Before switching from one mode of SDRAM to another mode, the BIOS should ensure the DRAM buffer is empty. For example, by issuing a DRAM read cycle to flush the DRAM buffer.
(2) In the MRS mode, the MA is translated as the column address and the BIOS should issue the appropriate CPU addresses to program the SDRAMs.
(3) NOP mode is used to force all CPU cycles to DRAM to generate an SDRAM NOP command on the memory interface.
(4) PALL mode is used to force all CPU cycles to DRAM to generate an SDRAM pre-charge all banks command on the memory interface.
(5) MRS command is used to convert all CPU cycles to commands on the memory interface.
(6) MA[11:0] lines are used to drive command:
   MA[2:0] = '010’ for burst of 4 mode.
   MA[4]    = '1/0’ for the value of CAS Latency (3 HCLKINs / 2 HCLKINs).

All these modes are used to initialize SDRAM. Please refer to the hardware and software setup section.
### 4 (0) SDRAM CAS Latency

<table>
<thead>
<tr>
<th>CL</th>
<th>Trcd</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3T</td>
</tr>
<tr>
<td>1</td>
<td>2T</td>
</tr>
</tbody>
</table>

This bit is used to control read data valid wait states after read command has been issued. '0' means the CAS Latency is 3 HCLKINs, and 1 means the CAS Latency is 2 HCLKINs.

Trcd is defined as the delay time from the “active” command to the “read/write” command.

### 3-2 (00) SDRAM RASJ pre-charge time

| 00 | 5T |
| 01 | 4T |
| 10 | 3T |
| 11 | 2T |

These two bits are used to control the period from the “pre-charge” command to the “active” command.

### 1-0 (00) SDRAM RASJ cycle time and SDRAM RASJ low pulse duration setting

<table>
<thead>
<tr>
<th>Trc</th>
<th>Tras</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>10T</td>
</tr>
<tr>
<td>01</td>
<td>9T</td>
</tr>
<tr>
<td>10</td>
<td>8T</td>
</tr>
<tr>
<td>11</td>
<td>7T</td>
</tr>
</tbody>
</table>

The Trc defines the period from the “refresh/active” command to the “active” command. The Tras defines the period from the “active” command to the “pre-charge” command.
Register Index:  49h
Register Name:  SDRAM Configuration-2
Default Value:  00h
Attribute:  Read/Write
Size:  8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0) | JEDEC “2n rule” restricted
  0 : yes
  1 : no (the interval between two commands are not limited to be even-numbered)
  This bit is used to support TI 2n rule SDRAM, the interval between two commands has to be limited to even-numbers. |
| 6 (0) | SDRAM REFRESH cycle Pre-charge all internal banks
  0 : Disable
  1 : Enable
  If this bit is enable, the “pre-charge All Banks” command after the “CAS-before-RAS refresh” command will be eliminated. |
| 5 (0) | SDRAM Pre-charge ALL command Insert 1 wait
  0 : Disable
  1 : Enable
  If this bit is enable, the “pre-charge all banks”, “pre-charge selected banks” and “row active” commands will delay 1T to increase control signal setup time when index 49h bit2 =1 (SDRAM bank miss detection Enable). |
| 4 (0) | SDRAM Command Insert 1 wait
  0 : Disable
  1 : Enable
  If this bit is enable, all the SDRAM commands will delay 1T to increase MA, SRASJ, SCASJ, MWEJ control signal setup time. |
| 3 (0) | SDRAM Enhanced Page Mode
  0 : Disable
  1 : Enable
  If this bit is enable, all SDRAM internal banks are closed after ‘N’ memory clocks of DRAM idle cycle. The ‘N’ is defined at index 5Fh bit[7-6] (Enhanced Page Mode counter). |
<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
</table>
| 2 (0) | SDRAM Bank Miss Detection             | 0 : Disable  
1 : Enable  
If this bit is enable, all SDRAM internal banks are closed in page miss cycle. Under this condition, the “active” command is asserted instead of “precharge” command to enhance the row miss performance when row miss happens. |
| 1 (0) | SDRAM Internal Page Detection         | 0 : Disable  
1 : Enable  
If this bit is enable, M1541 will keep multi-internal banks opened. Such that the possibility of page hit cycle is maximized and improve the row/bank switch performance. |
| 0 (0) | SDRAM Pipe Function                   | 0 : Disable  
1 : Enable  
If this bit is enable, M1541 will optimize the sequence and operate two consequent cycles.  
If this bit is disable, the next command will begin after the previous data output of the current command. |
Register Index: 4Ah
Register Name: DRAM Controller Configuration
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>Write Buffer Threshold</td>
</tr>
<tr>
<td></td>
<td>00: 2 LINEs</td>
</tr>
<tr>
<td></td>
<td>01: 4 LINEs</td>
</tr>
<tr>
<td></td>
<td>10: 6 LINEs</td>
</tr>
<tr>
<td></td>
<td>11: 8 LINEs</td>
</tr>
<tr>
<td></td>
<td>These two bits set the DRAM write buffer threshold. Whenever the content of DRAM write buffer over its threshold and index 4Ah bit5=1 (Write buffer threshold detect enable), the DRAM sequence will treat the DRAM write buffer as the highest priority and grant its arbitration to the DRAM write buffer to avoid the DRAM write buffer full.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Write Buffer Threshold Detect</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the DRAM sequence to grant its arbitration to DRAM posted write buffer. Whenever the number of the data reside in the DRAM posted write buffer is greater than the threshold set at index 4Ah bit[7-6] (Write buffer threshold). We recommend to enable this bit at normal operation.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Mixed DRAM Command Interval</td>
</tr>
<tr>
<td></td>
<td>bit 4 FPM/EDO to SDRAM SDRAM to FPM/EDO</td>
</tr>
<tr>
<td></td>
<td>0 4 6</td>
</tr>
<tr>
<td></td>
<td>1 3 5</td>
</tr>
<tr>
<td></td>
<td>This bit is used to prevent the errors when both FPM/EDO and SDRAM at the DRAM bus different banks at the same time. This bit will decide the interval required to exchange the RASJ, CASJ and MWEJ control signal between accessing different types of DRAM composed of FPM/EDO and SDRAM.</td>
</tr>
<tr>
<td>Bit</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-------------</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Supports two DIMMs only</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to Enable, the M1541 only supports 2 DIMMs SDRAM. The RASJ[7-4] become copy of the RASJ[3-0]. This configuration is designed to share the RASJ loading on two DIMMs layout.</td>
</tr>
<tr>
<td>1</td>
<td>Fast Next Mode</td>
</tr>
<tr>
<td></td>
<td>If this bit is disabled, DRAM controller will respond the command immediately. If this bit is enabled, DRAM controller will respond the command sent to DRAM at the next cycle.</td>
</tr>
<tr>
<td>2,0 (0)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register Index : 4Bh
Register Name : DRAM Sequencing Configuration
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>DRAM Sequencing Parking Select</td>
</tr>
<tr>
<td>0 : CPU</td>
<td>1 : AGP</td>
</tr>
<tr>
<td></td>
<td>This bit decides when there are no request from CPU and AGP, the DRAM sequencing will park the grant to CPU or AGP.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>AGP HPR Dominate Arbitration Mode.</td>
</tr>
<tr>
<td>0 : Disable</td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, DRAM sequencing will distinguish the priority of AGP read request. High-Priority-Read Request of AGP read command will be treated as highest priority then CPU. The second priority is the Low-Priority-Read Request. If disabled, all AGP High-Priority-Read and Low-Priority-Read Requests will be treated as the same.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>Arbitration Mode</td>
</tr>
<tr>
<td>00 : AGP → CPU → PCI → WBF</td>
<td></td>
</tr>
<tr>
<td>01 : CPU → AGP → PCI → WBF</td>
<td></td>
</tr>
<tr>
<td>10 : CPU → PCI → AGP → WBF</td>
<td></td>
</tr>
<tr>
<td>11 : AGP → CPU → PCI → WBF Round Robins</td>
<td></td>
</tr>
<tr>
<td>These two bits control the arbitration priority of the DRAM sequencer. A DRAM master with higher priority always gets faster service whenever it issues DRAM requests.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Snoop first</td>
</tr>
<tr>
<td>0 : Disable</td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>After this bit has been enabled, the DRAM sequencer will grant its arbitration to the host whenever a snoop cycle is pending and the host is requesting the usage of the DRAM. The DRAM sequencer will treat the Snoop cycle to be the first priority.</td>
</tr>
<tr>
<td></td>
<td>DRAM Sequencing Bypass Mode.</td>
</tr>
<tr>
<td>---</td>
<td>--------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
</tr>
</tbody>
</table>

When enabled, the DRAM sequencer will bypass the host request to the DRAM controller as soon as possible. Otherwise, all commands issued to the DRAM controller will be synchronized by the internal clock.

<table>
<thead>
<tr>
<th></th>
<th>GART Table check point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>T2</td>
</tr>
<tr>
<td>1</td>
<td>T3</td>
</tr>
</tbody>
</table>

This bit controls the GART hit/miss checkpoint timing. The cycle begins from the issued request command.

<table>
<thead>
<tr>
<th></th>
<th>Supports DRAM Posted Write Buffer Read-Around-Write Cycle.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Enable</td>
</tr>
<tr>
<td>1</td>
<td>Disable</td>
</tr>
</tbody>
</table>

This bit is used to control buffer for back-to-back CPU write and read cycles. Since the M1541 implements the DRAM write buffer to post CPU write cycles, the M1541 will do the read first and then flush the DRAM write buffer if this feature is enabled and the required data of the read cycle do not reside in the buffer. When this bit is disabled, the M1541 will flush the DRAM write buffer data first, and then do the CPU read cycle. A ‘0’ is recommended for normal operation.
Register Index : 4Ch  
Register Name : DRAM Master latency-1  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>DRAM Write Buffer (DMWBF) Latency. These bits set the DRAM write buffer to DRAM request latency. When the request time is out of the latency, DMWBF will become a higher priority request.</td>
</tr>
<tr>
<td>0000</td>
<td>0 clock</td>
</tr>
<tr>
<td>0001</td>
<td>4 clocks</td>
</tr>
<tr>
<td>0010</td>
<td>8 clocks</td>
</tr>
<tr>
<td>0011</td>
<td>12 clocks</td>
</tr>
<tr>
<td>0100</td>
<td>16 clocks</td>
</tr>
<tr>
<td>0101</td>
<td>20 clocks</td>
</tr>
<tr>
<td>0110</td>
<td>24 clocks</td>
</tr>
<tr>
<td>0111</td>
<td>28 clocks</td>
</tr>
<tr>
<td>1000</td>
<td>32 clocks</td>
</tr>
<tr>
<td>1001</td>
<td>36 clocks</td>
</tr>
<tr>
<td>1010</td>
<td>40 clocks</td>
</tr>
<tr>
<td>1011</td>
<td>44 clocks</td>
</tr>
<tr>
<td>1100</td>
<td>48 clocks</td>
</tr>
<tr>
<td>1101</td>
<td>52 clocks</td>
</tr>
<tr>
<td>1110</td>
<td>56 clocks</td>
</tr>
<tr>
<td>1111</td>
<td>60 clocks</td>
</tr>
</tbody>
</table>
### 3-0 (0h) Host Latency

These bits set the Host to DRAM request latency. When the request time is out of the latency, Host will become a higher priority request.

<table>
<thead>
<tr>
<th>Value</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0 clock</td>
</tr>
<tr>
<td>0001</td>
<td>4 clocks</td>
</tr>
<tr>
<td>0010</td>
<td>8 clocks</td>
</tr>
<tr>
<td>0011</td>
<td>12 clocks</td>
</tr>
<tr>
<td>0100</td>
<td>16 clocks</td>
</tr>
<tr>
<td>0101</td>
<td>20 clocks</td>
</tr>
<tr>
<td>0110</td>
<td>24 clocks</td>
</tr>
<tr>
<td>0111</td>
<td>28 clocks</td>
</tr>
<tr>
<td>1000</td>
<td>32 clocks</td>
</tr>
<tr>
<td>1001</td>
<td>36 clocks</td>
</tr>
<tr>
<td>1010</td>
<td>40 clocks</td>
</tr>
<tr>
<td>1011</td>
<td>44 clocks</td>
</tr>
<tr>
<td>1100</td>
<td>48 clocks</td>
</tr>
<tr>
<td>1101</td>
<td>52 clocks</td>
</tr>
<tr>
<td>1110</td>
<td>56 clocks</td>
</tr>
<tr>
<td>1111</td>
<td>60 clocks</td>
</tr>
</tbody>
</table>
Register Index : 4Dh
Register Name : DRAM Master Latency-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>AGP Latency. These bits set the AGP to DRAM request latency. When the request time is out of the latency, AGP will become a higher priority request.</td>
</tr>
<tr>
<td>0000</td>
<td>0 clock</td>
</tr>
<tr>
<td>0001</td>
<td>4 clocks</td>
</tr>
<tr>
<td>0010</td>
<td>8 clocks</td>
</tr>
<tr>
<td>0011</td>
<td>12 clocks</td>
</tr>
<tr>
<td>0100</td>
<td>16 clocks</td>
</tr>
<tr>
<td>0101</td>
<td>20 clocks</td>
</tr>
<tr>
<td>0110</td>
<td>24 clocks</td>
</tr>
<tr>
<td>0111</td>
<td>28 clocks</td>
</tr>
<tr>
<td>1000</td>
<td>32 clocks</td>
</tr>
<tr>
<td>1001</td>
<td>36 clocks</td>
</tr>
<tr>
<td>1010</td>
<td>40 clocks</td>
</tr>
<tr>
<td>1011</td>
<td>44 clocks</td>
</tr>
<tr>
<td>1100</td>
<td>48 clocks</td>
</tr>
<tr>
<td>1101</td>
<td>52 clocks</td>
</tr>
<tr>
<td>1110</td>
<td>56 clocks</td>
</tr>
<tr>
<td>1111</td>
<td>60 clocks</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>PCI Latency. These bits set the PCI DRAM request latency. When the request time is out of the latency, PCI will become a higher priority request.</td>
</tr>
<tr>
<td>---------</td>
<td>------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0000</td>
<td>0 clock</td>
</tr>
<tr>
<td>0001</td>
<td>4 clocks</td>
</tr>
<tr>
<td>0010</td>
<td>8 clocks</td>
</tr>
<tr>
<td>0011</td>
<td>12 clocks</td>
</tr>
<tr>
<td>0100</td>
<td>16 clocks</td>
</tr>
<tr>
<td>0101</td>
<td>20 clocks</td>
</tr>
<tr>
<td>0110</td>
<td>24 clocks</td>
</tr>
<tr>
<td>0111</td>
<td>28 clocks</td>
</tr>
<tr>
<td>1000</td>
<td>32 clocks</td>
</tr>
<tr>
<td>1001</td>
<td>36 clocks</td>
</tr>
<tr>
<td>1010</td>
<td>40 clocks</td>
</tr>
<tr>
<td>1011</td>
<td>44 clocks</td>
</tr>
<tr>
<td>1100</td>
<td>48 clocks</td>
</tr>
<tr>
<td>1101</td>
<td>52 clocks</td>
</tr>
<tr>
<td>1110</td>
<td>56 clocks</td>
</tr>
<tr>
<td>1111</td>
<td>60 clocks</td>
</tr>
</tbody>
</table>
Register Index: 4Eh
Register Name: DRAM Master Slice-1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>DMWBFS Slice. These bits set the DRAM write buffer to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted.</td>
</tr>
<tr>
<td>0000</td>
<td>1 command</td>
</tr>
<tr>
<td>0001</td>
<td>2 commands</td>
</tr>
<tr>
<td>0010</td>
<td>3 commands</td>
</tr>
<tr>
<td>0011</td>
<td>4 commands</td>
</tr>
<tr>
<td>0100</td>
<td>5 commands</td>
</tr>
<tr>
<td>0101</td>
<td>6 commands</td>
</tr>
<tr>
<td>0110</td>
<td>7 commands</td>
</tr>
<tr>
<td>0111</td>
<td>8 commands</td>
</tr>
<tr>
<td>1000</td>
<td>9 commands</td>
</tr>
<tr>
<td>1001</td>
<td>10 commands</td>
</tr>
<tr>
<td>1010</td>
<td>11 commands</td>
</tr>
<tr>
<td>1011</td>
<td>12 commands</td>
</tr>
<tr>
<td>1100</td>
<td>13 commands</td>
</tr>
<tr>
<td>1101</td>
<td>14 commands</td>
</tr>
<tr>
<td>1110</td>
<td>15 commands</td>
</tr>
<tr>
<td>1111</td>
<td>16 commands</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>Host Slice. These bits set the Host to DRAM access slice. After a DRAM request has</td>
</tr>
<tr>
<td></td>
<td>been granted, the DRAM sequencer will not change its arbitration until the number of</td>
</tr>
<tr>
<td></td>
<td>access is greater than the slice or the request has been de-asserted.</td>
</tr>
<tr>
<td>0000</td>
<td>1 command</td>
</tr>
<tr>
<td>0001</td>
<td>2 commands</td>
</tr>
<tr>
<td>0010</td>
<td>3 commands</td>
</tr>
<tr>
<td>0011</td>
<td>4 commands</td>
</tr>
<tr>
<td>0100</td>
<td>5 commands</td>
</tr>
<tr>
<td>0101</td>
<td>6 commands</td>
</tr>
<tr>
<td>0110</td>
<td>7 commands</td>
</tr>
<tr>
<td>0111</td>
<td>8 commands</td>
</tr>
<tr>
<td>1000</td>
<td>9 commands</td>
</tr>
<tr>
<td>1001</td>
<td>10 commands</td>
</tr>
<tr>
<td>1010</td>
<td>11 commands</td>
</tr>
<tr>
<td>1011</td>
<td>12 commands</td>
</tr>
<tr>
<td>1100</td>
<td>13 commands</td>
</tr>
<tr>
<td>1101</td>
<td>14 commands</td>
</tr>
<tr>
<td>1110</td>
<td>15 commands</td>
</tr>
<tr>
<td>1111</td>
<td>16 commands</td>
</tr>
</tbody>
</table>
Register Index : 4Fh
Register Name : DRAM Master Slice-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>AGP Slice. These bits set the AGP to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted.</td>
</tr>
<tr>
<td>0000</td>
<td>1 command</td>
</tr>
<tr>
<td>0001</td>
<td>2 commands</td>
</tr>
<tr>
<td>0010</td>
<td>3 commands</td>
</tr>
<tr>
<td>0011</td>
<td>4 commands</td>
</tr>
<tr>
<td>0100</td>
<td>5 commands</td>
</tr>
<tr>
<td>0101</td>
<td>6 commands</td>
</tr>
<tr>
<td>0110</td>
<td>7 commands</td>
</tr>
<tr>
<td>0111</td>
<td>8 commands</td>
</tr>
<tr>
<td>1000</td>
<td>9 commands</td>
</tr>
<tr>
<td>1001</td>
<td>10 commands</td>
</tr>
<tr>
<td>1010</td>
<td>11 commands</td>
</tr>
<tr>
<td>1011</td>
<td>12 commands</td>
</tr>
<tr>
<td>1100</td>
<td>13 commands</td>
</tr>
<tr>
<td>1101</td>
<td>14 commands</td>
</tr>
<tr>
<td>1110</td>
<td>15 commands</td>
</tr>
<tr>
<td>1111</td>
<td>16 commands</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>PCI Slice. These bits set the PCI to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted.</td>
</tr>
<tr>
<td>---------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0000</td>
<td>1 command</td>
</tr>
<tr>
<td>0001</td>
<td>2 commands</td>
</tr>
<tr>
<td>0010</td>
<td>3 commands</td>
</tr>
<tr>
<td>0011</td>
<td>4 commands</td>
</tr>
<tr>
<td>0100</td>
<td>5 commands</td>
</tr>
<tr>
<td>0101</td>
<td>6 commands</td>
</tr>
<tr>
<td>0110</td>
<td>7 commands</td>
</tr>
<tr>
<td>0111</td>
<td>8 commands</td>
</tr>
<tr>
<td>1000</td>
<td>9 commands</td>
</tr>
<tr>
<td>1001</td>
<td>10 commands</td>
</tr>
<tr>
<td>1010</td>
<td>11 commands</td>
</tr>
<tr>
<td>1011</td>
<td>12 commands</td>
</tr>
<tr>
<td>1100</td>
<td>13 commands</td>
</tr>
<tr>
<td>1101</td>
<td>14 commands</td>
</tr>
<tr>
<td>1110</td>
<td>15 commands</td>
</tr>
<tr>
<td>1111</td>
<td>16 commands</td>
</tr>
</tbody>
</table>
Register Index: **50h**  
Register Name: **ECCP - ECC/Parity Feature**  
Default Value: **00h**  
Attribute: **Read/Write**  
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
| 6 (0)      | SERRJ Duration.  
            | 0: SERRJ will be asserted for 1 PCI Clock.  
            | 1: SERRJ will be asserted until all the ECC(parity) Error Flags are cleared.  
            | When the M1541 detects an ECC or parity error, the M1541 will assert SERRJ for 1 PCI Clock (pulse mode) if this bit is set to '0'. Otherwise, the M1541 will assert the SERRJ to report the memory error until all the ECC/parity error flags are cleared (level mode).  
            | This bit is used to control the assertion time of SERRJ. |
| 5 (0)      | SERRJ on Parity or Multiple-bit ECC Error.  
            | 0: Disable  
            | 1: Enable.  
            | When this bit is set to '0', the M1541 will not assert the SERRJ signal when the memory parity or multiple-bit error occurs. Disabling this bit will disable the DRAM parity error check or DRAM ECC multiple-bit error check. Otherwise, the memory data error will be reported to the system via SERRJ assertion to generate NMI (Non-Maskable Interrupt). |
| 4 (0)      | SERRJ on Single-bit ECC Error.  
            | 0: Disable.  
            | 1: Enable.  
            | When this bit is set to '0', the M1541 will not assert SERRJ on single-bit DRAM ECC errors. Disabling this bit will disable the DRAM ECC single-bit error check. Otherwise, the M1541 will assert SERRJ to generate NMI (Non-Maskable Interrupt) when it detects a single-bit DRAM ECC error. |
| 3-1 (000)  | Reserved.    |
| 0 (0)      | DRAM Data Integrity Mode.  
            | 0: Parity.  
            | 1: ECC. |
When this bit is set to '0', the DRAM data integrity will be implemented by the parity algorithm. Otherwise, the ECC data integrity will be implemented.
Register Index : 51h
Register Name : ECCE - ECC or Parity Error Status
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (0h)</td>
<td>ECC Multiple-bit or Parity First Row error. These 3 bits record the first row associated with the ECC multiple-bit or parity error. When an error is detected, these bits are updated and ECCE[4] (this index bit[4]) is set.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>ECC Multiple-bit Error or Parity Error Flag. The M1541 sets this bit to ‘1’ when either an ECC multiple-bit error or parity error has been detected, depending on whether ECC or parity feature is enabled, respectively. A write of ‘1’ by software to ECCE[4] will clear this bit and write of ‘0’ has no effect on it.</td>
</tr>
<tr>
<td>3-1 (0h)</td>
<td>ECC Single-bit First Row Error. These 3 bits record the first row associated with the ECC single-bit error. When an error is detected, these bits are updated and ECCE[0] is set.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>ECC Single-bit Error Flag. The M1541 sets this bit to ‘1’ when an ECC single-bit error has been detected and the ECC function is enabled. A write of ‘1’ by software to ECCE[0] will clear this bit and write of ‘0’ has no effect on it.</td>
</tr>
</tbody>
</table>

Register Index : 52h
Register Name : Reserved
Default Value : 00h
Attribute : Read/Write
Size : 8 bits
Register Index : 53h
Register Name : DRAM Posted Write Buffer Control
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>CPU IDLE SEL TIMER</td>
</tr>
<tr>
<td></td>
<td>00 : 2 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>01 : 4 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>10 : 6 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>11 : 8 CPU CLKs</td>
</tr>
<tr>
<td></td>
<td>The CPU idle select timer is used to control the clock that keep internal host clock running when gated clock is enable.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>CPU to DRAM Posted Write Buffer Concurrent with PCI-to-DRAM Write</td>
</tr>
<tr>
<td></td>
<td>0 : Enable</td>
</tr>
<tr>
<td></td>
<td>1 : Disable</td>
</tr>
<tr>
<td></td>
<td>If disabled, the CPU to DRAM posted write buffer cycle will not be concurrent with PCI-to-DRAM write cycle.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>CPU-to-DRAM Posted Write Buffer Concurrent with PCI-to-DRAM Read.</td>
</tr>
<tr>
<td></td>
<td>0 : Enable</td>
</tr>
<tr>
<td></td>
<td>1 : Disable</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to disable, the CPU to DRAM posted write buffer cycle will not be concurrent with PCI-to-DRAM read cycle.</td>
</tr>
<tr>
<td>3-1 (00)</td>
<td>DRAM Posted Write Buffer Idle Flush Timer</td>
</tr>
<tr>
<td></td>
<td>000 : 4 clocks</td>
</tr>
<tr>
<td></td>
<td>001 : 8 clocks</td>
</tr>
<tr>
<td></td>
<td>010 : 12 clocks</td>
</tr>
<tr>
<td></td>
<td>110 : 16 clocks</td>
</tr>
<tr>
<td></td>
<td>111 : 32 clocks</td>
</tr>
<tr>
<td></td>
<td>Other : reserved</td>
</tr>
<tr>
<td></td>
<td>These three bits control the IDLE flush timer of DRAM post write buffer when index 53h bit0 is set to enable.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>DRAM Posted Write Buffer Idle Flush</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------</td>
</tr>
<tr>
<td>0 : Enable</td>
<td></td>
</tr>
<tr>
<td>1 : Disable</td>
<td></td>
</tr>
</tbody>
</table>

This option enables the idle timer for each line of DRAM posted write buffer. By enabling this option, M1541 will keep data in DRAM posted write buffer until that idle timer timeout then flush the data. Otherwise, the posted write data will be always flushed without any latency time.
Register Index: 54h  
Register Name: Memory Hole  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
| 5 (0)      | 14-15M Memory Location.  
            | 0 : Local Memory Area.  
            | 1 : Non-Local Memory Area.  
            | When this bit is set to ‘1’, all memory access address from 14M to 15M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 15M. Otherwise, it will be decoded as non-local memory and pass through to PCI bus. |
| 4 (0)      | 15-16M Memory's Location.  
            | 0 : Local Memory Area.  
            | 1 : Non-Local Memory Area.  
            | When this bit is set to ‘1’, all memory access address from 15M to 16M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 16M. Otherwise, it will be decoded as non-local memory and pass through to PCI bus. |
| 3 (0)      | Page A-B as Local Memory Area.  
            | 0 : Non-local Memory Area.  
            | 1 : Local Memory Area.  
            | When this bit is set to ‘1’, all memory access address from A0000h to BFFFFh will be decoded as local memory cycle and access local DRAM. Otherwise, it will be decoded as non-local memory and pass through to PCI bus. |
| 2 (0)      | Force Address Region 80000h-9FFFFh as Non-local Memory Area.  
            | 0 : Local Memory Area.  
            | 1 : Non-local Memory Area.  
            | When this bit is set to ‘1’, all memory access address from 80000h to 9FFFFh will be decoded as non-local cycle and pass through PCI bus. Otherwise, it will be decoded as local memory and access to DRAM. |
| 1-0 (00)   | Reserved.    |
Register Index : 55h
Register Name : SMRM - SMRAM Mapping
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (0h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>SMM Page -A or -B Region Code/Data Split.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td><strong>Note</strong>: This bit is valid only if this register bit [3:2]=&quot;01&quot;. When this bit is enabled, only the cycle command with DCJ='0' can access SMRAM. The CPU data access will pass through PCI bus.</td>
</tr>
<tr>
<td>3-2 (00)</td>
<td>SMRAM Region.</td>
</tr>
<tr>
<td></td>
<td>00: SMM Region at D000 Segment will be re-mapped to B000 Segment.</td>
</tr>
<tr>
<td></td>
<td>01: SMM Region at A000 or B000 Segment.</td>
</tr>
<tr>
<td></td>
<td>10: SMM Region at 3000 Segment will be re-mapped to B000 Segment.</td>
</tr>
<tr>
<td></td>
<td>11 : Reserved.</td>
</tr>
<tr>
<td></td>
<td><strong>Please refer to the following table.</strong></td>
</tr>
<tr>
<td>1 (0)</td>
<td>SMRAM Access Control.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td><strong>When this bit is disabled, SMRAM can only be accessed during SMI handler. Otherwise, SMRAM area can be accessed any time. This bit is used in SMRAM initialization and must be set to '0' when the initialization process is finished.</strong></td>
</tr>
<tr>
<td>0 (0)</td>
<td>Supports SMRAM Mapping.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td><strong>This bit is used to disable or enable SMRAM Mapping.</strong></td>
</tr>
</tbody>
</table>

**Table 4-3** The following is M1541 address re-mapping table for SMRAM mapping enable.
<table>
<thead>
<tr>
<th>Bit [3-1]</th>
<th>SMIACTJ</th>
<th>CPU Logical Address</th>
<th>Re-mapped Physical Address</th>
<th>Access DRAM Y/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
<td>D0000</td>
<td>B0000</td>
<td>Y</td>
</tr>
<tr>
<td>000</td>
<td>1</td>
<td>D0000</td>
<td>non-local</td>
<td>N</td>
</tr>
<tr>
<td>001</td>
<td>X</td>
<td>D0000</td>
<td>B0000</td>
<td>Y</td>
</tr>
<tr>
<td>010</td>
<td>0</td>
<td>A0000/ B0000</td>
<td>A0000/ B0000</td>
<td>Y</td>
</tr>
<tr>
<td>010</td>
<td>1</td>
<td>A0000/ B0000</td>
<td>non-local</td>
<td>N</td>
</tr>
<tr>
<td>011</td>
<td>X</td>
<td>A0000/ B0000</td>
<td>A0000/ B0000</td>
<td>Y</td>
</tr>
<tr>
<td>100</td>
<td>0</td>
<td>30000</td>
<td>B0000</td>
<td>Y</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
<td>30000</td>
<td>30000</td>
<td>Y</td>
</tr>
<tr>
<td>101</td>
<td>X</td>
<td>30000</td>
<td>B0000</td>
<td>Y</td>
</tr>
</tbody>
</table>
Register Index : 56h
Register Name : SHADRI - SHADOW Regions Read Enable - 1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>DC000h-DFFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region DC000h-DFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>D8000h-DBFFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region D8000h-DBFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>D4000h-D7FFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region D4000h-D7FFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>D0000h-D3FFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region D0000h-D3FFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>CC000h-CFFFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region CC000h-CFFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>Bit Set</td>
<td>Shadow Region Read Enable</td>
</tr>
<tr>
<td>---------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>2 (0)</td>
<td>C8000h-CBFFFh</td>
</tr>
<tr>
<td>1 (0)</td>
<td>C4000h-C7FFFh</td>
</tr>
<tr>
<td>0 (0)</td>
<td>C0000h-C3FFFh</td>
</tr>
</tbody>
</table>
Register Index: **57h**  
Register Name: **SHADRII - SHADOW Regions Read Enable - 2**  
Default Value: **00h**  
Attribute: Read/Write  
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | FC000h-FFFFFh Shadow Region Read Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region FC000h-FFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 6 (0)      | F8000h-FBFFFFh Shadow Region Read Enable.  
0 : Disable  
1 : Enable.  
When this bit is enabled, address region F8000h-FBFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 5 (0)      | F4000h-F7FFFFh Shadow Region Read Enable.  
0 : Disable  
1 : Enable.  
When this bit is enabled, address region F4000h-F7FFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 4 (0)      | F0000h-F3FFFFh Shadow Region Read Enable.  
0 : Disable  
1 : Enable.  
When this bit is enabled, address region F0000h-F3FFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 3 (0)      | EC000h-FFFFFh Shadow Region Read Enable.  
0 : Disable  
1 : Enable.  
When this bit is enabled, address region EC000h-FFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
<table>
<thead>
<tr>
<th></th>
<th>E8000h-EBFFh Shadow Region Read Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0: Disable.</td>
</tr>
<tr>
<td></td>
<td>1: Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address</td>
</tr>
<tr>
<td></td>
<td>region E8000h-EBFFh memory read</td>
</tr>
<tr>
<td></td>
<td>cycle will access local DRAM.</td>
</tr>
<tr>
<td></td>
<td>Otherwise, it will pass through PCI</td>
</tr>
<tr>
<td></td>
<td>bus.</td>
</tr>
<tr>
<td>1</td>
<td>E4000h-E7FFFh Shadow Region Read</td>
</tr>
<tr>
<td></td>
<td>Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address</td>
</tr>
<tr>
<td></td>
<td>region E4000h-E7FFFh memory read</td>
</tr>
<tr>
<td></td>
<td>cycle will access local DRAM.</td>
</tr>
<tr>
<td></td>
<td>Otherwise, it will pass through PCI</td>
</tr>
<tr>
<td></td>
<td>bus.</td>
</tr>
<tr>
<td>0</td>
<td>E0000h-E3FFFh Shadow Region Read</td>
</tr>
<tr>
<td></td>
<td>Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address</td>
</tr>
<tr>
<td></td>
<td>region E0000h-E3FFFh memory read</td>
</tr>
<tr>
<td></td>
<td>cycle will access local DRAM.</td>
</tr>
<tr>
<td></td>
<td>Otherwise, it will pass through PCI</td>
</tr>
<tr>
<td></td>
<td>bus.</td>
</tr>
</tbody>
</table>
Register Index: 58h
Register Name: SHADWI - SHADOW Regions Write Enable - 1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7(0)       | DC000h-DFFFFh Shadow Region Write Enable.  
|            | 0 : Disable.  
|            | 1 : Enable.  
|            | When this bit is enabled, address region DC000h-DFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 6(0)       | D8000h-DBFFFFh Shadow Region Write Enable.  
|            | 0 : Disable.  
|            | 1 : Enable.  
|            | When this bit is enabled, address region D8000h-DBFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 5(0)       | D4000h-D7FFFh Shadow Region Write Enable.  
|            | 0 : Disable.  
|            | 1 : Enable.  
|            | When this bit is enabled, address region D4000h-D7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 4(0)       | D0000h-D3FFFh Shadow Region Write Enable.  
|            | 0 : Disable.  
|            | 1 : Enable.  
|            | When this bit is enabled, address region D0000h-D3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 3(0)       | CC000h-CFFFFh Shadow Region Write Enable.  
|            | 0 : Disable.  
|            | 1 : Enable.  
<p>|            | When this bit is enabled, address region CC000h-CFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |</p>
<table>
<thead>
<tr>
<th>Bit</th>
<th>Region</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 (0)</td>
<td>C8000h-CBFFFh Shadow Region Write Enable.</td>
<td>0 : Disable. 1 : Enable. When this bit is enabled, address region C8000h-CBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>C4000h-C7FFFh Shadow Region Write Enable.</td>
<td>0 : Disable. 1 : Enable. When this bit is enabled, address region C4000h-C7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>C0000h-C3FFFh Shadow Region Write Enable.</td>
<td>0 : Disable. 1 : Enable. When the above bits are enabled, the corresponding memory address region write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
</tbody>
</table>
Register Index: **59h**

Register Name: **SHADWII - SHADOW Regions Write Enable - 2**

Default Value: **00h**

Attribute: **Read/Write**

Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | FC000h-FFFFFh Shadow Region Write Enable.  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled, address region FC000h-FFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 6 (0)      | F8000h-FBFFFh Shadow Region Write Enable.  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled, address region F8000h-FBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 5 (0)      | F4000h-F7FFFh Shadow Region Write Enable.  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled, address region F4000h-F7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 4 (0)      | F0000h-F3FFFh Shadow Region Write Enable.  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled, address region F0000h-F3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 3 (0)      | EC000h-EFFFFh Shadow Region Write Enable.  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled, address region EC000h-EFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 2 (0) | E8000h-EBFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region E8000h-EBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
|---|---|
| 1 (0) | E4000h-E7FFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region E4000h-E7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 0 (0) | E0000h-E3FFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region E0000h-E3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
Register Index: 5Ah
Register Name: SHADC - SHADOW Regions Cacheable Enable - 1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>DC000h-DFFFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[7] = '1', address region DC000h-DFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>D8000h-DFFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[6] = '1', address region D8000h-DFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>D4000h-D7FFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[5] = '1', address region D4000h-D7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>D0000h-D3FFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[4] = '1', address region D0000h-D3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>CC000h-CFFFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[3] = '1', address region CC000h-CFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>Bit</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>2 (0)</td>
<td>C8000h-CBFFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td>0</td>
<td>Disable.</td>
</tr>
<tr>
<td>1</td>
<td>Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[2] = '1', address region C8000h-CBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>C4000h-C7FFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td>0</td>
<td>Disable.</td>
</tr>
<tr>
<td>1</td>
<td>Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[1] = '1', address region C4000h-C7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>C0000h-C3FFFh Shadow Region Cacheable Enable.</td>
</tr>
<tr>
<td>0</td>
<td>Disable.</td>
</tr>
<tr>
<td>1</td>
<td>Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled and SHADRI[0] = '1', address region C0000h-C3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
</tbody>
</table>
Register Index : **5Bh**  
Register Name : **SHADCII - SHADOW Regions Cacheable Enable - 2**  
Default Value : **00h**  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | **FC000h-FFFFFh Shadow Region Cacheable Enable.**  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled and SHADRII[7] = '1', address region FC000h-FFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable. |
| 6 (0)      | **F8000h-FBFFFh Shadow Region Cacheable Enable.**  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled and SHADRII[6] = '1', address region F8000h-FBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable. |
| 5 (0)      | **F4000h-F7FFFh Shadow Region Cacheable Enable.**  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled and SHADRII[5] = '1', address region F4000h-F7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable. |
| 4 (0)      | **F0000h-F3FFFh Shadow Region Cacheable Enable.**  
            | 0 : Disable.  
            | 1 : Enable.  
            | When this bit is enabled and SHADRII[4] = '1', address region F0000h-F3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable. |
| 3 (0)      | **EC000h-EFFFFFh Shadow Region Cacheable Enable.**  
            | 0 : Disable.  
            | 1 : Enable.  
<pre><code>        | When this bit is enabled and SHADRII[3] = '1', address region EC000h-EFFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable. |
</code></pre>
<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Shadow Region Cacheable Enable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 (0)</td>
<td>E8000h-EBFFFh</td>
<td>0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[2] = '1', address region E8000h-EBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>E4000h-E7FFFh</td>
<td>0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[1] = '1', address region E4000h-E7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>E0000h-E3FFFh</td>
<td>0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[0] = '1', address region E0000h-E3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.</td>
</tr>
</tbody>
</table>
Register Index: 5Ch
Register Name: **Reserved Registers**
Default Value: 00h
Attribute: Read/Write

Register Index: 5Dh
Register Name: **DRAM Clock Gated Start Point Control**
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5,3 (0)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 4 (0)      | Ignore DRAM Posted Write Buffer (DMWBF) over threshold when other is latency out  
            | 0 : Disable  
            | 1 : Enable   
            | This bit is used to mask the feature set at index 4Ah bit5. When DRAM write buffer over the 
            | threshold will be ignore if there is any other DRAM request which is out of latency when this bit 
            | is set to ‘1’. -- |
| 2 (0)      | CLKEN gated control enable for notebook power saving  
            | 0 : Disable  
            | 1 : Enable   
            | This bit is used to control the gated clock circuit. When enabling this bit, the SDRAM interface 
            | is idle. The SDRAM CLKEN will insert to reduce the SDRAM power consumption. |
| 1-0 (00)   | DRAM Controller Gated Clock Timer  
            | 00 : 12 CPU CLKS -- Wake up delay 1 wait  
            | 01 : 8 CPU CLKS – Wake up delay 1 wait  
            | 10 : 8 CPU CLKS – Wake immediately  
            | 11 : 4 CPU CLKS – Wake immediately  
            | These two bits control the gated time and wakeup up time of the DRAM sequencer and the 
            | DRAM controller. |
Register Index : 5Eh
Register Name : **DRAM Refresh Control** (00h, R/W)
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>FPM/EDO Refresh Mode</td>
</tr>
<tr>
<td></td>
<td>0 : CAS before RAS Refresh</td>
</tr>
<tr>
<td></td>
<td>1 : RAS only Refresh</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control DRAM refresh mode. In suspend mode, only the CAS-before-RAS mode is supported to save power consumption.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Self Refresh Mode</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>This bit is used to support the self-refresh function of EDO/FPM DRAM.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>Refresh period adjustment when CPU CLOCK changes</td>
</tr>
<tr>
<td></td>
<td>00 : Refresh period/1 when CPU clock /1</td>
</tr>
<tr>
<td></td>
<td>01 : Refresh period/2 when CPU clock /2</td>
</tr>
<tr>
<td></td>
<td>10 : Refresh period/4 when CPU clock /4</td>
</tr>
<tr>
<td></td>
<td>11 : Refresh period/8 when CPU clock /8</td>
</tr>
<tr>
<td></td>
<td>When system enters power saving mode, some system will reduce the CPU frequency. When CPU frequency is reduced, in order to sustain the same refresh rate. These two bits must be set to adjust the refresh period which is based on CPU frequency.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Refresh Queue</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
</tbody>
</table>
|            | This bit is used to control the DRAM Refresh Queue. M1541 has implemented 4 DRAM Refresh Queues. When DRAM refresh request collides with DRAM bus activity, this DRAM refresh will be delayed until the DRAM bus activity is finished. If the DRAM Refresh Queues are full, the DRAM refresh request becomes the top priority, and the other DRAM bus activity will be delayed.
<table>
<thead>
<tr>
<th>2-0 (0)</th>
<th>DRAM Refresh Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1024 CPU Clocks (15 us in 66Mhz).</td>
</tr>
<tr>
<td>001</td>
<td>2048 CPU Clocks (30 us in 66Mhz).</td>
</tr>
<tr>
<td>010</td>
<td>4096 CPU Clocks (60 us in 66Mhz).</td>
</tr>
<tr>
<td>011</td>
<td>8192 CPU Clocks (120 us in 66Mhz).</td>
</tr>
<tr>
<td>100</td>
<td>16384 CPU Clocks (256 us in 66Mhz).</td>
</tr>
<tr>
<td></td>
<td>These three bits are used to control the period to refresh DRAMs</td>
</tr>
</tbody>
</table>

Register Index : 5Fh  
Register Name : DRAM Page Mode Counter Control (00h, R/W) 
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>Enhanced Page Mode Counter</td>
</tr>
<tr>
<td>00</td>
<td>4 CPUCLKs</td>
</tr>
<tr>
<td>01</td>
<td>8 CPUCLKs</td>
</tr>
<tr>
<td>10</td>
<td>12 CPUCLKs</td>
</tr>
<tr>
<td>11</td>
<td>16 CPUCLKs</td>
</tr>
<tr>
<td></td>
<td>These two bits decide the duration from the time that sequencing have not accept a command, then close all DRAM pages after this duration.</td>
</tr>
<tr>
<td>5-1 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>DRAM Refresh Function</td>
</tr>
<tr>
<td>0</td>
<td>Enable</td>
</tr>
<tr>
<td>1</td>
<td>Disable</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, DRAM controller performs refresh cycle according to the period defined by x5Eh[2:0]. Otherwise, the DRAM controller will not perform refresh cycle.</td>
</tr>
</tbody>
</table>
Register Index : **60h**
Register Name : **DB0C1 - DRAM Row0 Configuration -1**
Default Value : 07h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (07h)</td>
<td>Row0 DRAM Top Address Boundary-1, A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index : **61h**
Register Name : **DB0C1I - DRAM Row0 Configuration-2**
Default Value : 40h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (01)   | DRAM MA Definition.  
  When set to Fast Page Mode DRAM or EDO DRAM ( bit[5:4] = 00 or 01 )  
  00 : Row0 DRAM Memory address mapping is Disable  
  01 : Row0 DRAM Memory address mapping uses Table 4-4.  
  10 : Row0 DRAM Memory address mapping uses Table 4-5.  
  11 : Row0 DRAM Memory address mapping uses Table 4-6.  
  When set to Register SDRAM or SDRAM ( bit[5:4] = 10 or 11 )  
  00 : Row0 DRAM Memory address mapping uses Table 4-7  
  01 : Row0 DRAM Memory address mapping uses Table 4-8  
  10 : Row0 DRAM Memory address mapping uses Table 4-9  
  11 : Row0 DRAM Memory address mapping uses Table 4-10  
  These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 0. |
| 5-4 (0h)   | Row0 DRAM Type.  
  00 : Standard Fast-Page Mode DRAM.  
  01 : EDO DRAM.  
  10 : Registered Synchronous DRAM  
  11 : Synchronous DRAM.  
  These two bits are used to program the DRAM type used on DRAM Row 0. |
| 3-0 (0h)   | Row0 DRAM Top Address Boundary-2, A31-A28 Address Boundary. |
These four bits are used to combine index-60h to decide the top memory size for DRAM Row 0.

Table 4-4. The following types of FPM/EDO DRAMs are supported when bits [7:6] = '01'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>512Kx8</td>
<td>4Mb</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>1Mx4</td>
<td>4Mb</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>1Mx16</td>
<td>16Mb</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>2Mx8</td>
<td>16Mb</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>4Mx4</td>
<td>16Mb</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>4Mx4</td>
<td>16Mb</td>
<td>12</td>
<td>10</td>
</tr>
</tbody>
</table>

Table 4-5. The following types of FPM/EDO DRAMs are supported when bits [7:6] = '10'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mx16</td>
<td>64Mb</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>8Mx8</td>
<td>64Mb</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>16Mx4</td>
<td>64Mb</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>
Table 4-6. The following types of FPM/EDO DRAMs are supported when bits [7:6] = '11'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Mx16</td>
<td>16Mb</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>2Mx8</td>
<td>16Mb</td>
<td>12</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 4-7. The following types of SDRAMs are supported when bit[7:6] = '00'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx512Kx16</td>
<td>16Mb</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>2Bx2Mx16</td>
<td>64Mb</td>
<td>13</td>
<td>8</td>
</tr>
<tr>
<td>4Bx1Mx16</td>
<td>64Mb</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>4Bx512Kx32</td>
<td>64Mb</td>
<td>11</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 4-8. The following types of SDRAMs are supported when bit[7:6] = '01'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx1Mx8</td>
<td>16Mb</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>2Bx4Mx8</td>
<td>64Mb</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>4Bx2Mx8</td>
<td>64Mb</td>
<td>12</td>
<td>9</td>
</tr>
<tr>
<td>4Bx1Mx16</td>
<td>64Mb</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>2Bx4Mx16</td>
<td>128Mb</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>4Bx2Mx16</td>
<td>128Mb</td>
<td>12</td>
<td>9</td>
</tr>
<tr>
<td>2Bx8Mx16</td>
<td>128Mb</td>
<td>14</td>
<td>9</td>
</tr>
<tr>
<td>4Bx4Mx16</td>
<td>128Mb</td>
<td>13</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 4-9. The following types of SDRAMs are supported when bit[7:6] = '10'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx2Mx4</td>
<td>16Mb</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>2Bx8Mx4</td>
<td>64Mb</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>4Bx4Mx4</td>
<td>64Mb</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>4Bx2Mx8</td>
<td>64Mb</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>
Table 4-10. The following types of SDRAMs are supported when bit[7:6] = ‘11’

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx8Mx8</td>
<td>128Mb</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>4Bx4Mx8</td>
<td>128Mb</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>2Bx16Mx8</td>
<td>256Mb</td>
<td>14</td>
<td>10</td>
</tr>
<tr>
<td>4Bx8Mx8</td>
<td>256Mb</td>
<td>13</td>
<td>10</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx16Mx4</td>
<td>128Mb</td>
<td>13</td>
<td>11</td>
</tr>
<tr>
<td>4Bx8Mx4</td>
<td>128Mb</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>2Bx32Mx4</td>
<td>256Mb</td>
<td>14</td>
<td>11</td>
</tr>
<tr>
<td>4Bx16Mx4</td>
<td>256Mb</td>
<td>13</td>
<td>11</td>
</tr>
</tbody>
</table>
The M1541 supports 8 rows of DRAM. DRAM Rowx Configuration register defines populated DRAM type and Top Address Boundary for each row. DB0CI and DB0CII define for Row 0, DB1CI and DB1CII define for Row 1, DB2CI and DB2CII define for Row 2, DB3CI and DB3CII define for Row 3, DB4CI and DB4CII define for Row 4, DB5CI and DB5CII define for Row 5, B6CI and DB6CII define for Row 6, and DB7CI and DB7CII define for Row 7. Contents of these 8-bit registers represent the boundary address in 1MB granularity and DRAM type populated.

The M1541 uses “Not less than” policy to determine which row memory address resides. For this reason, the address boundary for each row in index 6Fh to 60h should be the maximum memory value (Top address boundary) minus 1, as the following below description.

\[ \text{DB0CII}[3:0] \& \text{DB0CI}[7:0] = \text{Total amount of memory in row0} - 1 \text{ (Unit: 1MB)}. \]

\[ \text{DB0CII}[5:4] \text{ define different DRAM Type for row0}. \]

\[ \text{DB0CII}[7:6] \text{ define different MA Type or unpopulated for row0}. \]

\[ \text{DB1CII}[3:0] \& \text{DB1CI}[7:0] = \text{Total amount of memory in (row0 + row1)} - 1 \text{ (Unit: 1MB)}. \]

\[ \text{DB1CII}[5:4] \text{ define different DRAM Type for row1}. \]

\[ \text{DB1CII}[7:6] \text{ define different MA Type or unpopulated for row1}. \]

\[ \text{DB2CII}[3:0] \& \text{DB2CI}[7:0] = \text{Total amount of memory in (row0 + row1 + row2)} - 1 \text{ (Unit: 1MB)}. \]

\[ \text{DB2CII}[5:4] \text{ define different DRAM Type for row2}. \]

\[ \text{DB2CII}[7:6] \text{ define different MA Type or unpopulated for row2}. \]

\[ \text{DB3CII}[3:0] \& \text{DB3CI}[7:0] = \text{Total amount of memory in (row0 + row1 + row2 + row3)} - 1 \text{ (Unit: 1MB)}. \]

\[ \text{DB3CII}[5:4] \text{ define different DRAM Type for row3}. \]

\[ \text{DB3CII}[7:6] \text{ define different MA Type or unpopulated for row3}. \]

\[ \text{DB4CII}[3:0] \& \text{DB4CI}[7:0] = \text{Total amount of memory in (row0 + row1 + row2 + row3 + row4)} - 1 \text{ (Unit: 1MB)}. \]

DB4CII[7:6] define different MA Type or unpopulated for row4.

DB5CII[3:0]&DB5CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3 + row4 + row5) -1  (Unit: 1MB).

DB5CII[5:4] define different DRAM Type for row5.

DB5CII[7:6] define different MA Type or unpopulated for row5.

DB6CII[3:0]&DB6CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3 + row4 + row5 + row6) -1
(Unit: 1MB).


DB6CII[7:6] define different MA Type or unpopulated for row6.

DB7CII[3:0]&DB7CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3 + row4 + row5 + row6 + row7) -1
(in 1MB).

DB7CII[5:4] define different DRAM Type for row7.
DB7CII[7:6] define different MA Type or unpopulated for row7.

As an example of a system configuration where 8 physical rows are configured for either single-sided or double-sided SIMMs, the DRAM will be configured like the following figure.

```
<table>
<thead>
<tr>
<th>RAS7J</th>
<th>SIMM-7 Back</th>
<th>SIMM-6 Back</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS6J</td>
<td>SIMM-7 Front</td>
<td>SIMM-6 Front</td>
</tr>
<tr>
<td>RAS5J</td>
<td>SIMM-5 Back</td>
<td>SIMM-4 Back</td>
</tr>
<tr>
<td>RAS4J</td>
<td>SIMM-5 Front</td>
<td>SIMM-4 Front</td>
</tr>
<tr>
<td>RAS3J</td>
<td>SIMM-3 Back</td>
<td>SIMM-2 Back</td>
</tr>
<tr>
<td>RAS2J</td>
<td>SIMM-3 Front</td>
<td>SIMM-2 Front</td>
</tr>
<tr>
<td>RAS1J</td>
<td>SIMM-1 Back</td>
<td>SIMM-0 Back</td>
</tr>
<tr>
<td>RAS0J</td>
<td>SIMM-1 Front</td>
<td>SIMM-0 Front</td>
</tr>
</tbody>
</table>
```

CAS7J CAS6J
CASSJ CAS4J
CAS3J CAS2J
CAS1J CAS0J
In this configuration, the M1541 will drive two RASJ lines to the SIMM bank. If the single-sided SIMMs are populated, the even RASJ is used and the odd RASJ is not used. If the double-sided SIMMs are populated, both RASJ lines are used.

Example A
Two single-sided 1MB X 32 FPM DRAMs (standard MA mapping) are populated at row 0, a total of 8 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

- DB0CI = 07h DB0CII = 40h
- DB1CI = 07h DB1CII = 00h
- DB2CI = 07h DB2CII = 00h
- DB3CI = 07h DB3CII = 00h
- DB4CI = 07h DB4CII = 00h
- DB5CI = 07h DB5CII = 00h
- DB6CI = 07h DB6CII = 00h
- DB7CI = 07h DB7CII = 00h

Example B
Four single-sided 1MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 0 and row 2, a total of 16 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

- DB0CI = 07h DB0CII = D0h
- DB1CI = 07h DB1CII = 00h
- DB2CI = 0Fh DB2CII = D0h
- DB3CI = 0Fh DB3CII = 00h
- DB4CI = 0Fh DB4CII = 00h
- DB5CI = 0Fh DB5CII = 00h
- DB6CI = 0Fh DB6CII = 00h
- DB7CI = 0Fh DB7CII = 00h

Example C
Two double-sided 2MB X 32 FPM DRAMs (standard MA mapping) are populated on row 4, row 5, row 6, and row 7, a total of 32 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

- DB0CI = 00h DB0CII = 00h
- DB1CI = 00h DB1CII = 00h
- DB2CI = 00h DB2CII = 00h
- DB3CI = 00h DB3CII = 00h
Example D

One double-sided 2MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 2 and row 3, and one double-sided 8MB X 32 FPM DRAMs (64Mb MA mapping) are populated on row 6 and row 7, a total of 80 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

- \( DB0CI = 00h \) \( DB0CII = 00h \)
- \( DB1CI = 00h \) \( DB1CII = 00h \)
- \( DB2CI = 07h \) \( DB2CII = D0h \)
- \( DB3CI = 0Fh \) \( DB3CII = D0h \)
- \( DB4CI = 0Fh \) \( DB4CII = 00h \)
- \( DB5CI = 0Fh \) \( DB5CII = 00h \)
- \( DB6CI = 2Fh \) \( DB6CII = 80h \)
- \( DB7CI = 4Fh \) \( DB7CII = 80h \)
Register Index : 62h
Register Name : DB1CI - DRAM Row1 Configuration -1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row1 DRAM Top Address Boundary- 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index : 63h
Register Name : DB1CII - DRAM Row1 Configuration-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01)</td>
</tr>
<tr>
<td></td>
<td>00 : Row1 DRAM Memory address mapping is Disable</td>
</tr>
<tr>
<td></td>
<td>01 : Row1 DRAM Memory address mapping uses Table 4-4.</td>
</tr>
<tr>
<td></td>
<td>10 : Row1 DRAM Memory address mapping uses Table 4-5.</td>
</tr>
<tr>
<td></td>
<td>11 : Row1 DRAM Memory address mapping uses Table 4-6.</td>
</tr>
<tr>
<td></td>
<td>When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11)</td>
</tr>
<tr>
<td></td>
<td>00 : Row1 DRAM Memory address mapping uses Table 4-7.</td>
</tr>
<tr>
<td></td>
<td>01 : Row1 DRAM Memory address mapping uses Table 4-8.</td>
</tr>
<tr>
<td></td>
<td>10 : Row1 DRAM Memory address mapping uses Table 4-9.</td>
</tr>
<tr>
<td></td>
<td>11 : Row1 DRAM Memory address mapping uses Table 4-10.</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 1.</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row1 DRAM Type.</td>
</tr>
<tr>
<td></td>
<td>00 : Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td></td>
<td>01 : EDO DRAM.</td>
</tr>
<tr>
<td></td>
<td>10 : Registered Synchronous DRAM</td>
</tr>
<tr>
<td></td>
<td>11 : Synchronous DRAM.</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the DRAM type used on DRAM Row 1.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Row1 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 1.</td>
</tr>
</tbody>
</table>
Register Index : 64h
Register Name : DB2CI - DRAM Row2 Configuration-1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row2 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index : 65h
Register Name : DB2CII - DRAM Row2 Configuration-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01)</td>
</tr>
<tr>
<td></td>
<td>00 : Row2 DRAM Memory address mapping is Disable</td>
</tr>
<tr>
<td></td>
<td>01 : Row2 DRAM Memory address mapping uses Table 4-4</td>
</tr>
<tr>
<td></td>
<td>10 : Row2 DRAM Memory address mapping uses Table 4-5</td>
</tr>
<tr>
<td></td>
<td>11 : Row2 DRAM Memory address mapping uses Table 4-6</td>
</tr>
<tr>
<td></td>
<td>When set to Register SDRAM or SDRAM ( bit[5:4] = 10 or 11)</td>
</tr>
<tr>
<td></td>
<td>00 : Row2 DRAM Memory address mapping uses Table 4-7</td>
</tr>
<tr>
<td></td>
<td>01 : Row2 DRAM Memory address mapping uses Table 4-8</td>
</tr>
<tr>
<td></td>
<td>10 : Row2 DRAM Memory address mapping uses Table 4-9</td>
</tr>
<tr>
<td></td>
<td>11 : Row2 DRAM Memory address mapping uses Table 4-10</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 2.</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row2 DRAM Type.</td>
</tr>
<tr>
<td></td>
<td>00 : Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td></td>
<td>01 : EDO DRAM.</td>
</tr>
<tr>
<td></td>
<td>10 : Registered Synchronous DRAM</td>
</tr>
<tr>
<td></td>
<td>11 : Synchronous DRAM.</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the DRAM type used on DRAM Row 2.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Row2 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 2.</td>
</tr>
</tbody>
</table>
Register Index: **66h**  
Register Name: **DB3CI - DRAM Row3 Configuration-1**  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row3 DRAM Top Address Boundary – 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: **67h**  
Register Name: **DB3CII - DRAM Row3 Configuration-2**  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (00)   | DRAM MA Definition.  
When set to Fast Page Mode DRAM or EDO DRAM ( bit[5:4] = 00 or 01 )  
00 : Row3 DRAM Memory address mapping is Disable  
01 : Row3 DRAM Memory address mapping uses Table 4-4  
10 : Row3 DRAM Memory address mapping uses Table 4-5  
11 : Row3 DRAM Memory address mapping uses Table 4-6  
When set to Register SDRAM or SDRAM ( bit[5:4] = 10 or 11 )  
00 : Row3 DRAM Memory address mapping uses Table 4-7  
01 : Row3 DRAM Memory address mapping uses Table 4-8  
10 : Row3 DRAM Memory address mapping uses Table 4-9  
11 : Row3 DRAM Memory address mapping uses Table 4-10  
These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 3. |
| 5-4 (0h)   | Row3 DRAM Type.  
00 : Standard Fast-Page Mode DRAM.  
01 : EDO DRAM.  
10 : Registered Synchronous DRAM  
11 : Synchronous DRAM.  
These two bits are used to program the DRAM type used on DRAM Row 3. |
| 3-0 (0h)   | Row3 DRAM Top Address Boundary-2. A31-A28 Address Boundary. |
These four bits are used to combine index-60h to decide the top memory size for DRAM Row 3.
Register Index: 68h
Register Name: DB4CI - DRAM Row4 Configuration-1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row4 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: 69h
Register Name: DB4CII - DRAM Row4 Configuration-2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01)</td>
</tr>
<tr>
<td></td>
<td>00 : Row4 DRAM Memory address mapping is Disabled</td>
</tr>
<tr>
<td></td>
<td>01 : Row4 DRAM Memory address mapping uses Table 4-4</td>
</tr>
<tr>
<td></td>
<td>10 : Row4 DRAM Memory address mapping uses Table 4-5</td>
</tr>
<tr>
<td></td>
<td>11 : Row4 DRAM Memory address mapping uses Table 4-6</td>
</tr>
<tr>
<td></td>
<td>When set to Register SDRAM or SDRAM ( bit[5:4] = 10 or 11)</td>
</tr>
<tr>
<td></td>
<td>00 : Row4 DRAM Memory address mapping uses Table 4-7</td>
</tr>
<tr>
<td></td>
<td>01 : Row4 DRAM Memory address mapping uses Table 4-8</td>
</tr>
<tr>
<td></td>
<td>10 : Row4 DRAM Memory address mapping uses Table 4-9</td>
</tr>
<tr>
<td></td>
<td>11 : Row4 DRAM Memory address mapping uses Table 4-10</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 4.</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row4 DRAM Type.</td>
</tr>
<tr>
<td></td>
<td>00 : Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td></td>
<td>01 : EDO DRAM.</td>
</tr>
<tr>
<td></td>
<td>10 : Registered Synchronous DRAM</td>
</tr>
<tr>
<td></td>
<td>11 : Synchronous DRAM.</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the DRAM type used on DRAM Row 4.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Row4 DRAM Top Address Boundary-2. A31-A28 Address Boundary.</td>
</tr>
</tbody>
</table>
These four bits are used to combine index-60h to decide the top memory size for DRAM Row 4.

Register Index: 6Ah
Register Name: DB5CI - DRAM Row5 Configuration-1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row5 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: 6Bh
Register Name: DB5CII - DRAM Row0 Configuration-2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01)</td>
</tr>
<tr>
<td></td>
<td>00 : Row5 DRAM Memory address mapping is Disable</td>
</tr>
<tr>
<td></td>
<td>01 : Row5 DRAM Memory address mapping uses Table 4-4</td>
</tr>
<tr>
<td></td>
<td>10 : Row5 DRAM Memory address mapping uses Table 4-5</td>
</tr>
<tr>
<td></td>
<td>11 : Row5 DRAM Memory address mapping uses Table 4-6</td>
</tr>
<tr>
<td></td>
<td>When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11)</td>
</tr>
<tr>
<td></td>
<td>00 : Row5 DRAM Memory address mapping uses Table 4-7</td>
</tr>
<tr>
<td></td>
<td>01 : Row5 DRAM Memory address mapping uses Table 4-8</td>
</tr>
<tr>
<td></td>
<td>10 : Row5 DRAM Memory address mapping uses Table 4-9</td>
</tr>
<tr>
<td></td>
<td>11 : Row5 DRAM Memory address mapping uses Table 4-10</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the Memory MA used on FPM or EDO DRAM/ Synchronous DRAM Row 5.</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row5 DRAM Type.</td>
</tr>
<tr>
<td>----------</td>
<td>-----------------</td>
</tr>
<tr>
<td>00 :</td>
<td>Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td>01 :</td>
<td>EDO DRAM.</td>
</tr>
<tr>
<td>10 :</td>
<td>Registered Synchronous DRAM</td>
</tr>
<tr>
<td>11 :</td>
<td>Synchronous DRAM.</td>
</tr>
</tbody>
</table>

These two bits are used to program the DRAM type used on DRAM Row 5.

<table>
<thead>
<tr>
<th>3-0 (0h)</th>
<th>Row5 DRAM Top Address Boundary-2. A31-A28 Address Boundary.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>These four bits are used to combine index-60h to decide the top memory size for DRAM Row 5.</td>
</tr>
</tbody>
</table>
Register Index: 6Ch
Register Name: DB6CI - DRAM Row6 Configuration-1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row6 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: 6Dh
Register Name: DB6CII - DRAM Row6 Configuration-2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01)</td>
</tr>
<tr>
<td></td>
<td>00: Row6 DRAM Memory address mapping is Disable</td>
</tr>
<tr>
<td></td>
<td>01: Row6 DRAM Memory address mapping uses Table 4-4</td>
</tr>
<tr>
<td></td>
<td>10: Row6 DRAM Memory address mapping uses Table 4-5</td>
</tr>
<tr>
<td></td>
<td>11: Row6 DRAM Memory address mapping uses Table 4-6</td>
</tr>
<tr>
<td></td>
<td>When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11)</td>
</tr>
<tr>
<td></td>
<td>00: Row6 DRAM Memory address mapping uses Table 4-7</td>
</tr>
<tr>
<td></td>
<td>01: Row6 DRAM Memory address mapping uses Table 4-8</td>
</tr>
<tr>
<td></td>
<td>10: Row6 DRAM Memory address mapping uses Table 4-9</td>
</tr>
<tr>
<td></td>
<td>11: Row6 DRAM Memory address mapping uses Table 4-10</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the Memory MA used on FPM or EDO DRAM/ Synchronous DRAM Row 6.</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row6 DRAM Type.</td>
</tr>
<tr>
<td></td>
<td>00: Standard Fast-Page Mode DRAM</td>
</tr>
<tr>
<td></td>
<td>01: EDO DRAM</td>
</tr>
<tr>
<td></td>
<td>10: Registered Synchronous DRAM</td>
</tr>
<tr>
<td></td>
<td>11: Synchronous DRAM</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the DRAM type used on DRAM Row 6.</td>
</tr>
</tbody>
</table>
3-0 (0h) | Row6 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 6.

Register Index : 6Eh
Register Name : DB7CI - DRAM Row7 Configuration-1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row7 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index : 6Fh
Register Name : DB7CII - DRAM Row7 Configuration-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>DRAM MA Definition. When set to Fast Page mode DRAM or EDO DRAM ( bit[5:4] = 00 or 01 ) 00 : Row7 DRAM Memory address mapping is Disable 01 : Row7 DRAM Memory address mapping uses Table 4-4 10 : Row7 DRAM Memory address mapping uses Table 4-5 11 : Row7 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM ( bit[5:4] = 10 or 11) 00 : Row7 DRAM Memory address mapping uses Table 4-7 01 : Row7 DRAM Memory address mapping uses Table 4-8 10 : Row7 DRAM Memory address mapping uses Table 4-9 11 : Row7 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 7.</td>
</tr>
</tbody>
</table>
| 5-4 (0h) | Row7 DRAM Type.  
00 : Standard Fast-Page Mode DRAM.  
01 : EDO DRAM.  
10 : Registered Synchronous DRAM  
11 : Synchronous DRAM.  
These two bits are used to program the DRAM type used on DRAM Row 7. |
| 3-0 (0h) | Row7 DRAM Top Address Boundary-2. A31-A28 Address Boundary.  
These four bits are used to combine index-60h to decide the top memory size for DRAM Row 7. |
Register Index: 70h  
Register Name: SDM256MB[7:0] - 256Mbit SDRAM select  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | ROW7 sets to 256Mbit SDRAM  
            | 0: Disable  
            | 1: Enable  
            | When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW7. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW7. |
| 6 (0)      | ROW6 sets to 256Mbit SDRAM  
            | 0: Disable  
            | 1: Enable  
            | When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW6. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW6. |
| 5 (0)      | ROW5 sets to 256Mbit SDRAM  
            | 0: Disable  
            | 1: Enable  
            | When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW5. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW5. |
| 4 (0)      | ROW4 sets to 256Mbit SDRAM  
            | 0: Disable  
            | 1: Enable  
            | When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW4. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW4. |
| 3 (0) | ROW3 sets to 256Mbit SDRAM  
0 : Disable  
1 : Enable  
When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW3. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW3. |
|---|---|
| 2 (0) | ROW2 sets to 256Mbit SDRAM  
0 : Disable  
1 : Enable  
When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW2. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW2. |
| 1 (0) | ROW1 sets to 256Mbit SDRAM  
0 : Disable  
1 : Enable  
When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW1. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW1. |
| 0 (0) | ROW0 sets to 256Mbit SDRAM  
0 : Disable  
1 : Enable  
When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW0. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW0. |
Register Index : 71h
Register Name : SDM4BANK[7:0] - SDRAM internal 2/4 Banks select
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Number of SDRAM internal bank of ROW7</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Number of SDRAM internal bank of ROW6</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Number of SDRAM internal bank of ROW5</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Number of SDRAM internal bank of ROW4</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Number of SDRAM internal bank of ROW3</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Number of SDRAM internal bank of ROW2</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>Number of SDRAM internal bank of ROW1</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>Number of SDRAM internal bank of ROW0</td>
</tr>
<tr>
<td></td>
<td>0 : 2 Banks, 1 : 4 Banks</td>
</tr>
<tr>
<td></td>
<td>This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.</td>
</tr>
</tbody>
</table>

Register Index : 72h
Register Name : SDRAM100 - SDRAM 100 MHz timing select.
Default Value : 00h
### Attribute: Read/Write

**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Trcd (SDRAM SRASJ to SCASJ delay) select when bit 6 = 1 enable</td>
</tr>
<tr>
<td></td>
<td>0 : Trcd = 3 CLKs</td>
</tr>
<tr>
<td></td>
<td>1 : Trcd = 2 CLKs</td>
</tr>
<tr>
<td></td>
<td>When bit 6 = 1 enable separate setting for Trcd and CL, this bit will decide the Trcd.</td>
</tr>
<tr>
<td></td>
<td>For M1541/M1542A1 E and later versions.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Enable the separate setting for Trcd (SDRAM SRASJ to SCASJ delay) and CL (SCASJ Latency)</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>When this bit set to 1, Trcd will be decided by index 72h bit 7 and CL will be decided by index 48h bit 4. For M1541/M1542A1 E and later versions.</td>
</tr>
<tr>
<td>5-3 (0h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Internal command sent to SDRAM controller delay 1 CPU clock</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is set to enable, the command sent to SDRAM controller will add one CPU clock delay.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>The SDRAM change row delays 1 CPU clock for 100 MHz.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>For 100MHz frequency, the consecutive different row read cycle performs X-1-1-1-2-1-1-1 when the second cycle is a page hit read.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>SDRAM ensures 4 data duration intervals.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>This option will ensure four data duration between each DRAM cycle and prevent current cycle from being interrupted by the next DRAM command.</td>
</tr>
</tbody>
</table>
Register Index: 73h
Register Name: 100 MHz Frequency timing Control
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (00h)</td>
<td>Reserved</td>
</tr>
<tr>
<td>4-3 (00)</td>
<td>Clock delay of DRAM Read Pipe Function</td>
</tr>
<tr>
<td></td>
<td>00: 0 ns</td>
</tr>
<tr>
<td></td>
<td>01: 1 ns</td>
</tr>
<tr>
<td></td>
<td>10: 2 ns</td>
</tr>
<tr>
<td></td>
<td>11: 3 ns</td>
</tr>
</tbody>
</table>

When index 73h bit 2 (MD input pipeline function) is enabled, these two bits control the clock delay of the additional MD input pipeline stage. By this function, M1541 minimizes the MD setup time.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 (0)</td>
<td>DRAM Read Pipe Function</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

This configuration setting adds an additional pipeline stage for memory data input path. It is used for minimizing the MD required setup time when supporting 100MHz SDRAM bus.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (0)</td>
<td>SDRAM Command and Data Output Pipeline Function</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

This configuration enables an additional pipeline stage for SDRAM control signal and write data. The additional pipeline stage clock source is ahead by PLL. With this additional pipeline stage, M1541 can maintain enough signal setup time for SDRAM when running at 100 MHz.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (0)</td>
<td>75-100 MHz frequency MD output pipe</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
</tbody>
</table>

This option is used to add an additional internal output data pipeline stage.

Register Index: 83h-74h
Register Name: Reserved Registers
Default Value: 00h
Attribute: Read Only
Register Index: 85h-84h
Register Name: **PCI Programmable Frame Buffer Memory Region**
Default Value: 00h
Attribute: Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 15-4 (000h) | Starting Address of Programmable Frame Buffer  
The 12 bits correspond to A[31:20] of the starting address.  
The remaining bits A[19:0] are assumed to be zero. |
| 3-0 (0h)   | Size of Programmable Frame Buffer  
0000 : 1 MBytes.  
0001 : 2 MBytes.  
0010 : 4 MBytes.  
0011 : 8 MBytes.  
0100 : 16 MBytes.  
1XXX : all CPU to PCI Memory Write cycle into buffer  
The Frame Buffer Region should not overlap with local memory. |
Register Index: **86h**
Register Name: **CPU to PCI Write Buffer Option**
Default Value: **00h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>Reserved</td>
</tr>
<tr>
<td>3 (0)</td>
<td>LINEAR_WORD-Merge for Frame Buffer Cycle</td>
</tr>
<tr>
<td>0 : disable, 1 : enable</td>
<td></td>
</tr>
<tr>
<td>When this bit is enable, only the words which address are consecutive linear can be merged into one line.</td>
<td></td>
</tr>
<tr>
<td>2 (0)</td>
<td>Use PCI Write-Burst for Frame Buffer cycle</td>
</tr>
<tr>
<td>0 : disable, 1 : enable</td>
<td></td>
</tr>
<tr>
<td>If this bit is enable, consecutive PCI write cycle which the address is reside the frame buffer region will become burst cycle on the PCI bus.</td>
<td></td>
</tr>
<tr>
<td>1 (0)</td>
<td>VGA 0A0000-0BFFFF Fixed frame buffer</td>
</tr>
<tr>
<td>0 : disable, 1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit is used to enable both the Frame buffer which address is fixed at 0A0000h-0B0000h and the Host to PCI_33 write buffer for Frame buffer cycle.</td>
<td></td>
</tr>
<tr>
<td>0 (0)</td>
<td>Programmable Frame buffer</td>
</tr>
<tr>
<td>0 : disable, 1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit is used to combine with index 85h and 84h to enable the PCI Frame buffer and CPU to PCI_33 write buffer.</td>
<td></td>
</tr>
</tbody>
</table>

Register Index: **87h**
Register Name: **H2PO - CPU to PCI Option**
Default Value: **00h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>PCI signal Distributed Output</td>
</tr>
<tr>
<td>0 : Disable, 1 : Enable</td>
<td></td>
</tr>
<tr>
<td>If this bit is enable, the PCI interface output signals are stepping.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>---</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 6 (0) | APIC support, i.e. invalidate PCI to DRAM Read Ahead Buffer (P2HR) buffer when PHLDAJ goes low 0 : disable, 1 : enable  
When APIC is supported in Dual Processor system, this bit must be set to '1' to invalidate PCI to DRAM Read Ahead Buffer since the M1541 cannot realize Interrupt Synchronous event. But in Single Processor systems, the M1541 can detect Interrupt Synchronous event to invalidate PCI to DRAM Read Ahead Buffer automatically. This bit is recommended to be reset to '0' in Single Processor systems. |
| 5 (0) | Translate CPU Shutdown cycle to Port 92 cycle 0 : enable, 1 : disable  
When this bit is set to '1', the M1541 will forward a shutdown special cycle from CPU bus to PCI bus. When this bit is set to '0', the M1541 will translate the shutdown cycle to I/O write cycle with I/O address 092h and write data is 01h. |
| 4(0) | H2P CLKRUN Control Mode 0 : Normal mode, 1 : Safe Mode  
If this bit is set to '0', the internal PCI clock is gated after the host to PCI cycle is complete. If this bit is set to '1', the internal PCI clock is gated when the next cycle is not Host to PCI cycle. |
| 3-2 (00) | H2PW Buffered Cycle Flush Waits Selection 00 : Wait 0 PCICLKs, 01 : Wait 2 PCICLKs  
10 : Wait 3 PCICLKs, 11 : Wait 4 PCICLKs  
These 2 bits define the latency time from the time H2P write data get into H2PW buffer to the time assert flush request. This option will increase the possibility for merging the consequent H2PW cycle. |
| 1 (0) | CPU Lock cycle when writing to FRAME buffer 0 : Ignore Lock, treat as non lock cycle, 1 : normal  
When this configuration is set to '1', CPU to PCI write cycle with HLOCKJ asserted will not be buffered. M1541 treats this kind of cycle as non-buffer cycle. |
| 0 (0) | CPU-to-PCI Lock cycle. 0 : normal, 1 : Ignore lock  
If this bit is set to '0', M1541 will transfer host lock cycle to PCI lock cycle. If this bit is set to '1', M1541 will ignore the HLOCKJ and no PCI lock cycle will be generated. |
4.4 PCI_33 PCI to Host interface

Register Index : 88h
Register Name : P2HO - PCI to Main Memory / PCI Arbiter Option
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>PCI master RETRY GAT mode</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>When this bit is enable, if PCI master is retried during a read transaction, the master will be marked as a GAT master. When the same master retry the transaction at a later time, M1541 will flush the designed buffers before granting the bus ownership to it.</td>
<td></td>
</tr>
<tr>
<td>6 (0)</td>
<td>PCI Master Lock signal for PCI Arbiter</td>
</tr>
<tr>
<td>0 : enable</td>
<td></td>
</tr>
<tr>
<td>1 : disable</td>
<td></td>
</tr>
<tr>
<td>When this bit is enable, the arbiter will not re-arbitrate the PCI bus during the locked transaction.</td>
<td></td>
</tr>
<tr>
<td>5 (0)</td>
<td>Flush H2PW buffer before grant to PCI</td>
</tr>
<tr>
<td>0 : Enable</td>
<td></td>
</tr>
<tr>
<td>1 : Disable</td>
<td></td>
</tr>
<tr>
<td>When this bit is enable and index 88h bit0=1 (IAS master GAT mode disable) or bit3=1 (Force PCI GAT mode disable), M1541 will flush internal CPU to PCI posted write buffer before granting the PCI_33 bus ownership to the master in GAT mode.</td>
<td></td>
</tr>
<tr>
<td>4 (0)</td>
<td>PCI Master LOCKJ signal for P2H cycle.</td>
</tr>
<tr>
<td>0 : Enable</td>
<td></td>
</tr>
<tr>
<td>1 : Disable</td>
<td></td>
</tr>
<tr>
<td>When this bit is enable, the M1541 will recognize LOCKJ signaled by PCI master. Otherwise the M1541 will ignore the LOCKJ signal issued by PCI master.</td>
<td></td>
</tr>
<tr>
<td>Bit</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Force PCI GAT Mode</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, the M1541 will flush all</td>
</tr>
<tr>
<td></td>
<td>necessary buffers before granting to the PCI master.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>CPU access PCI during Passive Release</td>
</tr>
<tr>
<td></td>
<td>This bit controls CPU to PCI access during Passive</td>
</tr>
<tr>
<td></td>
<td>Release. When it is enabled, CPU to PCI access is</td>
</tr>
<tr>
<td></td>
<td>allowed during Passive Release. Otherwise, arbiter</td>
</tr>
<tr>
<td></td>
<td>only accepts another PCI master access to local DRAM.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>Passive Release of PHOLD</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, the M1541 will recognize</td>
</tr>
<tr>
<td></td>
<td>Passive Release signaled from M1533/M1543 by de-asserting PHOLDJ for a PCI Clock and then asserting PHOLDJ for a PCI Clock. The M1541 will de-assert the PHLDAJ signal and re-arbitrate PCI bus request and possibly allow the CPU to access PCI depending on the bit 2 setting. When this bit is disabled, the M1541 does not recognize Passive Release, i.e., PHLDAJ will be continued to be asserted. A value '1' is recommended for normal operation.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>ISA master GAT mode</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, the M1541 will perform the</td>
</tr>
</tbody>
</table>
Register Index: 89h
Register Name: PCI Arbiter Time Slice
Default Value: 20h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (20h)</td>
<td>Number of PCI clocks for PCI Bus time slice. The time-slice will guarantee the minimum clocks that the PCI master be granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. The bits 1-0 are assumed to be &quot;00&quot; and are ignored.</td>
</tr>
</tbody>
</table>

Register Index: 8Ah
Register Name: CPU Arbiter Time Slice
Default Value: 20h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (20h)</td>
<td>Number of PCI clocks for CPU Bus time slice. The time-slice will guarantee the minimum clocks that the CPU master be granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. The bits 1-0 are assumed to be &quot;00&quot; and are ignored.</td>
</tr>
</tbody>
</table>
Register Index : **8Bh**  
Register Name : **PCIRC - PCI Retry Control for P2H Cycle**  
Default Value : **00h**  
Attribute : **Read/Write**  
Size : **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>5-4 (00)</td>
<td><strong>Time Slice Scaling for CPU and PCI Master in &quot;Passive Release&quot; Period</strong></td>
</tr>
<tr>
<td></td>
<td>00 : divide by 2</td>
</tr>
<tr>
<td></td>
<td>01 : divide by 4</td>
</tr>
<tr>
<td></td>
<td>10 : divide by 8</td>
</tr>
<tr>
<td></td>
<td>11 : divide by 1</td>
</tr>
<tr>
<td></td>
<td>These bits provide software configuration of resizing the number of time slice in index 89h and 8Ah.</td>
</tr>
<tr>
<td>3-2 (0)</td>
<td><strong>Retry latency for Second Data Phase control</strong></td>
</tr>
<tr>
<td></td>
<td>00 : Retry on first Data phase if wait state &gt; 8 PCI clocks</td>
</tr>
<tr>
<td></td>
<td>01 : Retry on first Data phase if wait state &gt; 4 PCI clocks</td>
</tr>
<tr>
<td></td>
<td>10 : Retry on first Data phase if wait state &gt; 2 PCI clocks</td>
</tr>
<tr>
<td></td>
<td>11 : Never Retry on Second Data phase</td>
</tr>
<tr>
<td></td>
<td>These bits are used to retry a PCI master cycle when the latency to the second data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1541 will complete the second data transfer regardless of latency.</td>
</tr>
<tr>
<td>1-0 (0)</td>
<td><strong>Retry latency for First Data Phase control</strong></td>
</tr>
<tr>
<td></td>
<td>00 : Retry on first Data phase if wait state &gt; 32 PCI clocks</td>
</tr>
<tr>
<td></td>
<td>01 : Retry on first Data phase if wait state &gt; 16 PCI clocks</td>
</tr>
<tr>
<td></td>
<td>10 : Retry on first Data phase if wait state &gt; 8 PCI clocks</td>
</tr>
<tr>
<td></td>
<td>11 : Never Retry on Second Data phase</td>
</tr>
<tr>
<td></td>
<td>These bits are used to retry a PCI master cycle when the latency to the first data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1541 will complete the first data transfer regardless of latency.</td>
</tr>
</tbody>
</table>
Register Index : 8Ch  
Register Name : PCI to Main Memory Option  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7(0)</td>
<td>Enable PCI master0 as Non_Preempt master (for P2P)</td>
</tr>
<tr>
<td></td>
<td>0 : disable, 1 : enable, when this bit is enable, PCI master0 will be treated as a non_preempt master. During its access, the PCI bus ownership will not be re-arbitrated.</td>
</tr>
<tr>
<td>6(0)</td>
<td>PCI Master Access M1541 Configuration Register. This bit decides whether the PCI master can access the configuration register or not.</td>
</tr>
<tr>
<td></td>
<td>0 : disable, only CPU can access M1541 configuration register. 1 : enable</td>
</tr>
<tr>
<td>5(0)</td>
<td>P2HW burst support. This bit provides the capability of supporting the PCI master burst write transaction.</td>
</tr>
<tr>
<td></td>
<td>0 : enable, 1 : disable</td>
</tr>
<tr>
<td>4(0)</td>
<td>P2HR burst support. This bit provides the capability of supporting the PCI master burst read transaction.</td>
</tr>
<tr>
<td></td>
<td>0 : enable, 1 : disable</td>
</tr>
<tr>
<td>3(0)</td>
<td>PCI master Read pre-fetch. This bit controls the M1541’s ability to pre-fetch data for PCI master read transaction.</td>
</tr>
<tr>
<td></td>
<td>0 : enable, 1 : disable</td>
</tr>
<tr>
<td>2-0 (000)</td>
<td>P2H Read buffer Pre-fetch Threshold. These bits control the M1541’s pre-fetch behavior in the case of PCI master read and pre-fetch is enable.</td>
</tr>
<tr>
<td></td>
<td>000 : 1 buffer</td>
</tr>
<tr>
<td></td>
<td>001 : 2 buffers</td>
</tr>
<tr>
<td></td>
<td>010 : 3 buffers</td>
</tr>
<tr>
<td></td>
<td>011 : 4 buffers</td>
</tr>
<tr>
<td></td>
<td>100 : 5 buffers</td>
</tr>
<tr>
<td></td>
<td>101 : 6 buffers</td>
</tr>
<tr>
<td></td>
<td>110 : 7 buffers</td>
</tr>
<tr>
<td></td>
<td>111 : 8 buffers</td>
</tr>
</tbody>
</table>
Register Index : 8Dh
Register Name : PCI Clock Control
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (0h)</td>
<td>P2HW Slice Control Timer. These bits control the time slice for PCI-to-DRAM write in the M1541 internal write bus.</td>
</tr>
<tr>
<td></td>
<td>0000 : 0 CLK</td>
</tr>
<tr>
<td></td>
<td>0001 : 1 CLK</td>
</tr>
<tr>
<td></td>
<td>0010 : 2 CLks</td>
</tr>
<tr>
<td></td>
<td>0011 : 3 CLks</td>
</tr>
<tr>
<td></td>
<td>1111 : 15 CLks</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Miss Read Pending Delay Timeout Retry</td>
</tr>
<tr>
<td></td>
<td>0 : enable, 1 : disable</td>
</tr>
<tr>
<td></td>
<td>When enabled, PCI master read will not be retried until the M1541 issues a read transaction to memory even if the PCI master's time slice has expired.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Internal Write Bus Pipeline Function.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable, 1 : Enable, this bit enables the M1541 internal write bus pipeline function.</td>
</tr>
<tr>
<td>2-0 (000)</td>
<td>PCI Frequency Mode</td>
</tr>
<tr>
<td></td>
<td>110 : 2X</td>
</tr>
<tr>
<td></td>
<td>101 : 2.5X</td>
</tr>
<tr>
<td></td>
<td>011 : 3X</td>
</tr>
<tr>
<td></td>
<td>others : Reserved</td>
</tr>
<tr>
<td></td>
<td>These bits reflect the relationship between CPU external frequency and PCI bus frequency. In order to keep the PCI frequency at 33 MHz, different CPU external frequencies should be set to different modes.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU External Frequency</th>
<th>PCI Frequency Mode</th>
<th>PCI Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>50/60/66 MHz</td>
<td>110 : 2X</td>
<td>25/30/33 MHz</td>
</tr>
<tr>
<td>75/83 MHz</td>
<td>101 : 2.5X</td>
<td>30/33 MHz</td>
</tr>
<tr>
<td>100 MHz</td>
<td>011 : 3X</td>
<td>33 MHz</td>
</tr>
</tbody>
</table>
Register Index : 08Eh  
Register Name : Internal Arbiter Write Control  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>AGPW Slice Control Timer. These bits control the time slice for AGP to DRAM write in the M1541 internal write bus</td>
</tr>
<tr>
<td></td>
<td>0000 : 0 CLK</td>
</tr>
<tr>
<td></td>
<td>0001 : 1 CLK</td>
</tr>
<tr>
<td></td>
<td>0010 : 2 CLks</td>
</tr>
<tr>
<td></td>
<td>:</td>
</tr>
<tr>
<td></td>
<td>1111 : 15 CLks</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>G2HW Slice Control Timer. These bits control the time slice for PCI_66 to DRAM write in the M1541 internal write bus</td>
</tr>
<tr>
<td></td>
<td>0000 : 0 CLK</td>
</tr>
<tr>
<td></td>
<td>0001 : 1 CLK</td>
</tr>
<tr>
<td></td>
<td>0010 : 2 CLks</td>
</tr>
<tr>
<td></td>
<td>:</td>
</tr>
<tr>
<td></td>
<td>1111 : 15 CLks</td>
</tr>
</tbody>
</table>
Register Index : 08Fh  
Register Name : Internal Arbiter P2H Read Control  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7-4 (0h) | G2HR Slice Control Timer. These bits control the time slice for PCI_66 to Host Read in the M1541 internal read bus  
0000 : 0 CLK  
0001 : 1 CLK  
0010 : 2 CLKs  
:  
1111 : 15 CLKs |
| 3-0 (0h) | P2HR Slice Control Timer. These bits control the time slice for PCI_33 to Host read in the M1541 internal read bus  
0000 : 0 CLK  
0001 : 1 CLK  
0010 : 2 CLKs  
:  
1111 : 15 CLKs |
Register Index : 90h
Register Name : LRWCTL - Lock Read/Write Control
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Interrupt line register read/write control</td>
</tr>
<tr>
<td></td>
<td>0 : disable, 1 : enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 interrupt line register located at index 3Ch is unlock and can be read and written. When this bit is disable, M1541 interrupt line register located at index 3Ch is read only.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>AGP register Locked read/write control</td>
</tr>
<tr>
<td></td>
<td>0 : disable (Read only), 1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 AGP register located at index 0b7h to 0b0h all are unlock and can be read and written. When this bit is disable, M1541 AGP register located at index 0b7h to 0b0h are read only.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Power Management Locked read/write control</td>
</tr>
<tr>
<td></td>
<td>0 : disable (Read only), 1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 Power management register located at index 0e7h to 0e0h all are unlock and can be read and written. When this bit is disable, M1541 Power management register located at index 0e7h to 0e0h are read only.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>PLL control register Locked read/write control</td>
</tr>
<tr>
<td></td>
<td>0 : disable (Read only), 1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 PLL control register located at index 0EDh are unlock and can be read and written. When this bit is disable, M1541 PLL control register located at index 0EDh are read only.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>M5243 PCI to PCI bridge Device Identification Register Locked read/write control</td>
</tr>
<tr>
<td></td>
<td>0 : disable (Read only), 1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M5243 DID register located at M5243 index 03h to 02h all are unlock and can be read and written. When this bit is disable, M5243 DID register located at M5243 index 03h to 02h are read only.</td>
</tr>
<tr>
<td>Register Index</td>
<td>M1541 Power management Base address of ACPI PM2_CNT port register Locked read/write control</td>
</tr>
<tr>
<td>----------------</td>
<td>------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>0 : disable (Read only)</td>
</tr>
<tr>
<td></td>
<td>1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 Base address of ACPI PM2_CNT port register located at index 0e9h to 0e8h all are unlock and can be read and written.</td>
</tr>
<tr>
<td></td>
<td>When this bit is disable, M1541 Base address of ACPI PM2_CNT port register located at index 0e9h to 0e8h are read only.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Index</th>
<th>M1541 Device 0 Capabilities Pointer register Locked read/write control</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 : disable (Read only)</td>
</tr>
<tr>
<td></td>
<td>1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 Device 0 Capabilities Pointer register located at index 34h is unlock and can be read and written. When this bit is disable, M1541 Device 0 Capabilities Pointer register located at index 34h is read only.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Index</th>
<th>M1541 sub-vender identification register Locked read/write control</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 : disable (Read only)</td>
</tr>
<tr>
<td></td>
<td>1 : enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, M1541 sub-vender identification register located at index 2dh to 2ch are unlock and can be read and written. When this bit is disable, M1541 sub-vender identification register index 2dh to 2ch is read only.</td>
</tr>
</tbody>
</table>

**Register Index**: 91h  
**Register Name**: BRSYCTL - Broadcast and Synchronous cycle Control  
**Default Value**: 13h  
**Attribute**: Read/Write  
**Size**: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (1)</td>
<td>INTA, Special cycle broadcast to both PCI_66 and PCI_33 bus</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>This bit enables M1541 broadcast the interrupt acknowledge and special cycle to both PCI and AGP bus.</td>
</tr>
</tbody>
</table>

**Register Index**: 0AFh-92h  
**Register Name**: Reserved Registers  
**Default Value**: 00h  
**Attribute**: Read Only
4.5 AGP Interface Registers

Register Index: 0B3h-0B0h
Register Name: A.G.P. Capability Identifier Registers
Default Value: 0010E002h
Attribute: Read Only
Size: 32 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24 (00h)</td>
<td>Reserved</td>
</tr>
<tr>
<td>23-20 (1h)</td>
<td>Major A.G.P. Revision Number (Hardwired to &quot;0001&quot;)</td>
</tr>
<tr>
<td>19-16 (0h)</td>
<td>Minor A.G.P. Revision Number (Hardwired to &quot;0000&quot;)</td>
</tr>
<tr>
<td>15-8 (0E0h)</td>
<td>Next Capability Pointer (Hardwired to &quot;11100000&quot;=0e0h)</td>
</tr>
<tr>
<td>7-0 (02h)</td>
<td>A.G.P. Capability ID (Defaults to &quot;00000010&quot;=02h)</td>
</tr>
</tbody>
</table>

Register Index: 0B7h-0B4h
Register Name: A.G.P. Status Registers
Default Value: 1C000203h
Attribute: Locked Read/write
Default is read only. When index-90h bit 0 is 1, these bits can read/write.
Size: 32 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24 (1Ch)</td>
<td>A.G.P. Request Queue Depth (Locked Read/Write, Default=1Ch)</td>
</tr>
<tr>
<td>23-10 (0000h)</td>
<td>Reserved, Hardwired to '0' (Read only)</td>
</tr>
<tr>
<td>9 (1)</td>
<td>SBA (Side Band Address) function (Locked Read/write)</td>
</tr>
<tr>
<td>8-2 (00h)</td>
<td>Reserved</td>
</tr>
<tr>
<td>1 (1)</td>
<td>A.G.P. Data Transfer Type Supported (Locked Read/Write) - 2X clocking mode</td>
</tr>
<tr>
<td>0 (1)</td>
<td>A.G.P. Data Transfer Type Supported (Locked Read/Write) - 1X clocking mode</td>
</tr>
</tbody>
</table>
Register Name: **A.G.P. Command Registers**

Default Value: 0000000h

Attribute: Read/Write

Size: 32 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24 (00h)</td>
<td>RQ_DEPTH</td>
</tr>
<tr>
<td></td>
<td>A.G.P. Request Queue Depth</td>
</tr>
<tr>
<td>23-10 (0000h)</td>
<td>Reserved, Hardwired to '00000' (Read only)</td>
</tr>
<tr>
<td>9 (0)</td>
<td>SBA_ENABLE (Read/write)</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit can enable or disable the SBA function.</td>
<td></td>
</tr>
<tr>
<td>8 (0)</td>
<td>AGP_ENABLE (Read/Write)</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit can enable or disable the AGP function.</td>
<td></td>
</tr>
<tr>
<td>7-2 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>A.G.P. Data Transfer Type Supported - 2X clocking mode</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit can enable or disable the 2X function.</td>
<td></td>
</tr>
<tr>
<td>0 (0)</td>
<td>A.G.P. Data Transfer Type Supported - 1X clocking mode</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit can enable or disable the 1X function.</td>
<td></td>
</tr>
</tbody>
</table>
Register Index : 0B9h
Register Name : A.G.P. Enable Registers
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-1 (00)</td>
<td>Reserved</td>
</tr>
<tr>
<td>0 (0)</td>
<td>AGP_Enable (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>This bit can enable/disable the AGP function.</td>
</tr>
</tbody>
</table>

Register Index : 0BFh-0BCh
Register Name : Aperture Control Register
Default Value : 00000000h
Attribute : Read/write
Size : 32 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-12 (0000h)</td>
<td>Graphics Aperture Remapping Table Base address</td>
</tr>
<tr>
<td></td>
<td>The address is from A[31] to A[12]. It is based on 4K bytes boundary.</td>
</tr>
<tr>
<td>11-4 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Graphics Aperture Size (Defaults to &quot;0000&quot;) GA_SIZE</td>
</tr>
<tr>
<td>0000 0MB</td>
<td>x10 D[31:0] =&gt; '0'</td>
</tr>
<tr>
<td>0001 1MB</td>
<td>x10 D[31:20] R/W, D[19:0] =&gt; '0'</td>
</tr>
<tr>
<td>0010 2MB</td>
<td>x10 D[31:21] R/W, D[20:0] =&gt; '0'</td>
</tr>
<tr>
<td>0011 4MB</td>
<td>x10 D[31:22] R/W, D[21:0] =&gt; '0'</td>
</tr>
<tr>
<td>0100 8MB</td>
<td>x10 D[31:23] R/W, D[22:0] =&gt; '0'</td>
</tr>
<tr>
<td>0110 16MB</td>
<td>x10 D[31:24] R/W, D[23:0] =&gt; '0'</td>
</tr>
<tr>
<td>0111 32MB</td>
<td>x10 D[31:25] R/W, D[24:0] =&gt; '0'</td>
</tr>
<tr>
<td>1000 64MB</td>
<td>x10 D[31:26] R/W, D[25:0] =&gt; '0'</td>
</tr>
<tr>
<td>1001 128MB</td>
<td>x10 D[31:27] R/W, D[26:0] =&gt; '0'</td>
</tr>
<tr>
<td>1010 256MB</td>
<td>x10 D[31:28] R/W, D[27:0] =&gt; '0'</td>
</tr>
</tbody>
</table>
Register Index : 0C3h-0C0h
Register Name : GTLB Control Register
Default Value : 00000000h
Attribute : Read/Write
Size : 32 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-20 (000h)</td>
<td>NLVM_TOP[31-20]</td>
</tr>
<tr>
<td></td>
<td>These bits set the top address of the NLVM (Non-Local Video Memory) region</td>
</tr>
<tr>
<td></td>
<td>bit : 31 30 ..... 21 20</td>
</tr>
<tr>
<td></td>
<td>NVLM_TOP Address : 31 30 ..... 21 20</td>
</tr>
<tr>
<td></td>
<td>The address is from A[31] to A[20].</td>
</tr>
<tr>
<td></td>
<td>NLVM_TOP[31-20] must be greater than NLVM_BASE[31-20] for meaningful memory region definition.</td>
</tr>
<tr>
<td>19-8 (000h)</td>
<td>NLVM_BASE[31-20]</td>
</tr>
<tr>
<td></td>
<td>These bits set the bottom address of the NLVM region</td>
</tr>
<tr>
<td></td>
<td>bit : 19 18 ..... 9 8</td>
</tr>
<tr>
<td></td>
<td>NVLM_BASE Address : 31 30 ..... 21 20</td>
</tr>
<tr>
<td></td>
<td>The address is from A[31] to A[20].</td>
</tr>
<tr>
<td></td>
<td>NLVM_BASE[31-20] must be less than NLVM_TOP[31-20] for meaningful memory region definition.</td>
</tr>
<tr>
<td>7(1)</td>
<td>GART Table enable control</td>
</tr>
<tr>
<td></td>
<td>0 : Enable, 1 : Disable</td>
</tr>
<tr>
<td></td>
<td>This bit controls the enable/disable of the GART maintenance.</td>
</tr>
<tr>
<td>4(1)</td>
<td>GART Table size</td>
</tr>
<tr>
<td></td>
<td>0 : 32 entries, 4-sector associate</td>
</tr>
<tr>
<td></td>
<td>1 : 64 entries, 8-sector associate</td>
</tr>
<tr>
<td></td>
<td>This bit controls the GART size. There are 2 options :</td>
</tr>
<tr>
<td></td>
<td>(1) 32 entries and 4-sector associate</td>
</tr>
<tr>
<td></td>
<td>(2) 64 entries and 8-sector associate</td>
</tr>
<tr>
<td></td>
<td>Set this bit to ‘1’ is recommended to get the most hit rate.</td>
</tr>
<tr>
<td>6-5,3-0 (0)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
Register Index: 0DFh-0D4h, 0CFh-0CAh, 0C7h-0C4h
Register Name: Reserved Registers
Default Value: 00h
Attribute: Read Only

Register Index: 0C8h
Register Name: AGP Control Register I
Default Value: BFh
Attribute: Read/Write

<table>
<thead>
<tr>
<th>Bit no.</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7(1)   | Buffer Depth selection for AGP read data buffer  
0 : 16 QW, 1 : 32 QW  
This bit selects the AGP read data buffer depth. Choosing 32 QW is recommended. |
| 6-4(011) | The available space of AGP read data buffer for asserting an AGP request to memory  
000 : 0 QW available  
001 : 4 QW available  
010 : 8 QW available  
011 : 12 QW available  
100 : 16 QW available  
101 : 20 QW available  
110 : 24 QW available  
111 : 28 QW available  
These bits decide when to assert the AGP request to DRAM. If the buffer available space is greater than the setting, AGP request will issue to DRAM. For example, if setting these bits to '011', the buffer will begin to issue AGP request to DRAM when the buffer empty space is more than 12 Qwords. |
| 3(0)   | Enable to lower the LPR/HPR dequeue priority when AGP read data buffer is full.  
0 : disable, 1 : enable |
| 2(0)   | Enable to upgrade the LPR/HPR dequeue priority when AGP write data buffer is full.  
0 :disable, 1 : enable |
| 1-0(11) | Queue depth selection of AGP request queue  
00 : 8, 01 : 16  
10 : 24, 11 : 32 |
These two bits select the AGP request queue depth. Set to 32-queue depths is recommended.
Register Index : 0C9h  
Register Name : AGP Control Register II  
Default Value : 0Ah  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (00)   | Output delay control of AD_STB[1:0]  
            | 00 : Default (The default value is 3.5ns)  
            | 01 : Default - 1 ns  
            | 10 : Default + 1 ns  
            | 11 : AD_STB[1:0] output is generated by 133 MHz clock (Double of the AGP clock : GCLKIN). These two bits select the output delay of AD_STB[1:0]. The default delay is 3.5 ns. |
| 5 (0)      | Flush Host to PCI-66 write command if it was asserted before a FLUSH command  
            | 0 : Enable  
            | 1 : Disable  
            | If set to ENABLE, the Host to PCI_66 write buffer will be flushed before a FLUSH command |
| 4 (0)      | Delay enqueue LWT command when Fence is occurring until the command before fence is dequeue  
            | 0 : Enable  
            | 1 : Disable  
            | IF set to ENABLE, system will delay the LWT command enqueue until those commands before fence are dequeued. |
| 3 (1)      | Fast assertion of read request  
            | 0 : Disable  
            | 1 : Enable  
            | If set to ENABLE, system will issue the read request immediately. |
| 2-0 (010)  | The threshold QW number for AGP read data buffer to assert an AGP read request on AGP BUS  
            | 000 : 0 QW available  
            | 001 : 4 QW available  
            | 010 : 8 QW available  
<pre><code>        | 011 : 12 QW available |
</code></pre>
<table>
<thead>
<tr>
<th>100</th>
<th>16 QW available</th>
</tr>
</thead>
<tbody>
<tr>
<td>101</td>
<td>20 QW available</td>
</tr>
<tr>
<td>110</td>
<td>24 QW available</td>
</tr>
<tr>
<td>111</td>
<td>28 QW available</td>
</tr>
</tbody>
</table>

The threshold length is 4QW when 2x transfer is selected, else 2QW when 1x transfer is selected.

Register Index: **0D3-0D0h**

Register Name: **L1/L2 Cache Flush Control**

Default Value: **00h**

Attribute: Read/Write

Size: 32 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-12 (00000h)</td>
<td>Cache flush page address [31-12]. These bits control the cache flush page register. Bits 31-12 correspond to address 31-12.</td>
</tr>
<tr>
<td>11-9 (0h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>8 (0)</td>
<td>Cache flush enable – L1/L2_FLUSH</td>
</tr>
<tr>
<td>0 : Disable Flush or Finish Flush</td>
<td></td>
</tr>
<tr>
<td>1 : Enable Flush</td>
<td></td>
</tr>
</tbody>
</table>

When this bit is enabled, the L1/L2 cache region indicated by Cache Flush page register (index 0D3h-0D0h bit 31-12) will be flushed to DRAM by hardware directly. When the hardware finishes the flush process, this bit will be cleared to 0.

<table>
<thead>
<tr>
<th>7-0 (00h)</th>
<th>Reserved</th>
</tr>
</thead>
</table>
4.6 Green Function Register

Register Index : 0E0h  
Register Name : **Power Management Capability Identifier Register**  
Default Value : 01h  
Attribute : Locked Read/Write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (01h)</td>
<td>Capability Identifier. The capability identifier, when read by system software as 01h indicates that the data structure currently being pointed to is the PCI Power management data structure. The register’s default is read only, when index 90h bit 5 = 1, this register can read/write.</td>
</tr>
</tbody>
</table>

Register Index : 0E1h  
Register Name : **Power Management Next Item Pointer Register**  
Default Value : 00h  
Attribute : Locked Read/Write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-0 (00h)  | Next Item Pointer  
This field provides an offset into the PCI function’s PCI configuration space pointing to the location of next item in the function’s capability list. If there are no additional items in the capability list, this register is set to 00h. The register default is read only. When index 90h bit 5 = 1, this register can read/write. |

Register Index : 0E3h-0E2h  
Register Name : **Power Management Capabilities Register**  
Default Value : 0000h  
Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1, this register can read/write.
<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-11</td>
<td>PME_Support</td>
</tr>
<tr>
<td>XXXX1</td>
<td>PMEJ can be asserted from D0</td>
</tr>
<tr>
<td>XXX1X</td>
<td>PMEJ can be asserted from D1</td>
</tr>
<tr>
<td>XX1XX</td>
<td>PMEJ can be asserted from D2</td>
</tr>
<tr>
<td>X1XXX</td>
<td>PMEJ can be asserted from D3 hot</td>
</tr>
<tr>
<td>1XXXX</td>
<td>PMEJ can be asserted from D3 cold</td>
</tr>
<tr>
<td></td>
<td>These five bits field indicate the power state in which the function may</td>
</tr>
<tr>
<td></td>
<td>assert PMEJ. A value of ‘0’ for any bit indicates that the function is not</td>
</tr>
<tr>
<td></td>
<td>capable of asserting the PMEJ signal while in that power state.</td>
</tr>
<tr>
<td>10</td>
<td>D2_Support</td>
</tr>
<tr>
<td>0</td>
<td>Do not support D2</td>
</tr>
<tr>
<td>1</td>
<td>Support D2</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to ‘1’, M1541 supports the D2 power management state.</td>
</tr>
<tr>
<td>9</td>
<td>D1_Support</td>
</tr>
<tr>
<td>0</td>
<td>Do not support D1</td>
</tr>
<tr>
<td>1</td>
<td>Support D1</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to ‘1’, M1541 supports the D1 power management state.</td>
</tr>
<tr>
<td>8-6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Device Specific Initialization (DSI)</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to ‘1’, it indicates the function requires a device</td>
</tr>
<tr>
<td></td>
<td>specific initialization sequence following transaction to the D0 un-initialized state.</td>
</tr>
<tr>
<td>4</td>
<td>Auxiliary Power Source</td>
</tr>
<tr>
<td></td>
<td>This bit is only meaningful if the bit 15 ( PMEJ can be asserted from D3</td>
</tr>
<tr>
<td></td>
<td>cold ) = 1</td>
</tr>
<tr>
<td>0</td>
<td>Supply its own auxiliary power source</td>
</tr>
<tr>
<td>1</td>
<td>Support PMEJ in D3 cold requires auxiliary power supplied by the system by</td>
</tr>
<tr>
<td></td>
<td>way of proprietary delivery vehicle.</td>
</tr>
<tr>
<td>3</td>
<td>PME clock</td>
</tr>
<tr>
<td>0</td>
<td>No PCI clock is required for M1541 to generate PMEJ.</td>
</tr>
<tr>
<td>1</td>
<td>M1541 relies on the presence of the PCI clock for PMEJ operation.</td>
</tr>
<tr>
<td>2-0</td>
<td>Version of PCI power management interface specification</td>
</tr>
<tr>
<td></td>
<td>The version support is V1.0 now.</td>
</tr>
</tbody>
</table>
Register Index : 0E5h-0E4h
Register Name : Power Management Control and Status Register
Default Value : 0000h
Attribute : Locked Read/write. Some bits can read/write, some bits are Locked read/write. These bits marked with Locked read/write default is read only, when index 90h bit 5 = 1, these bits can read/write.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 (0)</td>
<td>PME_Status (Read/Write_clear). This bit is set when the function would normally assert the PMEJ signal independent of the state of the PME_EN (index 0E4h bit 8) 0 : The function does not support PMEJ generation from D3 cold state. 1 : Indeterminate at time of initial OS boot if function supports PMEJ from D3 cold state. Write 1 to this bit will clear this bit to 0 and cause the M1541 to stop asserting a PMEJ (if enabled). Writing a “0” has no effect.</td>
</tr>
<tr>
<td>14-13 (00)</td>
<td>Data_scale (Locked read/write) These two-bit field indicates the scaling factor to be used when interpreting the value of the DATA register (index 0e7h). The value &amp; meaning of this field will vary depending on which data value has been selected bit[12-9] (DATA_select) field.</td>
</tr>
<tr>
<td>12-9 (0h)</td>
<td>Data_select (read/write) These four bits are used to select which data is to be reported through DATA register (index 0E7h) and data scale (bit[14-13]) field.</td>
</tr>
<tr>
<td>8 (0)</td>
<td>PME_EN (read/write) 0 : PMEJ assertion is disable 1 : Enable the function to assert PMEJ</td>
</tr>
<tr>
<td>7-2 (00h)</td>
<td>Reserved (Locked read/write)</td>
</tr>
<tr>
<td>1-0 (00)</td>
<td>Power State (read/write) 00 : D0 01 : D1 10 : D2 11 : D3 hot These two bits are used to determine the current power state of a function and to set the function into a new power state. If software attempts to write an unsupported, optional state to this field. The write operation must complete normal on the bus, however the data is discarded and no state change occurs.</td>
</tr>
</tbody>
</table>
Register Index : 0E6h
Register Name : PMCSR PCI-to-PCI Bridge Support Extensions
Default Value : 00h
Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Bus Power/Clock Control Enable</td>
</tr>
<tr>
<td></td>
<td>0 : Bus power/clock control mechanism has been disabled</td>
</tr>
<tr>
<td></td>
<td>1 : Bus power/clock control mechanism has been enabled</td>
</tr>
<tr>
<td></td>
<td>When the Bus Power/Clock control mechanism is disabled, the bridge’s PMCSR Power State field cannot be used by the system software to control the power or clock of the bridge’s secondary bus.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>B2/B3 support for D3 hot</td>
</tr>
<tr>
<td></td>
<td>0 : The bridge function is programmed to D3 hot, its secondary bus’ will have its power removed (B3)</td>
</tr>
<tr>
<td></td>
<td>1 : The bridge function is programmed to D3 hot, its secondary bus’ PCI clock will be stopped (B2)</td>
</tr>
<tr>
<td></td>
<td>The state of this bit determines the action that is to occur as a direct result of programming the function to D3 hot.</td>
</tr>
<tr>
<td></td>
<td>This bit is only meaningful if bit 7=1 (Bus Power/Clock control enable)</td>
</tr>
<tr>
<td>5-0 (00h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Register Index : 0E7h
Register Name : Data Register
Default Value : 00h
Attribute : Locked Read/Write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Data[7-0]. This register is used to report the state dependent data requested by the Data_Select (index 0E4h bit[12-9] ) field. The value of this register is scaled by the value reported by the Data_Scale (index 0E4h bit[12-9]) field.</td>
</tr>
</tbody>
</table>
Register Index: 0E9h-0E8h
Register Name: BASE ADDRESS OF ACPI PM2_CNTL PORT

Locked read/write, control bit is index 90h bit 2. If index 90h bit2 = ‘1’ then enable write this register.

Default Value: 0000h
Attribute: Locked Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-0 (0000h)</td>
<td>Base Address of ACPI PM2_CNTL Port. This 16-bit register is programmed as the I/O base address of ACPI PM2_CNTL Port. The default value is 0000h, and can be programmed by software to move the base address of ACPI PM2_CNTL Port.</td>
</tr>
</tbody>
</table>
Register Index: 0EAh
Register Name: PM2C - ACPI PM2_CNTL function
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>5-V Suspend Refresh period</td>
</tr>
<tr>
<td>00</td>
<td>15 us</td>
</tr>
<tr>
<td>01</td>
<td>30 us</td>
</tr>
<tr>
<td>10</td>
<td>60 us</td>
</tr>
<tr>
<td>11</td>
<td>120 us</td>
</tr>
<tr>
<td></td>
<td>These 2 bits define the DRAM suspend refresh period when M1541 enters the suspend mode.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>Reserved</td>
</tr>
<tr>
<td>3 (0)</td>
<td>CLKRUNJ/SERRJ Function Select</td>
</tr>
<tr>
<td>0</td>
<td>SERRJ</td>
</tr>
<tr>
<td>1</td>
<td>CLKRUNJ</td>
</tr>
<tr>
<td></td>
<td>This bit is used to define the CLKRUNJ/SERRJ pin function. When this bit is programmed to '0', SERRJ function is selected. In this configuration, M1541 can support DRAM ECC/PARITY and the PCI Parity check error report. When this bit is programmed to '1', CLKRUNJ function is selected. M1541 can support Mobile PCI Specification 2.0 CLKRUNJ function through this configuration.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Host to PCI IO Cycle Trap Support</td>
</tr>
<tr>
<td>0</td>
<td>normal</td>
</tr>
<tr>
<td>1</td>
<td>Delay BRDYJ for 1 CPU CLK</td>
</tr>
<tr>
<td></td>
<td>M1541 will delay all the PCI IO cycle by one CPU clock when this bit is set to ‘1’. The BRDYJ to CPU will delay one CPU clock compared to normal IO access. This is to make sure CPU can IO trap this IO instruction. So after SMM mode, an IO restart can function correctly.</td>
</tr>
</tbody>
</table>
1-0 (00) | ACPI PM2_CNTL FUNCTION
00 : Disable
01 : Enable, monitor the IO port access defined by index 0E9h-0E8h
10 : Enable, receive the IO port access defined by index 0E9h-0E8h and NOT transfer access to PCI bus
11 : Reserved

These two bits define the way that M1541 responds to the ACPI PM2_CNTL port write.
M1541 has implemented the ACPI PM2_CNTL I/O Port, and the address is defined by Index 71h-70h. When these two bits are programmed to be '00', M1541 will disable the ACPI PM2_CNTL I/O Port decode, and pass the I/O cycle to PCI bus. When these two bits are programmed to be '01', M1541 will snoop the ACPI PM2_CNTL I/O Port write data, and pass the I/O cycle to PCI bus. In this setting, M1541 just do the snoop write, and all the cycle will be terminated by M1533/M1543. When these two bits are programmed to be '10', M1541 will terminate the ACPI PM2_CNTL I/O Port access, and will not pass the I/O cycle to PCI bus.
Register Index : 0EBh
Register Name : GCKCTL - Gated Clock Control Register
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Host interface Clock Control</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>1 : Enable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the Host CPU interface clock. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no Host activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>DRAM Sequencing, DRAM Controller clock turn off in MD idle cycle</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal clock regarding the Memory Data Bus. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal DRAM controller clock when there is no Memory Data Bus activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>DMWBF/L2 Controller clock turn off in CPU idle cycle</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal DRAM controller clock regarding the DRAM &amp; Cache Controller. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal DRAM posted write buffer controller and L2 cache controller clock when there is no Host Bus activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>AGP to Host Buffer clock control</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>1 : Enable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal clock regarding the AGP to Host Buffer. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no AGP master activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Host to PCI_66 Buffer clock control</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Gated Clock</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>---</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>Enable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal clock regarding the Host to PCI_66 Interface Logic. When this bit is programmed to be ‘0’, the clock never stops. When this bit is programmed to be ‘1’, M1541 will automatically stop the internal clock when there is no Host to PCI_66 activity. This bit is suggested to be set to ‘0’ in desktop application; to be ‘1’ in notebook application to save more power.</td>
</tr>
<tr>
<td>2</td>
<td>PCI_66 to Host Buffer clock control</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>1 : Enable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal clock regarding the PCI_66 to Host Buffer. When this bit is programmed to be ‘0’, the clock never stops. When this bit is programmed to be ‘1’, M1541 will automatically stop the internal clock when there is no PCI_66 master activity. This bit is suggested to be set to ‘0’ in desktop application; to be ‘1’ in notebook application to save more power.</td>
</tr>
<tr>
<td>1</td>
<td>Host to PCI interface logic clock control</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>1 : Enable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal clock regarding the Host to PCI Interface Logic. When this bit is programmed to be ‘0’, the clock never stops. When this bit is programmed to be ‘1’, M1541 will automatically stop the internal clock when there is no Host to PCI activity. This bit is suggested to be set to ‘0’ in desktop application; to be ‘1’ in notebook application to save more power.</td>
</tr>
<tr>
<td>0</td>
<td>PCI to Host Buffer Clock Control</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>1 : Enable Gated Clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal clock regarding the PCI to Host Buffer. When this bit is programmed to be ‘0’, the clock never stops. When this bit is programmed to be ‘1’, M1541 will automatically stop the internal clock when there is no PCI master activity. This bit is suggested to be set to ‘0’ in desktop application; to be ‘1’ in notebook application to save more power.</td>
</tr>
</tbody>
</table>
Register Index: 0ECh
Register Name: POD - Programmable Output Driving Strength
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>Reserved</td>
</tr>
<tr>
<td>5 (0)</td>
<td>MAA[1:0] Driving Capability Select.</td>
</tr>
<tr>
<td></td>
<td>0 : 32 mA</td>
</tr>
<tr>
<td></td>
<td>1 : 16 mA</td>
</tr>
<tr>
<td></td>
<td>This bit controls the strength of the output buffers driving the MAA[1:0] pins.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>MA[14:2] Driving Capability Select.</td>
</tr>
<tr>
<td></td>
<td>0 : 32 mA</td>
</tr>
<tr>
<td></td>
<td>1 : 16 mA</td>
</tr>
<tr>
<td></td>
<td>This bit controls the strength of the output buffers driving the MA[11:2] pins.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>CASJ[7:0] Driving Capability Select.</td>
</tr>
<tr>
<td></td>
<td>0 : 24 mA</td>
</tr>
<tr>
<td></td>
<td>1 : 12 mA</td>
</tr>
<tr>
<td></td>
<td>This bit controls the strength of the output buffers driving the CASJ[7:0] pins.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>RASJ[7:0] Driving Capability Select.</td>
</tr>
<tr>
<td></td>
<td>0 : 24 mA</td>
</tr>
<tr>
<td></td>
<td>1 : 12 mA</td>
</tr>
<tr>
<td></td>
<td>This bit controls the strength of the output buffers driving the RASJ[7:0]</td>
</tr>
<tr>
<td>1 (0)</td>
<td>MD[63:0],MPD[7:0] Driving Capability Select.</td>
</tr>
<tr>
<td></td>
<td>0 : 16 mA</td>
</tr>
<tr>
<td></td>
<td>1 : 10 mA</td>
</tr>
<tr>
<td></td>
<td>This bit controls the strength of the output buffers driving the MD[63:0], MPD[7:0] pins.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>HD[63:0] Driving Capability Select.</td>
</tr>
<tr>
<td></td>
<td>0 : 16 mA</td>
</tr>
<tr>
<td></td>
<td>1 : 12 mA</td>
</tr>
<tr>
<td></td>
<td>This bit controls the strength of the output buffers driving the HD[63:0] pins.</td>
</tr>
</tbody>
</table>
Register Index : 0EDh
Register Name : Hardware setting register
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (000)</td>
<td>HOST bus frequency (read only)</td>
</tr>
<tr>
<td></td>
<td>000 : Reserved</td>
</tr>
<tr>
<td></td>
<td>001 : 60MHz</td>
</tr>
<tr>
<td></td>
<td>010 : 66MHz</td>
</tr>
<tr>
<td></td>
<td>011 : 75MHz</td>
</tr>
<tr>
<td></td>
<td>100 : 83MHz</td>
</tr>
<tr>
<td></td>
<td>101 : 90MHz</td>
</tr>
<tr>
<td></td>
<td>110 : 100 MHz</td>
</tr>
<tr>
<td></td>
<td>111 : Reserved</td>
</tr>
<tr>
<td>(HA[31:29] as hardware setting pin). These three bits are hardware strobe from HA[31:29] to indicate the CPU bus frequency for BIOS POST procedure reference.</td>
<td></td>
</tr>
<tr>
<td>4 (0)</td>
<td>CPU clock PLL enable</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td>(HA[28] as hardware setting pin). This bit is hardware strobe from HA[28] to enable the CPU PLL circuit for 100MHz clock compensation. Locked read/write, controlled by index 90h bit 4.</td>
<td></td>
</tr>
<tr>
<td>3-1 (000)</td>
<td>CPU CLK compensate select</td>
</tr>
<tr>
<td></td>
<td>000 : No compensate</td>
</tr>
<tr>
<td></td>
<td>001 : 1 buffer</td>
</tr>
<tr>
<td></td>
<td>010 : 2 buffers</td>
</tr>
<tr>
<td></td>
<td>011 : 3 buffers</td>
</tr>
<tr>
<td></td>
<td>100 : 4 buffers</td>
</tr>
<tr>
<td></td>
<td>101 : 5 buffers</td>
</tr>
<tr>
<td></td>
<td>110 : 6 buffers</td>
</tr>
<tr>
<td></td>
<td>111 : 7 buffers</td>
</tr>
<tr>
<td>(HA[27-25] as hardware setting pin) These three bits are hardware strobe from HA[27-25] to enable the CPU PLL compensate circuit for 100MHz clock compensation. Locked read/write, controlled by index 90h bit 4.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CPU CLK PLL internal test select</td>
</tr>
<tr>
<td>---</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>0 (0)</td>
<td>For M1541 A1 C and earlier version</td>
</tr>
<tr>
<td>0</td>
<td>Normal</td>
</tr>
<tr>
<td>1</td>
<td>Test</td>
</tr>
<tr>
<td>(HA[24] as hardware setting pin)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>CPU CLK compensate select</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-2 (00)</td>
<td>For M1541 A1 D and later version</td>
</tr>
<tr>
<td>00</td>
<td>No compensate</td>
</tr>
<tr>
<td>01</td>
<td>2 buffer</td>
</tr>
<tr>
<td>10</td>
<td>4 buffers</td>
</tr>
<tr>
<td>11</td>
<td>6 buffers</td>
</tr>
<tr>
<td>(HA[27-26] as hardware setting pin). These three bits are hardware strobe from HA[27-26] to enable the CPU PLL compensate circuit for 100MHz clock compensation. Locked read/write, controlled by index 90h bit 4.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>HD output clock select</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-0 (00)</td>
<td>For M1541 A1 D and later version</td>
</tr>
<tr>
<td>00</td>
<td>default</td>
</tr>
<tr>
<td>01</td>
<td>ahead 1 ns</td>
</tr>
<tr>
<td>10</td>
<td>ahead 2 ns</td>
</tr>
<tr>
<td>11</td>
<td>ahead 3 ns</td>
</tr>
<tr>
<td>These two bits control the CPU interface HD data bus output synchronization clock (HA[25-24] as hardware setting pin).</td>
<td></td>
</tr>
</tbody>
</table>
**Register Index:** 0EEh  
**Register Name:** Miscellaneous-1  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>MESI clock select</td>
</tr>
<tr>
<td></td>
<td>For M1541 A1 C and earlier versions</td>
</tr>
<tr>
<td></td>
<td>00 : HCLK_IN, Host clock input</td>
</tr>
<tr>
<td></td>
<td>01 : ADV_CLK, Advance clock</td>
</tr>
<tr>
<td></td>
<td>10 : Ahead 2 ns</td>
</tr>
<tr>
<td></td>
<td>11 : Ahead 3 ns</td>
</tr>
<tr>
<td></td>
<td>These two bits select which clock source for internal TAG/MESI SRAM usage.</td>
</tr>
<tr>
<td>5-4 (00)</td>
<td>MESI clock select</td>
</tr>
<tr>
<td></td>
<td>For M1541 A1 D and later versions</td>
</tr>
<tr>
<td></td>
<td>00 : HCLK_IN, Host clock input</td>
</tr>
<tr>
<td></td>
<td>01 : Ahead 1 ns</td>
</tr>
<tr>
<td></td>
<td>10 : Ahead 2 ns</td>
</tr>
<tr>
<td></td>
<td>11 : Ahead 3 ns</td>
</tr>
<tr>
<td></td>
<td>These two bits select which clock source for internal TAG/MESI SRAM usage.</td>
</tr>
<tr>
<td>3-2 (00)</td>
<td>SDRAM memory write Data Ahead clock select</td>
</tr>
<tr>
<td></td>
<td>00 : Ahead 4 ns</td>
</tr>
<tr>
<td></td>
<td>01 : Ahead 1 ns</td>
</tr>
<tr>
<td></td>
<td>10 : Ahead 2 ns</td>
</tr>
<tr>
<td></td>
<td>11 : Ahead 3 ns</td>
</tr>
<tr>
<td></td>
<td>When index 0EEh bit1 (100Mhz SDRAM memory write Data ahead clock select use internal ahead clock) =0, these two bits define how much the advanced clock for DMW circuit leads the M1541 internal host clock.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>100Mhz SDRAM memory write Data ahead clock select</td>
</tr>
<tr>
<td></td>
<td>For M1541 A1 C and earlier version</td>
</tr>
<tr>
<td></td>
<td>0 : External clock</td>
</tr>
<tr>
<td></td>
<td>1 : Internal Ahead clock</td>
</tr>
<tr>
<td></td>
<td>This bit is used for selecting the DRAM memory write circuit clock. When this bit is set to ‘0’, the DRAM memory write circuit will use the clock which is input from DPLL10 instead of the internal PLL. The data and control signal sent to DRAM will use DPLL11</td>
</tr>
<tr>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td><strong>1 (0)</strong></td>
<td>100Mhz SDRAM memory write Data ahead clock select</td>
</tr>
<tr>
<td>For M1541 A1</td>
<td>0 : ahead clock</td>
</tr>
<tr>
<td>D and later version</td>
<td>1 : clock test mode</td>
</tr>
<tr>
<td></td>
<td>This bit is used for selecting the DRAM memory write circuit clock. When this bit is set to ‘0’, the DRAM memory write circuit will use the ahead clock. The data and control signal sent to DRAM will use ahead clock as clock source. When set to 1, the circuit will be in clock test mode for chip testing only For D and later versions, this bit should set to ‘0’</td>
</tr>
<tr>
<td><strong>0 (0)</strong></td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register Index : 0EFh
Register Name : Miscellaneous-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

When SDRAM PLL is set to Digital PLL, this index should be set to 0A3h (recommended)
When SDRAM PLL is set to Analog PLL, this index should be set to 0A0h
When SDRAM PLL is set to disable, this index should be set to 00h

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>SDRAM Memory Read PLL reference clock select</td>
</tr>
<tr>
<td></td>
<td>00 : HCLK from output of Host PLL</td>
</tr>
<tr>
<td></td>
<td>01 : HCLK from output of Host PLL + 1 buffer</td>
</tr>
<tr>
<td></td>
<td>10 : Reference HCLK</td>
</tr>
<tr>
<td></td>
<td>11 : Reference HCLK + 1 buffer</td>
</tr>
<tr>
<td></td>
<td>These two bits select the reference clock source of PLL for SDRAM.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>SDRAM Memory Read PLL enable</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, the SDRAM controller will use internal Digital or Analog PLL for the automatic adjustment mechanism. The Digital or Analog PLL will be decided by bit 0.</td>
</tr>
<tr>
<td>4-2 (000)</td>
<td>DRAM Memory Read PLL compensate</td>
</tr>
<tr>
<td></td>
<td>000 : 0 buffer, no compensation</td>
</tr>
<tr>
<td></td>
<td>001 : 1 buffer</td>
</tr>
<tr>
<td></td>
<td>010 : 2 buffers</td>
</tr>
<tr>
<td></td>
<td>011 : 3 buffers</td>
</tr>
<tr>
<td></td>
<td>100 : 4 buffers</td>
</tr>
<tr>
<td></td>
<td>101 : 5 buffers</td>
</tr>
<tr>
<td></td>
<td>110 : 6 buffers</td>
</tr>
<tr>
<td></td>
<td>111 : 7 buffers</td>
</tr>
<tr>
<td></td>
<td>These three bits control the compensation of SDRAM clock source of PLL.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>SDRAM DPLL Auto enable</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Auto</td>
</tr>
<tr>
<td></td>
<td>If this bit is enable, the SDRAM controller will use internal Digital PLL for the automatic adjustment</td>
</tr>
</tbody>
</table>
mechanism.

<table>
<thead>
<tr>
<th>0 (0)</th>
<th>SDRAM Analog PLL/DPLL select</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 : Select Analog PLL</td>
</tr>
<tr>
<td></td>
<td>1 : Select Digital PLL</td>
</tr>
</tbody>
</table>
This bit is used to select the SDRAM controller clock source.

<table>
<thead>
<tr>
<th>Register Index</th>
<th>0F3h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Name</td>
<td>Predict the next SDRAM Control Signal</td>
</tr>
<tr>
<td>Default Value</td>
<td>00h</td>
</tr>
<tr>
<td>Attribute</td>
<td>Read/Write</td>
</tr>
<tr>
<td>Size</td>
<td>8 bits</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 (0)</td>
<td>Predict the next SDRAM control signal</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Index</th>
<th>0F5h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Name</td>
<td>DMROPL Status Register</td>
</tr>
<tr>
<td>Default Value</td>
<td>00h</td>
</tr>
<tr>
<td>Attribute</td>
<td>Read/Write</td>
</tr>
<tr>
<td>Size</td>
<td>8 bits</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>SDRAM DPLL Status (Read Only)</td>
</tr>
<tr>
<td></td>
<td>0 : Feedback clock lag reference clock.</td>
</tr>
<tr>
<td></td>
<td>1 : Feedback clock ahead reference clock.</td>
</tr>
</tbody>
</table>
This bit indicates the status of Digital PLL for M1541 SDRAM clock source.

<table>
<thead>
<tr>
<th>6-0 (00h)</th>
<th>SDRAM DPLL counter (Read/Write)</th>
</tr>
</thead>
<tbody>
<tr>
<td>These bits indicate the status of Digital PLL for M1541 SDRAM clock source. Writing to these bits will control the DPLL delay stage and thus control the output clock phase. Reading data from these bits indicate current delay stage.</td>
<td></td>
</tr>
</tbody>
</table>
Register Index: 0F6h
Register Name: GDPL Status register
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>AGP DPLL status (Read only)</td>
</tr>
<tr>
<td></td>
<td>0: Feedback clock lag reference clock.</td>
</tr>
<tr>
<td></td>
<td>1: Feedback clock ahead reference clock.</td>
</tr>
<tr>
<td></td>
<td>This bit indicates the status of Digital PLL for M1541 internal AGP source.</td>
</tr>
<tr>
<td>6-0 (00h)</td>
<td>AGP DPLL counter (Read/Write)</td>
</tr>
<tr>
<td></td>
<td>These bits indicate the status of Digital PLL for M1541 internal AGP clock source. Writing to these bits will control the DPLL delay stage and thus control the output clock phase. Reading data from these bits indicate current delay stage.</td>
</tr>
</tbody>
</table>

Register Index: 0F7h
Register Name: GCLK PLL Control Register
Default Value: 00h
Attribute: Read/write
Size: 8 bits

When AGP PLL is set to Digital PLL, this index should be set to 043h (recommended)
When AGP PLL is set to Analog PLL, this index should be set to 01h
When AGP PLL is set to disable, this index should be set to 00h

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Reserved</td>
</tr>
<tr>
<td>6 (0)</td>
<td>GCLK DPLL auto enable</td>
</tr>
<tr>
<td></td>
<td>0: disable</td>
</tr>
<tr>
<td></td>
<td>1: auto enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is set to ‘1’, the Digital PLL for AGP clock will adjust automatically.</td>
</tr>
<tr>
<td>5-2 (00)</td>
<td>Reserved</td>
</tr>
<tr>
<td>1 (0)</td>
<td>GCLK PLL/DPLL select</td>
</tr>
<tr>
<td></td>
<td>0: Analog PLL</td>
</tr>
<tr>
<td></td>
<td>1: Digital PLL</td>
</tr>
<tr>
<td></td>
<td>This bit selects the Digital or Analog version of PLL for M1541 internal AGP clock.</td>
</tr>
<tr>
<td>Bit Number</td>
<td>Bit Function</td>
</tr>
<tr>
<td>------------</td>
<td>------------------------------------------------</td>
</tr>
<tr>
<td>7-1 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>PCI Master Arbiter Function.</td>
</tr>
<tr>
<td></td>
<td>0 : enable.</td>
</tr>
<tr>
<td></td>
<td>1 : disable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the PCI Master Arbiter Function. When this bit is set to '1', the M1541 internal PCI master arbiter will be disabled, and the M1541 on behalf of the CPU host is the only one master in the system. In normal operation, the bit must be set to '0'.</td>
</tr>
</tbody>
</table>
4.8 M5243 Configuration Space

M1541 built-in PCI-to-PCI bridge M5243 PCI_66 Configuration Space -- Device 1

The M1541 will respond to PCI-to-PCI bridge configuration access for which AD12=IDSEL is high during the address phase.

The PCI to PCI bridge is called M5243 and is a Device -1 device.

Register Index 01h-00h
Register Name VID - Vendor Identification Register
Default Value 10B9h
Attribute Read Only
Size 16 bits
Description This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index 03h-02h
Register Name DID - Device Identification Register
Default Value 5243h
Attribute Locked Read/Write
Size 16 bits
Description This is a 16-bit value. Default is 5243h. It is controlled by index 90h bit 3(P2P_BRI_DEV_ID_EN), when the bit = ‘1’ then enable write this port

Register Index 05h-04h
Register Name COM - Command Register
Default Value 0006h
Attribute Read/Write
Size 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-9 (000h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>8 (0)</td>
<td>Enable the GSERRJ Output Driver.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
</tbody>
</table>
GSERRJ uses an o/d (Open Drain) pad in M5243. The motherboard design should use a pull-up resistor (2.2KΩ) to keep this pin logic high. When the PCI_66 Parity check is enabled and an error is found, the M5243 will drive GSERRJ low to M1533/ M1543 to generate NMI when this bit is enabled. Disabling the GSERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 by BIOS in systems that wish to report Parity error.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Enable Address/Data Stepping. M5243 does not support this feature. Write to this bit has no effect.</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>Respond to Parity Errors.</td>
<td>0 : Disable. 1 : Enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The M5243 will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M5243 will assert GSERRJ and set the Parity Error Bit in the DS register.</td>
</tr>
<tr>
<td>5</td>
<td>Enable VGA Palette Snooping.</td>
<td>0 : No broadcasting for I/O write 3C6H, 3C8H, 3C9H 1 : Broadcasting for I/O write 3C6H, 3C8H, 3C9H</td>
</tr>
<tr>
<td>4</td>
<td>Enable Post Memory Write Command. M5243 does not support this feature. Write to this bit has no effect.</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>Enable Special Cycle. M5243 does not support this feature. Write to this bit has no effect.</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>Control to Act As a PCI Bus Master. M5243 does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect.</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>Enable Response to Memory Access. M5243 always accepts PCI master accesses to local memory.</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>Enable Response to I/O Access. M5243 responds to any PCI master I/O accesses.</td>
<td>0</td>
</tr>
</tbody>
</table>
Register Index: 07h-06h
Register Name: DS - PCI_66 Device Status Register
Default Value: 0400h
Attribute: Read Only, Read/Write Clear
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 (0)</td>
<td>Detected Parity Error. This bit is set by the M5243 whenever it detects a parity error in a PCI_66 transaction even if parity error handling is disabled (as controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.</td>
</tr>
<tr>
<td>14 (0)</td>
<td>Signaled System Error. The M5243 will set this bit whenever it asserts GSERRJ. Software can reset this bit to 0 by writing a 1 to it.</td>
</tr>
<tr>
<td>13 (0)</td>
<td>Received Master Abort. This bit is set by M5243 whenever it terminates a CPU to PCI_66 transaction with master abort. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>12 (0)</td>
<td>Received Target Abort. This bit is set by the M5243 whenever its initiated CPU to PCI_66 transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>11 (0)</td>
<td>Send Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M5243 never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.</td>
</tr>
</tbody>
</table>
| 10-9 (10)  | DEVSELJ Timing. Read Only
00 : Fast.
01 : Medium.
10 : Slow.
The M5243 timing for DEVSELJ assertion. Slow timing is selected.
The actual timing of DEVSELJ is medium |
| 8-5 (0h)   | Reserved |
| 4 (0h)     | CAP_LIST, read only
If write '1' to M5243 offset 90h bit 0 then this bit = '1'
If write '0' to M5243 offset 90h bit 0 then this bit = '0' |
| 3-0 (0h)   | Reserved |

Register Index: 08h
Register Name: RI - Revision ID Register
Default Value: 00h (A0 Stepping)
Attribute: Read Only
Size: 8 bits
Description: This register contains the version number of PCI_66 device. The value 00 means A0 stepping.
Register Index: 09h
Register Name: Reserved Registers
Default Value: 00h
Attribute: Read Only
Register Index: **0Ah**
Register Name: **SCC - Sub-Class Code Register**
Default Value: **04h : PCI to PCI Bridge**
Attribute: **Read Only**
Size: **8 bits**
Description: These registers contain the sub-Class Codes of the PCI_66.

Register Index: **0Bh**
Register Name: **CC - Class Code Register**
Default Value: **06h, Bridge device**
Attribute: **Read Only**
Size: **8 bits**
Description: These registers contain the Class Codes of the PCI_66.

Register Index: **0Ch**
Register Name: **Reserved Registers**
Default Value: **00h**
Attribute: **Read Only**

Register Index: **0Dh**
Register Name: **LT - PCI Latency Timer value**
Default Value: **20h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3 (04h)</td>
<td>Master Latency Timer Count Value. LT is used to control the amount of time the M5243, as a bus master, can burst data to the PCI_66 Bus. It can be used to guarantee a minimum amount of the system resources.</td>
</tr>
<tr>
<td>2-0 (0h)</td>
<td>Reserved. They are assumed to be 0 when determining the Count Value.</td>
</tr>
</tbody>
</table>

Register Index: **0Eh**
Register Name: **Head type**
Default Value: **01h**
Attribute: **Read only**
Size : 8 bits

Register Index : 0Fh-18h
Register Name : Reserved

Register Index : 19h
Register Name : Secondary Bus Number Register
Default Value : 01h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Bus Number assigned to the second bus of &quot;virtual&quot; PCI-to-PCI bridge</td>
</tr>
</tbody>
</table>
Register Index : **1Ah**  
Register Name : **Subordinate Bus Number Register**  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Bus Number for the subordinate bus that resides at the level below A.G.P. (Default &quot;00000000&quot;)</td>
</tr>
</tbody>
</table>

Register Index : **1Bh**  
Register Name : **Secondary Master Latency Timer value**  
Default Value : 20h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (20h)</td>
<td>Timer Value for Latency Counter</td>
</tr>
</tbody>
</table>

Register Index : **1Ch**  
Register Name : **I/O Base Address Register**  
Default Value : 0F0h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0fh)</td>
<td>Corresponds to A[15:12] of the I/O Base Address</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Register Index : **1Dh**  
Register Name : **I/O limit Address Register**  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits
<table>
<thead>
<tr>
<th>Address (00h)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Corresponds to A[15:12] of the I/O limit Address</td>
</tr>
<tr>
<td>3-0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register Index: **1Fh-1Eh**
Register Name: *Secondary PCI-PCI Status Register*
Default Value: 00h
Attribute: Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 (0)</td>
<td>Set when M5243 detects a parity error AGP.</td>
</tr>
<tr>
<td>14 (0)</td>
<td>Set when M5243 asserts GSERRJ.</td>
</tr>
<tr>
<td>13 (0)</td>
<td>Set when receives a Master Abort at CPU to AGP cycle.</td>
</tr>
<tr>
<td>12 (0)</td>
<td>Set when receives a Target Abort at CPU to AGP cycle.</td>
</tr>
<tr>
<td>11-0 (000h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Register Index: **21h-20h**
Register Name: *Memory Base Address Register*
Default Value: 0FFF0h
Attribute: Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-4 (0FFh)</td>
<td>Corresponds to A[31:20] of the CPU to AGP non-prefetchable memory Base Address</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Register Index: **23h-22h**
Register Name: *Memory Limit Address Register*
Default Value: 0000h
Attribute: Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-4 (000h)</td>
<td>Corresponds to A[31:20] of the CPU to AGP non-pre-fetchable memory Limit Address</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register Index : 25h-24h  
Register Name : Pre-fetchable Memory Base Address Register  
Default Value : 0FFF0h  
Attribute : Read/Write  
Size : 16 bits  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-4 (0fffh)</td>
<td>Corresponds to A[31:20] of the CPU to AGP Pre-fetchable memory Base Address</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Register Index : 27h-26h  
Register Name : Pre-fetchable Memory Limit Address Register  
Default Value : 0000h  
Attribute : Read/Write  
Size : 16 bits  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-4 (000h)</td>
<td>Corresponds to A[31:20] of the CPU to AGP Pre-fetchable Memory Limit Address</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Register Index : 33h-28h  
Register Name : Reserved Registers  
Default Value : 00h  
Attribute : Read Only  

Register Index : 34h  
Register Name : Capability pointer Register  
Default Value : 0E0h  
Attribute : Locked Read/write  
Size : 8 bits  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (0e0h)</td>
<td>Point to the start index of AGP standard register block</td>
</tr>
<tr>
<td></td>
<td>Default is pointer to index 0E0h.</td>
</tr>
<tr>
<td></td>
<td>If M1541 index 90h bit1=1 then this register can be read/written</td>
</tr>
</tbody>
</table>
Register Index: 3Dh
Register Name: Interrupt pin
Default Value: 00h
Attribute: Read only
Size: 8 bits

Register Index: 3Ch
Register Name: Interrupt line
Default Value: 00h
Attribute: Lock Read/Write (control bit M1541 offset 90 bit 7)
Size: 8 bits

Register Index: 3Bh-35h
Register Name: Reserved Registers
Default Value: 00h
Attribute: Read Only

Register Index: 3Fh-3Eh
Register Name: PCI-to-PCI Bridge Control Register
Default Value: 0000h
Attribute: Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-11 (00h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 10 (0)     | Discard Timer Status  
|            | when set to 1, indicates that a delayed transaction has been discarded |
| 9 (0)      | Secondary Discard Timer Enable  
|            | 0: disable  
<p>|            | 1: enable   |
| 8-4 (00h)  | Reserved     |</p>
<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Value 0</th>
<th>Value 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 (0)</td>
<td>VGA Enable</td>
<td>disable</td>
<td>enable</td>
</tr>
<tr>
<td></td>
<td>(Control the routing of CPU-initiated transactions target VGA compatible I/O (3B0h<del>3BBh &amp; 3Coh</del>3DFh) and memory (0A0000h~0BFFFFh) address region to AGP.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 (0)</td>
<td>ISA Enable</td>
<td>disable, forward to AGP if in the range between IOBASE and IOLIMIT</td>
<td>enable, forward the top 768Bytes of each 1KByte block (IOBASE~IOLIMIT) to primary PCI.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>System Error Enable</td>
<td>disable (forwarding of GSERRJ to primary SERRJ is disable)</td>
<td>enable (forward to primary PCI)</td>
</tr>
<tr>
<td>0 (0)</td>
<td>Parity Error Response Enable</td>
<td>disable (ignores address and data parity errors on the AGP)</td>
<td>enable (assert GSERRJ)</td>
</tr>
</tbody>
</table>

Register Index: **83h-40h**
Register Name: **Reserved Registers**
Default Value: **00h**
Attribute: **Read Only**
Register Index: 85h-84h
Register Name: **PCI_66 Programmable Frame Buffer Memory Region**
Default Value: 0000h
Attribute: Read/Write
Size: 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 15-4 (000h) | Starting address of Programmable Frame Buffer  
The 12-bits correspond to A[31:20] of the starting address. The remaining bits A[19:0] is assumed to be zero. These bits combined with bits 3-0 can determine the Frame Buffer starting address and stopping address. When Index-86h bit 0 is set to ‘1’, the M5243 will decode the boundary and enable CPU to PCI write buffer. |
| 3-0 (0h) | Size of Programmable GFrame Buffer  
0000: 1 MBytes.  
0001: 2 MBytes.  
0010: 4 MBytes.  
0011: 8 MBytes.  
0100: 16 MBytes.  
1XXX: all CPU to PCI_66 Memory Write Cycle into buffer  
The GFrame Buffer Region should not overlap with local memory. |

The GFrame Buffer Region should not overlap with local memory.
Register Index: 86h
Register Name: CPU to PCI_66 Write Buffer Option
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00)</td>
<td>Reserved</td>
</tr>
<tr>
<td>5 (0)</td>
<td>GCLKRUNJ/GSERRJ function select</td>
</tr>
<tr>
<td>0 : GSERRJ</td>
<td></td>
</tr>
<tr>
<td>1 : GCLKRUNJ</td>
<td></td>
</tr>
<tr>
<td>This bit decides whether the GCLKRUNJ/GSERRJ will be GCLKRUNJ or GSERRJ.</td>
<td></td>
</tr>
<tr>
<td>4 (0)</td>
<td>GPERRJ on PCI_66 bus forward to PERRJ on PCI_33 bus enable</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>When enable this bit, the PCI_66 bus GPERRJ error will reflect at PCI_33 PERRJ signal.</td>
<td></td>
</tr>
<tr>
<td>3 (0)</td>
<td>LINEAR_WORD-Merge for GFrame Buffer Cycle</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>When this bit is enabled, only the consecutive linear increased addresses can be merged. Otherwise, the second write cycle will write into a new Host to PCI_66 Write Buffer location instead of merging with the previous buffer location posted by the first write cycle.</td>
<td></td>
</tr>
<tr>
<td>2 (0)</td>
<td>Use PCI_66 Write-Burst</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit is used to enable PCI_66 write burst capability. If this bit is enabled, the consecutive PCI_66 write cycles will become a burst cycle on the PCI_66 bus.</td>
<td></td>
</tr>
<tr>
<td>1 (0)</td>
<td>VGA 0A0000-0BFFFF Fixed Frame Buffer</td>
</tr>
<tr>
<td>0 : disable</td>
<td></td>
</tr>
<tr>
<td>1 : enable</td>
<td></td>
</tr>
<tr>
<td>This bit is used to enable 0A0000h-0BFFFFh Frame Buffer and the Host to PCI_66 Write Buffer.</td>
<td></td>
</tr>
</tbody>
</table>
| 0 (0) | Programmable Frame Buffer.
| 0 : disable  
| 1 : enable  
| This bit is used to combine with index 85h-84h to enable the programmable PCI_66 Frame Buffer and the Host to PCI Write Buffer. |
Register Index: **87h**
Register Name: **CPU to PCI_66 Option**
Default Value: **00h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Monochrome Device Adapter Enable</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>If this bit is set to enable and M5243 index 3Eh bit3=1(VGA enable), then the Memory region 087FFFh-0B0000h and IO address 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh will send forward to PCI_33.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Graphic Non_buffer FRAMEJ Request control</td>
</tr>
<tr>
<td></td>
<td>0 : Enable the Graphic Non_buffer FRAMEJ request control</td>
</tr>
<tr>
<td></td>
<td>1 : Disable the Graphic Non_buffer FRAMEJ request control</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the internal Non_buffer FRAMEJ request control</td>
</tr>
<tr>
<td>4-0 (00h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### 4.8.1 PCI_66 to Host Interface Register

Register Index: **88h**
Register Name: **PCI_66 to Main Memory / PCI_66 Arbiter Option**
Default Value: **00h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>PCI_66 master GAT mode</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, if PCI_66 master is retried during a read transaction, the master will be marked as a GAT master. When the same master retries the transaction at a later time, M5243 will flush the designed buffers before granting the bus ownership to it.</td>
</tr>
<tr>
<td>Bit Number</td>
<td>Bit Function</td>
</tr>
<tr>
<td>------------</td>
<td>-------------</td>
</tr>
<tr>
<td>6-4 (000)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Force PCI_66 GAT Mode</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, the M5243 will flush all necessary internal buffers before granting to the PCI_66 master.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Force Host to PCI_66 write request to assert all the time</td>
</tr>
<tr>
<td></td>
<td>0 : disable</td>
</tr>
<tr>
<td></td>
<td>1 : enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, the M5243 will always assert its request for PCI_66 bus ownership.</td>
</tr>
<tr>
<td>1-0 (00)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Register Index : **89h**

Register Name : **PCI\_66 Arbiter Time Slice**

Default Value : **20h**

Attribute : Read/Write

Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (20h)</td>
<td>Number of PCI_66 clocks for PCI_66 bus time slice</td>
</tr>
<tr>
<td></td>
<td>The time-slice will guarantee the minimum clocks that the PCI_66 master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle.</td>
</tr>
<tr>
<td></td>
<td>The bits 1-0 are assumed to be &quot;00&quot; and are ignored.</td>
</tr>
</tbody>
</table>
Register Index : 8Ah
Register Name : CPU Arbiter Time Slice
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (20h)</td>
<td>Number of PCI_66 clocks for CPU Bus time slice. The time-slice will guarantee the minimum clocks that the CPU master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be &quot;00&quot; and are ignored.</td>
</tr>
</tbody>
</table>

Register Index : 8Bh
Register Name : PCI_66 Retry Control for PCI-66 to Host Cycle
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>Reserved</td>
</tr>
<tr>
<td>3-2 (00)</td>
<td>Retry Latency for PCI_66 to PCI_33 Cycle Control</td>
</tr>
<tr>
<td></td>
<td>00 : Retry on first Data phase if wait state &gt; 32 PCI_66 clocks or Retry on Second Data phase if wait state &gt; 8 PCI_66 clocks</td>
</tr>
<tr>
<td></td>
<td>01 : Retry on first Data phase if wait state &gt; 16 PCI_66 clocks or Retry on Second Data phase if wait state &gt; 4 PCI_66 clocks</td>
</tr>
<tr>
<td></td>
<td>The following setting is pseudo delay transaction mode</td>
</tr>
<tr>
<td></td>
<td>10 : Retry on first Data phase if wait state &gt; 2 PCI_66 clocks or Retry on Second Data phase if wait state &gt; 2 PCI_66 clocks</td>
</tr>
<tr>
<td></td>
<td>11 : Never Retry on first Data phase. Never Retry on Second Data phase</td>
</tr>
<tr>
<td>Setting</td>
<td>Retry Latency for PCI_66 to Host Cycle Control</td>
</tr>
<tr>
<td>---------</td>
<td>-----------------------------------------------</td>
</tr>
<tr>
<td>00</td>
<td>Retry on first Data phase if wait state &gt; 32 PCI_66 clocks or Retry on Second Data phase if wait state &gt; 8 PCI_66 clocks</td>
</tr>
<tr>
<td>01</td>
<td>Retry on first Data phase if wait state &gt; 16 PCI_66 clocks or Retry on Second Data phase if wait state &gt; 4 PCI_66 clocks</td>
</tr>
<tr>
<td></td>
<td>The following setting is pseudo delay transaction mode</td>
</tr>
<tr>
<td>10</td>
<td>Retry on first Data phase if wait state &gt; 2 PCI_66 clocks or Retry on Second Data phase if wait state &gt; 2 PCI_66 clocks</td>
</tr>
<tr>
<td>11</td>
<td>Never Retry on first Data phase Never Retry on Second Data phase</td>
</tr>
</tbody>
</table>
Register Index :  8Ch
Register Name :  PCI_66 to Main Memory Option
Default Value :  00h
Attribute :  Read/Write
Size :  8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Check PCI_66 master memory read multiple command</td>
</tr>
<tr>
<td></td>
<td>0 : enable</td>
</tr>
<tr>
<td></td>
<td>1 : disable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enable, the M5243 will recognize memory read multiple PCI_66 command.</td>
</tr>
<tr>
<td>6-2 (00)</td>
<td>Reserved</td>
</tr>
<tr>
<td>1-0 (00)</td>
<td>PCI_66 to Host Read Buffer Pre-fetch Threshold</td>
</tr>
<tr>
<td></td>
<td>00 : Reserved</td>
</tr>
<tr>
<td></td>
<td>01 : Pre-fetch two lines at most</td>
</tr>
<tr>
<td></td>
<td>10 : Pre-fetch three lines at most</td>
</tr>
<tr>
<td></td>
<td>11 : Reserved</td>
</tr>
</tbody>
</table>

Register Index :  8Dh
Register Name :  Reserved Registers
Default Value :  00h
Attribute :  Read Only

Register Index :  8Eh
Register Name :  AGP Write/AGP Read Arbiter Time Slice
Default Value :  020h
Attribute :  Read/Write
Size :  8 bits
### Number of PCI_66 clocks for AGP write/AGP read master bus time slice

The Time-Slice will guarantee the minimum clocks that the AGP write/AGP read master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored.

<table>
<thead>
<tr>
<th>Register Index</th>
<th>Register Name</th>
<th>Default Value</th>
<th>Attribute</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>8Fh</td>
<td>PCI_33 to PCI_66 Write Arbiter Time Slice</td>
<td>20h</td>
<td>Read/Write</td>
<td>8 bits</td>
</tr>
</tbody>
</table>

### Number of PCI_66 clocks for PCI_33 to PCI_66 write bus time slice

The Time-Slice will guarantee the minimum clocks that the PCI_66 master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored.

<table>
<thead>
<tr>
<th>Register Index</th>
<th>Register Name</th>
<th>Default Value</th>
<th>Attribute</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>0DFh-90h</td>
<td>Reserved Registers</td>
<td>00h</td>
<td>Read Only</td>
<td></td>
</tr>
</tbody>
</table>

Register Name: **PCI_33 to PCI_66 Write Arbiter Time Slice**

Register Index: **8Fh**

Register Name: **Reserved Registers**

Default Value: **20h**

Attribute: **Read/Write**

Size: **8 bits**

Register Index: **0DFh-90h**

Register Name: **Reserved Registers**

Default Value: **00h**

Attribute: **Read Only**
4.8.2 PCI_66 Green Function Support

Register Index: 0E0h
Register Name: PCI_66 Power Management Capability Identifier Register
Default Value: 01h
Attribute: Locked Read/Write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (01h)</td>
<td>PCI_66 Capability Identifier</td>
</tr>
<tr>
<td></td>
<td>The capability identifier, when read by system software as 01h indicates that the data structure currently being pointed to is the PCI Power management data structure.</td>
</tr>
<tr>
<td></td>
<td>The register default is read only, when M1541 index 90h bit 5 = 1, this register can be read/write.</td>
</tr>
</tbody>
</table>

Register Index: 0E1h
Register Name: PCI_66 Power Management Next Item Pointer Register
Default Value: 00h
Attribute: Locked Read/write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>PCI_66 Next Item Pointer</td>
</tr>
<tr>
<td></td>
<td>This field provides an offset into the function's PCI configuration space pointing to the location of next item in the function’s capability list. If there are no additional items in the capabilities list, this register is set to 00h.</td>
</tr>
<tr>
<td></td>
<td>The register default is read only, when M1541 index 90h bit 5 = 1, this register can read/write.</td>
</tr>
</tbody>
</table>
Register Index: 0E3h-0E2h  
Register Name: **PCI_66 Power Management Capabilities Register**  
Default Value: 0000h  
Attribute: Locked Read/write. The register default is read only, when M1541 index 90h bit 5 = 1, this register can read/write.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 15-11 (00000) | PCI_66 PME_Support  
XXXX1: PMEJ can be asserted from D0  
XXX1X: PMEJ can be asserted from D1  
XX1XX: PMEJ can be asserted from D2  
X1XXX: PMEJ can be asserted from D3 hot  
1XXXX: PMEJ can be asserted from D3 cold  
These five bits field indicate the power states in which function may assert PMEJ. A value of ‘0’ for any bit indicates that the function is not capable of asserting the PMEJ signal while in that power state. |
| 10 (0) | PCI_66 D2_Support  
0: Do not support D2  
1: Support D2  
If this bit is a ‘1’, M5243 supports the D2 power management state. |
| 9 (0) | PCI_66 D1_Support  
0: Do not support D1  
1: Support D1  
If this bit is a ‘1’, M5243 supports the D2 power management state. |
| 8-6 (000) | Reserved |
| 5 (0) | PCI_66 Device Specific Initialization (DSI)  
0: Not required  
1: Required  
If this bit is ‘1’, it indicates that the function requires a device specific initialization sequence following transition to the D0 un-initialized state. |
| 4 (0) | PCI_66 Auxiliary Power Source  
This bit is only meaningful if the bit 15 (PMEJ can be asserted from D3 cold) = 1  
0: Supply own auxiliary power source  
1: Support for PMEJ in D3 cold requires auxiliary power supplied by the system by way of proprietary delivery vehicle. |
<table>
<thead>
<tr>
<th>3 (0)</th>
<th>PCI_66 PME clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 :</td>
<td>It indicates that M5243 relies on the presence of the PCI_66 clock for PMEJ operation.</td>
</tr>
<tr>
<td>1 :</td>
<td>It indicates that no PCI clock is required for M5243 to generate PMEJ.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2-0 (001)</th>
<th>Version of PCI_66 power management interface specification</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>The version support is V1.0 now.</td>
</tr>
</tbody>
</table>
Register Index: 0E5h-0E4h
Register Name: PCI_66 Power Management Control and Status Register
Default Value: 0000h
Attribute: Some bits can read/write, some bits are Locked read/write. These bits marked with Locked read/write default is read only, when index 90h bit 5 = 1, these bits can read/write.

<table>
<thead>
<tr>
<th>Bit Function</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15 (0)                              | **PCI_66 PME_Status (Read/Write_clear)**  
This bit is set when the function would normally assert the PMEJ signal independent of the state of the PME_EN (index 0E4h bit 8)  
Write “1” to this bit will clear this bit to “0” and cause the M5243 to stop asserting a PMEJ (if enable). Writing a “0” has no effect.  
This bit defaults to “0” if the M5243 does not support PMEJ generation from D3 cold. |
| 14-13 (00)                          | **PCI_66 Data_scale (Locked read/write)**  
These two bits field indicate the scaling factor to be used when interpreting the value of the DATA register (index 0e7h). The value & meaning of this field varies depending on which data value has been selected bit[12-9] (DATA_select) field. |
| 12-9 (0h)                           | **PCI_66 Data_Select (read/write)**  
These four bits are used to select which data is to be reported through DATA register (index 0E7h) and data scale (bit[14-13]) field. |
| 8 (0)                               | **PCI_66 PME_EN (read/write)**  
0 : PMEJ assertion is disable  
1 : Enable the function to assert PMEJ |
| 7-2 (00h)                           | **Reserved (Locked read/write)** |
| 1-0 (00)                            | **PCI_66 Power State (read/write)**  
00 : D0  
01 : D1  
10 : D2  
11 : D3 hot  
These two bits are used to determine the current power state of a function and set the function into a new power state. If software attempts to write an unsupported, optional state to this field. The write operation must complete normal on the bus, however the data is discarded and no state change occurs. |
Register Index : 0E6h
Register Name : PCI_66 PMCSR PCI to PCI Bridge Support Extensions
Default Value : 00h
Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>PCI_66 Bus Power/Clock Control Enable</td>
</tr>
<tr>
<td>0 : PCI_66 Bus power/clock control mechanism has been disabled</td>
<td></td>
</tr>
<tr>
<td>1 : PCI_66 Bus power/clock control mechanism has been enabled</td>
<td></td>
</tr>
<tr>
<td>When the Bus Power/Clock control mechanism is disabled, the bridge’s PMCSR Power State field cannot be used by the system software to control the power or clock of the bridge’s secondary bus.</td>
<td></td>
</tr>
<tr>
<td>6 (0)</td>
<td>B2/B3 support for D3 hot</td>
</tr>
<tr>
<td>0 : The bridge function is programmed to D3 hot, its secondary bus will have its power removed (B3)</td>
<td></td>
</tr>
<tr>
<td>1 : The bridge function is programmed to D3 hot, its secondary bus PCI_66 clock will be stopped (B2)</td>
<td></td>
</tr>
<tr>
<td>The state of this bit determines the action that is to occur as a direct result of programming the function to D3 hot. This bit is only meaningful if bit 7=1 (PCI_66 Bus Power/Clock control enable)</td>
<td></td>
</tr>
<tr>
<td>5-0 (00h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Register Index : 0E7h
Register Name : Data Register
Default Value : 00h
Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>PCI_66 Data[7-0]</td>
</tr>
<tr>
<td>This register is used to report the state dependent data requested by the Data_Select (index 0E4h bit[12-9] ) field. The value of this register is scaled by the value reported by the Data_Scale (Index 0E4h bit[12-9] ) field.</td>
<td></td>
</tr>
</tbody>
</table>

Register Index : 0FFh-E8h
Register Name : Reserved Registers
Default Value : 00h
Attribute : Read Only
Section 5: Hardware Setup Guide

The M1541 will strobe the hardware setting value in the respective registers when the RSTJ goes inactive. BIOS can utilize the register value to save the software programming time to detect L2 type, size, PLL enable/disable and setting the bus frequency. For notebook applications, it is recommended to use software programming to reduce power consumption since the pull-up and pull-down resistors will continuously consume system power. If the BIOS wants to utilize the hardware setting value, the system board designer must make sure the strobe value is identical to their definition. Otherwise, the software programming must be used to detect the hardware configuration. The HA[31:19] default is pull low by M1541. The pull low resistor range is from 60K Ohm to 20K Ohm and the typical value is 40K Ohm. If circuit needs to pull high, a below or equal to 10K pull high resistor is required.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Description</th>
<th>Pull-up</th>
<th>Pull-down</th>
<th>Register Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>HA[31..29]</td>
<td>Indicate Host frequency</td>
<td>-</td>
<td>-</td>
<td>Index-0EDh bits[7:5] (1)</td>
</tr>
<tr>
<td>HA[28]</td>
<td>CPU interface PLL support</td>
<td>Enable</td>
<td>Disable</td>
<td>Index-0EDh bit[4]</td>
</tr>
<tr>
<td>HA[27-25]</td>
<td>CPUCLK compensate select</td>
<td>-</td>
<td>-</td>
<td>Index-0EDh bits[3-1] (4)</td>
</tr>
<tr>
<td>HA[24]</td>
<td>CPUCLK PLL internal test select</td>
<td>Test mode</td>
<td>Normal mode</td>
<td>Index-0EDh bit[0]</td>
</tr>
<tr>
<td>HA[27-26]</td>
<td>CPUCLK compensate select</td>
<td>-</td>
<td>-</td>
<td>Index-0EDh bits[3-2] (5)</td>
</tr>
<tr>
<td>HA[25-24]</td>
<td>HD output clock select</td>
<td>-</td>
<td>-</td>
<td>Index-0EDh bit[1-0] (6)</td>
</tr>
<tr>
<td>HA[23]</td>
<td>Internal TAG support</td>
<td>Enable</td>
<td>Disable</td>
<td>Index-040h bit[6]</td>
</tr>
<tr>
<td>HA[22]</td>
<td>L2 cache type select</td>
<td>MOSYS cache</td>
<td>PB_SRAM</td>
<td>Index-41h bit[4]</td>
</tr>
<tr>
<td>HA[21..20]</td>
<td>Cache size detect</td>
<td>-</td>
<td>-</td>
<td>Index-41h bits[3-2] (3)</td>
</tr>
<tr>
<td>HA[19]</td>
<td>L2 bank select</td>
<td>2-bank</td>
<td>1-bank</td>
<td>Index-41h bit[5]</td>
</tr>
</tbody>
</table>

Note: (1) HA31 HA30 HA29 Host frequency

<table>
<thead>
<tr>
<th>HA21</th>
<th>HA20</th>
<th>Cache size</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>256KB</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>512KB</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1MB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>None</td>
</tr>
</tbody>
</table>

Note (3) For M1541 A1 C and earlier version

<table>
<thead>
<tr>
<th>HA27</th>
<th>HA25</th>
<th>HA24</th>
<th>CPU CLK compensate select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No compensate</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1 buffer</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2 buffers</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3 buffers</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4 buffers</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5 buffers</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6 buffers</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7 buffers</td>
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</tbody>
</table>

For M1541 A1 D and later version

<table>
<thead>
<tr>
<th>HA27</th>
<th>HA26</th>
<th>CPU CLK compensate select</th>
<th>HA25</th>
<th>HA24</th>
<th>HD output clock select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>No compensate</td>
<td>0</td>
<td>0</td>
<td>default</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>2 buffers</td>
<td>1</td>
<td>0</td>
<td>ahead 1 ns</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>4 buffers</td>
<td>1</td>
<td>1</td>
<td>ahead 2 ns</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>6 buffers</td>
<td>1</td>
<td>1</td>
<td>ahead 3 ns</td>
</tr>
</tbody>
</table>
Section 6: Packaging Information
456L BGA Dimension Spec (35 x 35 mm)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>0.50</td>
<td>0.60</td>
<td>0.70</td>
</tr>
<tr>
<td>A2</td>
<td>1.12</td>
<td>1.17</td>
<td>1.22</td>
</tr>
<tr>
<td>b</td>
<td>0.60</td>
<td>0.75</td>
<td>0.90</td>
</tr>
<tr>
<td>c</td>
<td>0.51</td>
<td>0.56</td>
<td>0.61</td>
</tr>
<tr>
<td>D</td>
<td>29.80</td>
<td>30.00</td>
<td>30.20</td>
</tr>
<tr>
<td>D1</td>
<td>31.55</td>
<td>31.75</td>
<td>31.95</td>
</tr>
<tr>
<td>E</td>
<td>29.80</td>
<td>30.00</td>
<td>30.20</td>
</tr>
<tr>
<td>E1</td>
<td>31.55</td>
<td>31.75</td>
<td>31.95</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>1.27</td>
<td></td>
</tr>
<tr>
<td>Hd</td>
<td>34.80</td>
<td>35.00</td>
<td>35.20</td>
</tr>
<tr>
<td>He</td>
<td>34.80</td>
<td>35.00</td>
<td>35.20</td>
</tr>
<tr>
<td>o</td>
<td>23°</td>
<td>30°</td>
<td>37°</td>
</tr>
</tbody>
</table>
Section 7 : Revision History

Initial version 10/15/97
p.6-9,11-13,18,20,25,28-30,36-38,40,59,65,81,82,95,97,108,109 10/20/97
p.2,6-9,16-22,28 10/23/97
p.45,104,118-121,123,125,126,128,130,133,134 11/20/97
p.32 12/19/97
Appendix A 02/16/98
p.45,63-65,72,81,96-99,101-103,105-107,113,115-117,128,130,136 03/12/98
p.117,118 04/08/98
p.96,114 04/15/98
p.57,101 06/02/98
p.128 06/03/98
p.1 06/12/98
p.27,28,31,56,64,72,96-98,103,105,115-117 06/19/98
p.52,57,65,81,96,97 07/16/98 HHC
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