M1531B : CPU-to-PCI bridge, Memory, Cache and Buffer Controller

1.1 Features

- Supports all Intel/Cyrix/AMD/TI/IBM 586 socket processors. Host bus at 83.3MHz, 75MHz, 66 MHz, 60 MHz and 50MHz at 3.3V/2.5V.
  - Supports linear wrap mode for Cyrix M1 & M2
  - Supports Write Allocation feature for K6
  - Supports Pseudo Synchronous PCI bus access (CPU bus 75MHz - PCI bus 30MHz, CPU bus 83.3MHz - PCI bus 33MHz)

- Supports Pipelined-Burst SRAM
  - Direct mapped, 256KB/512KB/1MB
  - Write-Back/Dynamic-Write-Back cache policy
  - Built-in 8K*2 bit SRAM for MESI protocol to reduce cost and enhance performance
  - Cacheable memory up to 64MB with 8-bit Tag SRAM
  - Cacheable memory up to 512MB with 11-bit Tag SRAM
  - 3-1-1-1-1-1-1 for Pipelined Burst SRAM at back-to-back burst read and write cycles.
  - Supports 3.3V/5V SRAMs for Tag Address.
  - Supports CPU Single Read Cycle L2 Allocation.

- Supports FPM/EDO/SDRAM DRAMs
  - 8 RAS Lines up to 1GByte support
  - 64-bit data path to Memory
  - Symmetrical/Asymmetrical DRAMs
  - 3.3V or 5V DRAMs
  - Duplicated MA[1:0] driving pins for burst access
  - No buffer needed for RASJ and CASJ and MA[1:0]
  - CBR and RAS-only refresh for FPM
  - CBR- and RAS-only refresh and Extended refresh and self refresh for EDO
  - CBR- and Self refresh for SDRAM
  - 16 QWORD deep merging buffer for 3-1-1-1-1-1-1-1 posted write cycle to enhance high speed CPU burst access
  - 6-3-3-3-3 for back-to-back FPM read page hit
  - 5-2-2-2-2-2 for back-to-back EDO read page hit
  - 6-1-1-1-1-1 for back-to-back SDRAM read page hit
  - 2-2-2-2 for retired data for posted write on FPM and EDO page-hit
  - x-1-1-1 for retired data for posted write SDRAM page-hit
  - Enhanced DRAM page miss performance
  - Supports 64M-bit (16M*4, 8M*8, 4M*16) technology of DRAMs
  - Supports Programmable-strength RAS/CAS/MWEJ/MA buffers.
  - Supports Error Checking & Correction (ECC) and Parity for DRAM
  - Supports the most flexible six 32-bit populated banks of DRAM to support the most friendly DRAM upgrade ability
  - Supports SIMM and DIMM

- Synchronous/Pseudo Synchronous 25/30/33MHz 3.3V/5V tolerance PCI interface
  - Concurrent PCI architecture
    - PCI bus arbiter: five PCI masters and M1533/M1543 (ISA Bridge) supported
    - 6 DWORDs for CPU-to-PCI Memory write posted buffers
    - Converts back-to-back CPU to PCI memory write to PCI burst cycle
    - 38/22 DWORDs for PCI-to-DRAM Write-posted/Read-prefetching buffers
    - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 writeback)
    - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
    - Supports PCI mechanism #1 only
    - PCI spec. 2.1 support. (N(32/16/8)+8 rule, passive release, fair arbitration)
    - Enhanced performance for Memory-Read-Line and Memory-Read-Multiple and Memory-write-Invalidate PCI commands.

- Enhanced Power Management
  - ACPI support
  - Supports PCI bus CLKRUN function
  - Supports Dynamic Clock Stop
  - Supports Power On Suspend
  - Supports Suspend to Disk
  - Supports Suspend to DRAM
  - Self Refresh during Suspend

- 328-pin (27mmx27mm) BGA package
Table of Contents :

Section 1 : Introduction .............................................................. 1
  1.1 Features ............................................................................. 1
  1.2 Introduction ..................................................................... 3

Section 2 : Pin Description .......................................................... 5
  2.1 Pin Diagram ..................................................................... 5
  2.2 Pin Description Table ........................................................ 7
  2.3 Numerical Pin List ......................................................... 11
  2.4 Alphabetical Pin List ....................................................... 15

Section 3 : Function Description .................................................. 19
  3.1 System Architecture ....................................................... 19
  3.2 CPU Interface ................................................................. 21
  3.3 Clock Design Philosophy .................................................. 21
  3.4 Cache Memory Timing/Configuration ......................... 22
  3.5 System Memory Timing/Configuration ....................... 24
  3.6 CPU-to-PCI Posted Write Buffer .................................... 33
  3.7 PCI Master Latency and Throughput Analysis ............... 33
  3.8 Low Power Features ......................................................... 34
  3.9 DRAM Refresh ................................................................. 35
  3.10 ECC/Parity Algorithm ..................................................... 35

Section 4 : Configuration Registers .............................................. 36

Section 5 : Hardware and Software Programming Guide .................. 86
  5.1 Hardware Setup Table ..................................................... 86
  5.2 DRAM Detection Flow ..................................................... 87
  5.3 L2 Cache Autosizing Flowchart .................................... 98
  5.4 Enable Shadow Region ................................................... 100
  5.5 Software MESI Test ........................................................ 101

Section 6 : Packaging Information ............................................... 102

Section 7 : Revision History ........................................................ 103

Appendix A : M1531B Application Notes ..................................... 104
1.2 Introduction

Aladdin-IV is the succeeding generation chipset of Aladdin-III from Acer Labs. It maintains the best system architecture (2-chip solution) to achieve the best system performance with the lowest system cost (TTL-free). Aladdin-IV consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for the most engaging multimedia/multithreading OS and software applications. It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and makes the system manufacturing easier.

M1531B is the successor of M1531. The major differences are the 64-Mbit SDRAM support and more cacheable region support in SDRAM configuration. Please refer to the application note in Appendix A.

M1531B includes the higher CPU bus frequency (up to 83.3MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and L2 controller, internal MESI tag bits (8K*2) to reduce cost and enhance performance, high performance FPM/EDO/SDRAM DRAM controller, PCI 2.1 compliant bus interface, smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance, and also the highly efficient PCI fair arbiter. M1531B also provides the most flexible 32/64-bit memory bus interface for the best DRAM upgrade ability and ECC/Parity design to enhance the system reliability.

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, PCI-to-DRAM access can run concurrently with CPU-to-L2 access. M1531B also supports the snoop ahead feature to achieve the PCI master full bandwidth access (133Mbytes). M1531B also provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support the Microsoft’s On Now technology OS.

M1533 provides the best power management system solution. M1533 integrates ACPI support, deep green function, 2-channel dedicated Ultra-33 IDE master controller, 2-port USB controller, SMBus controller, and PS2 Keyboard/Mouse controller.

M1543 provides the best desktop system solution. M1543 integrates ACPI support, green function, 2-channel dedicated Ultra-33 IDE Master controller, 2-port USB controller, SMBus controller, PS/2 Keyboard/Mouse controller and the Super I/O (Floppy Disk Controller, 2 serial port/1 parallel port) support.

In the following diagram, ALADDIN-IV gives a highly integrated system solution and a most up-to-date architecture, which provides the best cost/performance system solution for Desktop and also for Notebook vendors.
Figure 2-1. M1531B Pin Diagram
Figure 2-2. M1531B Pin Diagram (bottom view)
## 2.2 Pin Description Table:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Host Interface:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A[31:3]</td>
<td>I/O</td>
<td>Group A Host Address Bus Lines. A[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1531B drives them during inquiry cycles on behalf of PCI masters.</td>
</tr>
<tr>
<td>BEJ[7:0]</td>
<td>I</td>
<td>Group A Byte Enables. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1531B.</td>
</tr>
<tr>
<td>ADSJ</td>
<td>I</td>
<td>Group A Address Strobe. The CPU will start a new cycle by asserting ADSJ first. The M1531B will not precede to execute a cycle until it detects ADSJ active.</td>
</tr>
<tr>
<td>BRDYJ</td>
<td>O</td>
<td>Group A Burst Ready. The assertion of BRDYJ means the current transaction is complete. The CPU will terminate the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.</td>
</tr>
<tr>
<td>NAJ</td>
<td>O</td>
<td>Group A Next Address. It is asserted by the M1531B to inform the CPU that pipelined cycles are ready for execution.</td>
</tr>
<tr>
<td>AHOLD</td>
<td>O</td>
<td>Group A CPU AHold Request Output. It connects to the input of CPU's AHOLD pin and is actively driven for inquiry cycles.</td>
</tr>
<tr>
<td>EADSJ</td>
<td>O</td>
<td>Group A External Address Strobe. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1531B will assert this signal to proceed snooping.</td>
</tr>
<tr>
<td>BOFFJ</td>
<td>O</td>
<td>Group A CPU Back-Off. If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1531B will assert this signal to request CPU floating all its output buses.</td>
</tr>
<tr>
<td>HITMJ</td>
<td>I</td>
<td>Group A Primary Cache Hit and Modified. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.</td>
</tr>
<tr>
<td>MIOJ</td>
<td>I</td>
<td>Group A Host Memory or I/O. This bus definition pin indicates the current bus cycle is either memory or input/output.</td>
</tr>
<tr>
<td>DCJ</td>
<td>I</td>
<td>Group A Host Data or Code. This bus definition pin is used to distinguish data access cycles from code access cycles.</td>
</tr>
<tr>
<td>WRJ</td>
<td>I</td>
<td>Group A Host Write or Read. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.</td>
</tr>
<tr>
<td>HLOCKJ</td>
<td>I</td>
<td>Group A Host Lock. When HLOCKJ is asserted by the CPU, the M1531B will recognize the CPU is locking the current cycles.</td>
</tr>
<tr>
<td>CACHEJ</td>
<td>I</td>
<td>Group A Host Cacheable. This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.</td>
</tr>
<tr>
<td>KENJ/INV</td>
<td>O</td>
<td>Group A Cache Enable Output. This signal is connected to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cachable. INV is used during L1 snoop cycles. The M1531B drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.</td>
</tr>
<tr>
<td>SMIACTJ</td>
<td>I</td>
<td>Group A SMM Interrupt Active. This signal is asserted by the CPU to inform the M1531B that SMM mode is being entered.</td>
</tr>
<tr>
<td>HD[63:0]</td>
<td>I/O</td>
<td>Group A Host Data Bus Lines. These signals are connected to the CPU's data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.</td>
</tr>
<tr>
<td>MPD[7:0]</td>
<td>I/O</td>
<td>Group C DRAM Parity/ECC check bits. These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit.</td>
</tr>
<tr>
<td>RASJ[7] / SRASJ[0]</td>
<td>O</td>
<td>Group C Row Address Strobe 7. (FPM/EDO) of DRAM row 7. SDRAM Row Address Strobe (SDRAM) copy 0. It connects to SDRAM RASJ. This is a multifunction pin and determined by Index-5Ch bit0.</td>
</tr>
</tbody>
</table>
## Pin Description Table (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DRAM Interface</strong> 3.3V/5V Tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RASJ[6]/ SCASJ[0]</td>
<td>O Group C</td>
<td>Row Address Strobe 6, (FPM/EDO) of DRAM row 6. SDRAM Column address strobe (SDRAM) copy 0. It connects to SDRAM CASJ. This is a multifunction pin and determined by Index-5Ch bit0.</td>
</tr>
<tr>
<td>RASJ5/TIO[9]</td>
<td>I/O Group C</td>
<td>Row Address Strobe 5, (FPM/EDO) of DRAM row 5. In SDRAM, they are used to drive the corresponding SDRAM CSJs. SRAM Tag[9]. It connects to SRAM tag address bit 9. This is a multifunction pin and determined by index-4Ch bits [7:6].</td>
</tr>
<tr>
<td>RASJ4/TIO[10]</td>
<td>I/O Group C</td>
<td>Row Address Strobe 4, (FPM/EDO) of DRAM row 4. In SDRAM, they are used to drive the corresponding SDRAM CSJs. SRAM Tag[10]. It connects to SRAM tag address bit 10. This is a multifunction pin and determined by index-4Ch bits [7:6].</td>
</tr>
<tr>
<td>RASJ[3:0]</td>
<td>O Group C</td>
<td>Row Address Strobes. These signals are used to drive the corresponding RASJs of FPM/EDO DRAMs. In SDRAM, they are used to drive the corresponding SDRAM CSJs.</td>
</tr>
<tr>
<td>CASJ[7:0] / DQM[7:0]</td>
<td>O Group C</td>
<td>Column Address Strobes or Synchronous DRAM Input/Output Data Mask. These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].</td>
</tr>
<tr>
<td>MA[11:2]</td>
<td>O Group C</td>
<td>DRAM Address Lines. These signals are the address lines[11:2] of all DRAMs. The M1531B supports DRAM types ranging from 256K to 64Mbits.</td>
</tr>
<tr>
<td>MAA[1:0]</td>
<td>O Group C</td>
<td>Memory Address copy A for [1:0]. These signals are the address lines[1:0] copy 0 of all DRAMs.</td>
</tr>
<tr>
<td>MAB[1:0] / MA[13:12]</td>
<td>O Group C</td>
<td>Memory Address copy B for [1:0]/SDRAM Memory Address lines[13:12]. These signals are the address lines[1:0] copy 1 of FPM/EDO DRAMs. In SDRAM, M1531B automatically changes these pins' function as MA[13:12] to support 64Mbits SDRAM. Please refer to application note in Appendix A.</td>
</tr>
<tr>
<td>MWEJ[0]</td>
<td>O Group C</td>
<td>DRAM Write Enable. This is the DRAM write enable pin and behaves according to the early-write mechanism, i.e., it activates before the CASJs do. For refresh cycles, it will remain deasserted.</td>
</tr>
<tr>
<td>MD[63:0]</td>
<td>I/O Group C</td>
<td>Memory Data. These pins are connected to DRAM’s data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.</td>
</tr>
<tr>
<td>CLKEN[0]/ REQJ[4]</td>
<td>I/O Group C</td>
<td>SDRAM Clock Enable Copy 0 or PCI Master Request. This signal is used as SDRAM clock enable copy 0 to do self refresh during suspend. This pin can also be used as bus request signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.</td>
</tr>
<tr>
<td>CLKEN[1]/ GNTJ[4]</td>
<td>O Group C</td>
<td>SDRAM Clock Enable Copy 1 or PCI Master Grant. This signal is used as SDRAM clock enable copy 1 to do self refresh during suspend. This pin can also be used as grant signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.</td>
</tr>
</tbody>
</table>

## Secondary Cache Interface 3.3V/2.5V

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CADVJ</td>
<td>O Group A</td>
<td>Synchronous SRAM Advance. This signal will make PBSRAM internal burst address counter advance.</td>
</tr>
<tr>
<td>CADSJ</td>
<td>O Group A</td>
<td>Synchronous SRAM Address Strobe. This signal connects to PBSRAM ADSCJ.</td>
</tr>
<tr>
<td>CCSJ</td>
<td>O Group A</td>
<td>Synchronous SRAM Chip Select. This signal connects to PBSRAM CE1J to mask ADSPJ and enable ADSCJ sampling.</td>
</tr>
<tr>
<td>GWEJ</td>
<td>O Group A</td>
<td>Synchronous SRAM Global Write Enable. This signal will write all the byte lanes data into PBSRAM.</td>
</tr>
<tr>
<td>Signal</td>
<td>Group</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>COEJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Output Enable.</strong> This signal will enable the data output driving of PBSRAM.</td>
</tr>
<tr>
<td>BWEJ</td>
<td>O</td>
<td><strong>Synchronous SRAM Byte-Write Enable.</strong> This signal connects to byte write enable of PBSRAM.</td>
</tr>
</tbody>
</table>
### Pin Description Table (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Secondary Cache Interface 3.3V/5V Tolerance</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MWEJ[1]</td>
<td>I/O</td>
<td>Group C Another copy of MWEJ. This pin is used for multifunction in M1531. In M1531B, this pin is always as another copy of MWEJ. BIOS should fix the programming index-41h bit 6, bit 3 and bit 0 as ‘110’.</td>
</tr>
<tr>
<td>SRASJ[1]</td>
<td>I/O</td>
<td>Group C Synchronous DRAM (SDRAM) RAS copy 1. This pin is used for multifunction in M1531. In M1531B, this pin is always as synchronous DRAM (SDRAM) RAS copy 1. BIOS should fix the programming index-41h bit 3 and bit 0 as ‘10’.</td>
</tr>
<tr>
<td>SCASJ[1]</td>
<td>I/O</td>
<td>Group C Synchronous DRAM (SDRAM) CAS copy 1. This pin is used for multifunction in M1531. In M1531B, this pin is always as synchronous DRAM CAS copy 1. BIOS should fix the programming index-41h bit 3 and bit 0 as ‘10’.</td>
</tr>
<tr>
<td>TIO[8:0]</td>
<td>I/O</td>
<td>Group B SRAM Tag[8:0]. This pin contains the L2 tag address for 256 KB L2 caches. TIO[6:0] contain the L2 tag address and TIO7 contains the L2 cache valid bit for 512 KB caches. TIO[5:0] contain L2 tag address, TIO7 contains L2 cache valid bit and TIO6 contains the L2 cache dirty bit for 1MB cache. TIO[8] is the tag address bit 8 and supports cacheable region up to 128MB.</td>
</tr>
<tr>
<td>TAGWEJ</td>
<td>O</td>
<td>Group B Tag Write Enable. This signal, when asserted, will write into the external tag new state and tag addresses.</td>
</tr>
<tr>
<td><strong>PCI Interface 3.3V/5V Tolerance</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD[31:0]</td>
<td>I/O</td>
<td>Group B PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.</td>
</tr>
<tr>
<td>CBEJ[3:0]</td>
<td>I/O</td>
<td>Group B PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.</td>
</tr>
<tr>
<td>FRAMEJ</td>
<td>I/O</td>
<td>Group B Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1531B on behalf of CPU, or as an input during PCI master access.</td>
</tr>
<tr>
<td>DEVSELJ</td>
<td>I/O</td>
<td>Group B Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.</td>
</tr>
<tr>
<td>IRDYJ</td>
<td>I/O</td>
<td>Group B Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.</td>
</tr>
<tr>
<td>TRDYJ</td>
<td>I/O</td>
<td>Group B Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.</td>
</tr>
<tr>
<td>STOPJ</td>
<td>I/O</td>
<td>Group B Stop. This signal indicates the target is requesting the master to stop the current transaction.</td>
</tr>
<tr>
<td>LOCKJ</td>
<td>I/O</td>
<td>Group B Lock Resource Signal. This pin indicates the PCI master or the bridge intends to do exclusive transfers.</td>
</tr>
<tr>
<td>REQJ[3:0]</td>
<td>I</td>
<td>Group B Bus Request signals of PCI Masters. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.</td>
</tr>
<tr>
<td>GNTJ[3:0]</td>
<td>O</td>
<td>Group B Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.</td>
</tr>
<tr>
<td>PHLDJ</td>
<td>I</td>
<td>Group B PCI bus Hold Request. This active low signal is a request from M1533/M1543 for the PCI bus.</td>
</tr>
<tr>
<td>PHLDAJ</td>
<td>O</td>
<td>Group B PCI bus Hold Acknowledge. This active low signal grants PCI bus to M1533/M1543.</td>
</tr>
<tr>
<td>PAR</td>
<td>I/O</td>
<td>Group B Parity bit of PCI bus. It is the even parity bit across PAD[31:0] and CBEJ[3:0].</td>
</tr>
<tr>
<td>SERRJ/</td>
<td>I/O</td>
<td>Group B System Error or PCI Clock RUN. If the M1531B detects parity errors in DRAMs, it will assert SERRJ to notify the system. As CLKRUNJ, this signal will connect to M1533 CLKRUNJ to start, or maintain the PCI CLOCK. It is a multifunction pin and determined by Index-77h bit0.</td>
</tr>
<tr>
<td>CLKRUNJ</td>
<td></td>
<td>Group B</td>
</tr>
</tbody>
</table>
### Pin Description Table (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock, Reset, and Suspend</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HCLKIN</td>
<td>I Group A</td>
<td><strong>CPU bus Clock Input.</strong> This signal is used by all of the M1531B logic that is in the Host clock domain.</td>
</tr>
<tr>
<td>RSTJ</td>
<td>I Group B</td>
<td><strong>System Reset.</strong> This pin, when asserted, resets the M1531B state machine, and sets the register bits to their default values.</td>
</tr>
<tr>
<td>PCICLK</td>
<td>I Group B</td>
<td><strong>PCI bus Clock Input.</strong> This signal is used by all of the M1531B logic that is in the PCI clock domain.</td>
</tr>
<tr>
<td>PCIMRQJ</td>
<td>O Group B</td>
<td><strong>Total PCI Request.</strong> This signal is used to notify M1533/M1543 there is PCI master requesting PCI bus.</td>
</tr>
<tr>
<td>SUSPENDJ</td>
<td>I Group C</td>
<td><strong>Suspend.</strong> When actively sampled, the M1531B will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.</td>
</tr>
<tr>
<td>OSC32KO</td>
<td>I Group C</td>
<td>The refresh reference clock of frequency 32KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.</td>
</tr>
<tr>
<td><strong>Power Pins</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC_A</td>
<td>P</td>
<td><strong>Vcc 3.3V or 2.5V Power for Group A.</strong> This power is used for CPU interface and L2 control signals. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.</td>
</tr>
<tr>
<td>VCC_B</td>
<td>P</td>
<td><strong>Vcc 3.3V Power for Group B.</strong> This power is used for PCI interface and Tag signals. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.</td>
</tr>
<tr>
<td>VCC_C</td>
<td>P</td>
<td><strong>Vcc 3.3V Power for Group C.</strong> This power is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.</td>
</tr>
<tr>
<td>VDD_5</td>
<td>P</td>
<td><strong>Vcc 5.0V Power for Group A and Group B.</strong> This pin supplies the 5V input tolerance circuit and the core power for the internal circuit except the suspend circuit.</td>
</tr>
<tr>
<td>VDD_5S</td>
<td>P</td>
<td><strong>Vcc 5.0V Power for Group C.</strong> This pin supplies the 5V input tolerance circuit and the core power for the internal suspend circuit.</td>
</tr>
<tr>
<td>Vss or Gnd</td>
<td>P</td>
<td><strong>Ground</strong></td>
</tr>
</tbody>
</table>
### 2.3 Numerical Pin List

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>--</td>
<td>-</td>
</tr>
<tr>
<td>A2</td>
<td>PHLDAJ</td>
<td>O</td>
</tr>
<tr>
<td>A3</td>
<td>AD3</td>
<td>I/O</td>
</tr>
<tr>
<td>A4</td>
<td>AD6</td>
<td>I/O</td>
</tr>
<tr>
<td>A5</td>
<td>AD8</td>
<td>I/O</td>
</tr>
<tr>
<td>A6</td>
<td>AD12</td>
<td>I/O</td>
</tr>
<tr>
<td>A7</td>
<td>PAR</td>
<td>I/O</td>
</tr>
<tr>
<td>A8</td>
<td>TRDYJ</td>
<td>I/O</td>
</tr>
<tr>
<td>A9</td>
<td>AD17</td>
<td>I/O</td>
</tr>
<tr>
<td>A10</td>
<td>AD22</td>
<td>I/O</td>
</tr>
<tr>
<td>A11</td>
<td>AD25</td>
<td>I/O</td>
</tr>
<tr>
<td>A12</td>
<td>AD30</td>
<td>I/O</td>
</tr>
<tr>
<td>A13</td>
<td>REQJ3</td>
<td>I/O</td>
</tr>
<tr>
<td>A14</td>
<td>GNTJ3</td>
<td>O/I</td>
</tr>
<tr>
<td>A15</td>
<td>GNTJ3</td>
<td>O/I</td>
</tr>
<tr>
<td>A16</td>
<td>MPD2</td>
<td>I/O</td>
</tr>
<tr>
<td>A17</td>
<td>MPD0</td>
<td>I/O</td>
</tr>
<tr>
<td>A18</td>
<td>MD61</td>
<td>I/O</td>
</tr>
<tr>
<td>A19</td>
<td>MD29</td>
<td>I/O</td>
</tr>
<tr>
<td>A20</td>
<td>MD62</td>
<td>I/O</td>
</tr>
<tr>
<td>B1</td>
<td>BEJ0</td>
<td>I/I</td>
</tr>
<tr>
<td>B2</td>
<td>PHLDJ</td>
<td>I/I</td>
</tr>
<tr>
<td>B3</td>
<td>AD2</td>
<td>I/O</td>
</tr>
<tr>
<td>B4</td>
<td>AD5</td>
<td>I/O</td>
</tr>
<tr>
<td>B5</td>
<td>AD7</td>
<td>I/O</td>
</tr>
<tr>
<td>B6</td>
<td>AD11</td>
<td>I/O</td>
</tr>
<tr>
<td>B7</td>
<td>CBEJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>B8</td>
<td>DEVSELJ</td>
<td>I/O</td>
</tr>
<tr>
<td>B9</td>
<td>AD16</td>
<td>I/O</td>
</tr>
<tr>
<td>B10</td>
<td>AD21</td>
<td>I/O</td>
</tr>
<tr>
<td>B11</td>
<td>AD24</td>
<td>I/O</td>
</tr>
<tr>
<td>B12</td>
<td>AD29</td>
<td>I/O</td>
</tr>
<tr>
<td>B13</td>
<td>REQJ2</td>
<td>I/I</td>
</tr>
<tr>
<td>B14</td>
<td>GNTJ1</td>
<td>O/I</td>
</tr>
<tr>
<td>B15</td>
<td>MPD5</td>
<td>I/O</td>
</tr>
<tr>
<td>B16</td>
<td>MPD1</td>
<td>I/O</td>
</tr>
<tr>
<td>B17</td>
<td>MD63</td>
<td>I/O</td>
</tr>
<tr>
<td>B18</td>
<td>MD27</td>
<td>I/O</td>
</tr>
<tr>
<td>B19</td>
<td>MD60</td>
<td>I/O</td>
</tr>
<tr>
<td>B20</td>
<td>MD28</td>
<td>I/O</td>
</tr>
<tr>
<td>C1</td>
<td>BEJ3</td>
<td>I/I</td>
</tr>
<tr>
<td>C2</td>
<td>BEJ2</td>
<td>I/I</td>
</tr>
<tr>
<td>C3</td>
<td>BEJ1</td>
<td>I/I</td>
</tr>
<tr>
<td>C4</td>
<td>AD4</td>
<td>I/O</td>
</tr>
<tr>
<td>C5</td>
<td>CBEJ0</td>
<td>I/O</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C6</td>
<td>AD10</td>
<td>I/O</td>
</tr>
<tr>
<td>C7</td>
<td>AD15</td>
<td>I/O</td>
</tr>
<tr>
<td>C8</td>
<td>STOPJ</td>
<td>I/O</td>
</tr>
<tr>
<td>C9</td>
<td>CBEJ2</td>
<td>I/O</td>
</tr>
<tr>
<td>C10</td>
<td>AD20</td>
<td>I/O</td>
</tr>
<tr>
<td>C11</td>
<td>CBEJ3</td>
<td>I/O</td>
</tr>
<tr>
<td>C12</td>
<td>AD28</td>
<td>I/O</td>
</tr>
<tr>
<td>C13</td>
<td>REQJ1</td>
<td>I/I</td>
</tr>
<tr>
<td>C14</td>
<td>GNTJ0</td>
<td>O/I</td>
</tr>
<tr>
<td>C15</td>
<td>MPD4</td>
<td>I/O</td>
</tr>
<tr>
<td>C16</td>
<td>MD30</td>
<td>I/O</td>
</tr>
<tr>
<td>C17</td>
<td>MD25</td>
<td>I/O</td>
</tr>
<tr>
<td>C18</td>
<td>MD58</td>
<td>I/O</td>
</tr>
<tr>
<td>C19</td>
<td>MD26</td>
<td>I/O</td>
</tr>
<tr>
<td>C20</td>
<td>MD59</td>
<td>I/O</td>
</tr>
<tr>
<td>D1</td>
<td>BEJ6</td>
<td>I/I</td>
</tr>
<tr>
<td>D2</td>
<td>BEJ5</td>
<td>I/I</td>
</tr>
<tr>
<td>D3</td>
<td>BEJ4</td>
<td>I/I</td>
</tr>
<tr>
<td>D4</td>
<td>AD0</td>
<td>I/O</td>
</tr>
<tr>
<td>D5</td>
<td>AD1</td>
<td>I/O</td>
</tr>
<tr>
<td>D6</td>
<td>AD9</td>
<td>I/O</td>
</tr>
<tr>
<td>D7</td>
<td>AD14</td>
<td>I/O</td>
</tr>
<tr>
<td>D8</td>
<td>LOCKJ</td>
<td>I/O</td>
</tr>
<tr>
<td>D9</td>
<td>FRAMEJ</td>
<td>I/O</td>
</tr>
<tr>
<td>D10</td>
<td>AD19</td>
<td>I/O</td>
</tr>
<tr>
<td>D11</td>
<td>AD23</td>
<td>I/O</td>
</tr>
<tr>
<td>D12</td>
<td>AD27</td>
<td>I/O</td>
</tr>
<tr>
<td>D13</td>
<td>REQJ0</td>
<td>I/I</td>
</tr>
<tr>
<td>D14</td>
<td>MPD7</td>
<td>I/O</td>
</tr>
<tr>
<td>D15</td>
<td>MPD3</td>
<td>I/O</td>
</tr>
<tr>
<td>D16</td>
<td>MD55</td>
<td>I/O</td>
</tr>
<tr>
<td>D17</td>
<td>MD23</td>
<td>I/O</td>
</tr>
<tr>
<td>D18</td>
<td>MD56</td>
<td>I/O</td>
</tr>
<tr>
<td>D19</td>
<td>MD24</td>
<td>I/O</td>
</tr>
<tr>
<td>D20</td>
<td>MD57</td>
<td>I/O</td>
</tr>
<tr>
<td>E1</td>
<td>DCJ</td>
<td>I/I</td>
</tr>
<tr>
<td>E2</td>
<td>HITMJ</td>
<td>I/I</td>
</tr>
<tr>
<td>E3</td>
<td>EADJSJ</td>
<td>O/I</td>
</tr>
<tr>
<td>E4</td>
<td>BEJ7</td>
<td>I/I</td>
</tr>
<tr>
<td>E5</td>
<td>RSTJ</td>
<td>I/I</td>
</tr>
<tr>
<td>E6</td>
<td>PCIMRQJ</td>
<td>O/I</td>
</tr>
<tr>
<td>E7</td>
<td>AD13</td>
<td>I/O</td>
</tr>
<tr>
<td>E8</td>
<td>SERRJ</td>
<td>I/O</td>
</tr>
<tr>
<td>E9</td>
<td>IRDYJ</td>
<td>I/O</td>
</tr>
<tr>
<td>E10</td>
<td>AD18</td>
<td>I/O</td>
</tr>
</tbody>
</table>
### Numerical Pin List (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>E11</td>
<td>PCLKIN</td>
<td>I</td>
</tr>
<tr>
<td>E12</td>
<td>AD26</td>
<td>I/O</td>
</tr>
<tr>
<td>E13</td>
<td>AD31</td>
<td>I/O</td>
</tr>
<tr>
<td>E14</td>
<td>MD06</td>
<td>I/O</td>
</tr>
<tr>
<td>E15</td>
<td>MD31</td>
<td>I/O</td>
</tr>
<tr>
<td>E16</td>
<td>MD20</td>
<td>I/O</td>
</tr>
<tr>
<td>E17</td>
<td>MD53</td>
<td>I/O</td>
</tr>
<tr>
<td>E18</td>
<td>MD21</td>
<td>I/O</td>
</tr>
<tr>
<td>E19</td>
<td>MD54</td>
<td>I/O</td>
</tr>
<tr>
<td>E20</td>
<td>MD22</td>
<td>I/O</td>
</tr>
<tr>
<td>F1</td>
<td>BRDYJ</td>
<td>O</td>
</tr>
<tr>
<td>F2</td>
<td>BOFFJ</td>
<td>O</td>
</tr>
<tr>
<td>F3</td>
<td>SMIACTJ</td>
<td>I</td>
</tr>
<tr>
<td>F4</td>
<td>HLOCKJ</td>
<td>I</td>
</tr>
<tr>
<td>F5</td>
<td>ADSJ</td>
<td>I</td>
</tr>
<tr>
<td>F6</td>
<td>VCC_B</td>
<td>P</td>
</tr>
<tr>
<td>F14</td>
<td>VCC_C</td>
<td>P</td>
</tr>
<tr>
<td>F15</td>
<td>VCC_C</td>
<td>P</td>
</tr>
<tr>
<td>F16</td>
<td>MD50</td>
<td>I/O</td>
</tr>
<tr>
<td>F17</td>
<td>MD18</td>
<td>I/O</td>
</tr>
<tr>
<td>F18</td>
<td>MD51</td>
<td>I/O</td>
</tr>
<tr>
<td>F19</td>
<td>MD19</td>
<td>I/O</td>
</tr>
<tr>
<td>F20</td>
<td>MD52</td>
<td>I/O</td>
</tr>
<tr>
<td>G1</td>
<td>HD63</td>
<td>I/O</td>
</tr>
<tr>
<td>G2</td>
<td>CACHEJ</td>
<td>I</td>
</tr>
<tr>
<td>G3</td>
<td>AHOLOD</td>
<td>O</td>
</tr>
<tr>
<td>G4</td>
<td>KENJ</td>
<td>O</td>
</tr>
<tr>
<td>G5</td>
<td>NAJ</td>
<td>O</td>
</tr>
<tr>
<td>G6</td>
<td>VCC_A</td>
<td>P</td>
</tr>
<tr>
<td>G15</td>
<td>VCC_C</td>
<td>P</td>
</tr>
<tr>
<td>G16</td>
<td>MD15</td>
<td>I/O</td>
</tr>
<tr>
<td>G17</td>
<td>MD48</td>
<td>I/O</td>
</tr>
<tr>
<td>G18</td>
<td>MD16</td>
<td>I/O</td>
</tr>
<tr>
<td>G19</td>
<td>MD49</td>
<td>I/O</td>
</tr>
<tr>
<td>G20</td>
<td>MD17</td>
<td>I/O</td>
</tr>
<tr>
<td>H1</td>
<td>HD60</td>
<td>I/O</td>
</tr>
<tr>
<td>H2</td>
<td>HD61</td>
<td>I/O</td>
</tr>
<tr>
<td>H3</td>
<td>HD62</td>
<td>I/O</td>
</tr>
<tr>
<td>H4</td>
<td>WRJ</td>
<td>I</td>
</tr>
<tr>
<td>H5</td>
<td>MOJ</td>
<td>I</td>
</tr>
<tr>
<td>H6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H16</td>
<td>MD45</td>
<td>I/O</td>
</tr>
<tr>
<td>H17</td>
<td>MD13</td>
<td>I/O</td>
</tr>
<tr>
<td>H18</td>
<td>MD46</td>
<td>I/O</td>
</tr>
<tr>
<td>H19</td>
<td>MD14</td>
<td>I/O</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>H20</td>
<td>MD47</td>
<td>I/O</td>
</tr>
<tr>
<td>J1</td>
<td>HD55</td>
<td>I/O</td>
</tr>
<tr>
<td>J2</td>
<td>HD56</td>
<td>I/O</td>
</tr>
<tr>
<td>J3</td>
<td>HD57</td>
<td>I/O</td>
</tr>
<tr>
<td>J4</td>
<td>HD58</td>
<td>I/O</td>
</tr>
<tr>
<td>J5</td>
<td>HD59</td>
<td>I/O</td>
</tr>
<tr>
<td>J8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J16</td>
<td>MD10</td>
<td>I/O</td>
</tr>
<tr>
<td>J17</td>
<td>MD43</td>
<td>I/O</td>
</tr>
<tr>
<td>J18</td>
<td>MD11</td>
<td>I/O</td>
</tr>
<tr>
<td>J19</td>
<td>MD44</td>
<td>I/O</td>
</tr>
<tr>
<td>J20</td>
<td>MD12</td>
<td>I/O</td>
</tr>
<tr>
<td>K1</td>
<td>HD51</td>
<td>I/O</td>
</tr>
<tr>
<td>K2</td>
<td>HD52</td>
<td>I/O</td>
</tr>
<tr>
<td>K3</td>
<td>HD53</td>
<td>I/O</td>
</tr>
<tr>
<td>K4</td>
<td>HD54</td>
<td>I/O</td>
</tr>
<tr>
<td>K5</td>
<td>HCLKin</td>
<td>I</td>
</tr>
<tr>
<td>K8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K16</td>
<td>MD40</td>
<td>I/O</td>
</tr>
<tr>
<td>K17</td>
<td>MD8</td>
<td>I/O</td>
</tr>
<tr>
<td>K18</td>
<td>MD41</td>
<td>I/O</td>
</tr>
<tr>
<td>K19</td>
<td>MD9</td>
<td>I/O</td>
</tr>
<tr>
<td>K20</td>
<td>MD42</td>
<td>I/O</td>
</tr>
<tr>
<td>L1</td>
<td>HD46</td>
<td>I/O</td>
</tr>
<tr>
<td>L2</td>
<td>HD47</td>
<td>I/O</td>
</tr>
<tr>
<td>L3</td>
<td>HD48</td>
<td>I/O</td>
</tr>
<tr>
<td>L4</td>
<td>HD49</td>
<td>I/O</td>
</tr>
<tr>
<td>L5</td>
<td>HD50</td>
<td>I/O</td>
</tr>
<tr>
<td>L8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L16</td>
<td>MD5</td>
<td>I/O</td>
</tr>
<tr>
<td>L17</td>
<td>MD38</td>
<td>I/O</td>
</tr>
<tr>
<td>L18</td>
<td>MD6</td>
<td>I/O</td>
</tr>
<tr>
<td>L19</td>
<td>MD39</td>
<td>I/O</td>
</tr>
<tr>
<td>L20</td>
<td>MD7</td>
<td>I/O</td>
</tr>
<tr>
<td>M1</td>
<td>HD41</td>
<td>I/O</td>
</tr>
</tbody>
</table>
### Numerical Pin List (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2</td>
<td>HD42</td>
<td>I/O</td>
</tr>
<tr>
<td>M3</td>
<td>HD43</td>
<td>I/O</td>
</tr>
<tr>
<td>M4</td>
<td>HD44</td>
<td>I/O</td>
</tr>
<tr>
<td>M5</td>
<td>HD45</td>
<td>I/O</td>
</tr>
<tr>
<td>M8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M16</td>
<td>MD35</td>
<td>I/O</td>
</tr>
<tr>
<td>M17</td>
<td>MD3</td>
<td>I/O</td>
</tr>
<tr>
<td>M18</td>
<td>MD36</td>
<td>I/O</td>
</tr>
<tr>
<td>M19</td>
<td>MD4</td>
<td>I/O</td>
</tr>
<tr>
<td>M20</td>
<td>MD37</td>
<td>I/O</td>
</tr>
<tr>
<td>N1</td>
<td>HD36</td>
<td>I/O</td>
</tr>
<tr>
<td>N2</td>
<td>HD37</td>
<td>I/O</td>
</tr>
<tr>
<td>N3</td>
<td>HD38</td>
<td>I/O</td>
</tr>
<tr>
<td>N4</td>
<td>HD39</td>
<td>I/O</td>
</tr>
<tr>
<td>N5</td>
<td>HD40</td>
<td>I/O</td>
</tr>
<tr>
<td>N8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N15</td>
<td>VDD5S</td>
<td>P</td>
</tr>
<tr>
<td>N16</td>
<td>REQJ4</td>
<td>I/O</td>
</tr>
<tr>
<td>N17</td>
<td>GNTJ4</td>
<td>O</td>
</tr>
<tr>
<td>N18</td>
<td>MD1</td>
<td>I/O</td>
</tr>
<tr>
<td>N19</td>
<td>MD34</td>
<td>I/O</td>
</tr>
<tr>
<td>N20</td>
<td>MD2</td>
<td>I/O</td>
</tr>
<tr>
<td>P1</td>
<td>HD31</td>
<td>I/O</td>
</tr>
<tr>
<td>P2</td>
<td>HD32</td>
<td>I/O</td>
</tr>
<tr>
<td>P3</td>
<td>HD33</td>
<td>I/O</td>
</tr>
<tr>
<td>P4</td>
<td>HD34</td>
<td>I/O</td>
</tr>
<tr>
<td>P5</td>
<td>HD35</td>
<td>I/O</td>
</tr>
<tr>
<td>P6</td>
<td>VCC A</td>
<td>P</td>
</tr>
<tr>
<td>P15</td>
<td>VCC C</td>
<td>P</td>
</tr>
<tr>
<td>P16</td>
<td>32K</td>
<td>I</td>
</tr>
<tr>
<td>P17</td>
<td>SUSPENDJ</td>
<td>I</td>
</tr>
<tr>
<td>P18</td>
<td>MD32</td>
<td>I/O</td>
</tr>
<tr>
<td>P19</td>
<td>MD0</td>
<td>I/O</td>
</tr>
<tr>
<td>P20</td>
<td>MD33</td>
<td>I/O</td>
</tr>
<tr>
<td>R1</td>
<td>HD26</td>
<td>I/O</td>
</tr>
<tr>
<td>R2</td>
<td>HD27</td>
<td>I/O</td>
</tr>
<tr>
<td>R3</td>
<td>HD28</td>
<td>I/O</td>
</tr>
<tr>
<td>R4</td>
<td>HD29</td>
<td>I/O</td>
</tr>
<tr>
<td>R5</td>
<td>HD30</td>
<td>I/O</td>
</tr>
<tr>
<td>R6</td>
<td>VDD5</td>
<td>P</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>R7</td>
<td>VCC A</td>
<td>P</td>
</tr>
<tr>
<td>R14</td>
<td>VCC B</td>
<td>P</td>
</tr>
<tr>
<td>R15</td>
<td>VCC C</td>
<td>P</td>
</tr>
<tr>
<td>R16</td>
<td>RASJ6</td>
<td>O</td>
</tr>
<tr>
<td>R17</td>
<td>RASJ7</td>
<td>O</td>
</tr>
<tr>
<td>R18</td>
<td>CASJ2</td>
<td>O</td>
</tr>
<tr>
<td>R19</td>
<td>CASJ7</td>
<td>O</td>
</tr>
<tr>
<td>R20</td>
<td>CASJ3</td>
<td>O</td>
</tr>
<tr>
<td>T1</td>
<td>HD21</td>
<td>I/O</td>
</tr>
<tr>
<td>T2</td>
<td>HD22</td>
<td>I/O</td>
</tr>
<tr>
<td>T3</td>
<td>HD23</td>
<td>I/O</td>
</tr>
<tr>
<td>T4</td>
<td>HD24</td>
<td>I/O</td>
</tr>
<tr>
<td>T5</td>
<td>HD25</td>
<td>I/O</td>
</tr>
<tr>
<td>T6</td>
<td>HD0</td>
<td>I/O</td>
</tr>
<tr>
<td>T7</td>
<td>A12</td>
<td>I/O</td>
</tr>
<tr>
<td>T8</td>
<td>A5</td>
<td>I/O</td>
</tr>
<tr>
<td>T9</td>
<td>GWEJ</td>
<td>O</td>
</tr>
<tr>
<td>T10</td>
<td>COEJ</td>
<td>O</td>
</tr>
<tr>
<td>T11</td>
<td>CADVJ</td>
<td>O</td>
</tr>
<tr>
<td>T12</td>
<td>TWEJ</td>
<td>O</td>
</tr>
<tr>
<td>T13</td>
<td>MAA0</td>
<td>O</td>
</tr>
<tr>
<td>T14</td>
<td>MAA1</td>
<td>O</td>
</tr>
<tr>
<td>T15</td>
<td>SCASJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>T16</td>
<td>SRASJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>T17</td>
<td>MWEJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>T18</td>
<td>RASJ1</td>
<td>O</td>
</tr>
<tr>
<td>T19</td>
<td>RASJ0</td>
<td>O</td>
</tr>
<tr>
<td>T20</td>
<td>CASJ6</td>
<td>O</td>
</tr>
<tr>
<td>U1</td>
<td>HD16</td>
<td>I/O</td>
</tr>
<tr>
<td>U2</td>
<td>HD17</td>
<td>I/O</td>
</tr>
<tr>
<td>U3</td>
<td>HD18</td>
<td>I/O</td>
</tr>
<tr>
<td>U4</td>
<td>HD19</td>
<td>I/O</td>
</tr>
<tr>
<td>U5</td>
<td>HD20</td>
<td>I/O</td>
</tr>
<tr>
<td>U6</td>
<td>HD1</td>
<td>I/O</td>
</tr>
<tr>
<td>U7</td>
<td>A13</td>
<td>I/O</td>
</tr>
<tr>
<td>U8</td>
<td>A8</td>
<td>I/O</td>
</tr>
<tr>
<td>U9</td>
<td>CCSJ</td>
<td>O</td>
</tr>
<tr>
<td>T10</td>
<td>BWEJ</td>
<td>O</td>
</tr>
<tr>
<td>U11</td>
<td>CADSJ</td>
<td>O</td>
</tr>
<tr>
<td>U12</td>
<td>TIO0</td>
<td>I/O</td>
</tr>
<tr>
<td>U13</td>
<td>TIO1</td>
<td>I/O</td>
</tr>
<tr>
<td>U14</td>
<td>MAB0</td>
<td>O</td>
</tr>
<tr>
<td>U15</td>
<td>MAB1</td>
<td>O</td>
</tr>
<tr>
<td>U16</td>
<td>MA5</td>
<td>O</td>
</tr>
<tr>
<td>U17</td>
<td>MWEJ</td>
<td>I/O</td>
</tr>
<tr>
<td>U18</td>
<td>RASJ4</td>
<td>O</td>
</tr>
<tr>
<td>U19</td>
<td>RASJ3</td>
<td>O</td>
</tr>
<tr>
<td>U20</td>
<td>RASJ2</td>
<td>O</td>
</tr>
<tr>
<td>V1</td>
<td>HD15</td>
<td>I/O</td>
</tr>
<tr>
<td>V2</td>
<td>HD14</td>
<td>I/O</td>
</tr>
</tbody>
</table>
### Numerical Pin List (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>V3</td>
<td>HD13</td>
<td>I/O</td>
</tr>
<tr>
<td>V4</td>
<td>HD6</td>
<td>I/O</td>
</tr>
<tr>
<td>V5</td>
<td>HD3</td>
<td>I/O</td>
</tr>
<tr>
<td>V6</td>
<td>A17</td>
<td>I/O</td>
</tr>
<tr>
<td>V7</td>
<td>A14</td>
<td>I/O</td>
</tr>
<tr>
<td>V8</td>
<td>A10</td>
<td>I/O</td>
</tr>
<tr>
<td>V9</td>
<td>A4</td>
<td>I/O</td>
</tr>
<tr>
<td>V10</td>
<td>A29</td>
<td>I/O</td>
</tr>
<tr>
<td>V11</td>
<td>A25</td>
<td>I/O</td>
</tr>
<tr>
<td>V12</td>
<td>A24</td>
<td>I/O</td>
</tr>
<tr>
<td>V137</td>
<td>A23</td>
<td>I/O</td>
</tr>
<tr>
<td>V14</td>
<td>TIO2</td>
<td>I/O</td>
</tr>
<tr>
<td>V15</td>
<td>MA2</td>
<td>O</td>
</tr>
<tr>
<td>V16</td>
<td>MA4</td>
<td>O</td>
</tr>
<tr>
<td>V17</td>
<td>MA8</td>
<td>O</td>
</tr>
<tr>
<td>V18</td>
<td>CASJ5</td>
<td>O</td>
</tr>
<tr>
<td>V19</td>
<td>CASJ1</td>
<td>O</td>
</tr>
<tr>
<td>V20</td>
<td>RASJ5</td>
<td>O</td>
</tr>
<tr>
<td>W1</td>
<td>HD12</td>
<td>I/O</td>
</tr>
<tr>
<td>W2</td>
<td>HD11</td>
<td>I/O</td>
</tr>
<tr>
<td>W3</td>
<td>HD10</td>
<td>I/O</td>
</tr>
<tr>
<td>W4</td>
<td>HD5</td>
<td>I/O</td>
</tr>
<tr>
<td>W5</td>
<td>HD2</td>
<td>I/O</td>
</tr>
<tr>
<td>W6</td>
<td>A18</td>
<td>I/O</td>
</tr>
<tr>
<td>W7</td>
<td>A15</td>
<td>I/O</td>
</tr>
<tr>
<td>W8</td>
<td>A11</td>
<td>I/O</td>
</tr>
<tr>
<td>W9</td>
<td>A7</td>
<td>I/O</td>
</tr>
<tr>
<td>W10</td>
<td>A30</td>
<td>I/O</td>
</tr>
<tr>
<td>W11</td>
<td>A31</td>
<td>I/O</td>
</tr>
<tr>
<td>W12</td>
<td>A22</td>
<td>I/O</td>
</tr>
<tr>
<td>W13</td>
<td>A21</td>
<td>I/O</td>
</tr>
<tr>
<td>W14</td>
<td>TIO4</td>
<td>I/O</td>
</tr>
<tr>
<td>W15</td>
<td>TIO6</td>
<td>I/O</td>
</tr>
<tr>
<td>W16</td>
<td>MA3</td>
<td>O</td>
</tr>
<tr>
<td>W17</td>
<td>MA7</td>
<td>O</td>
</tr>
<tr>
<td>W18</td>
<td>MA10</td>
<td>O</td>
</tr>
<tr>
<td>W19</td>
<td>CASJ0</td>
<td>O</td>
</tr>
<tr>
<td>W20</td>
<td>CASJ4</td>
<td>O</td>
</tr>
<tr>
<td>Y1</td>
<td>HD9</td>
<td>I/O</td>
</tr>
<tr>
<td>Y2</td>
<td>HD8</td>
<td>I/O</td>
</tr>
<tr>
<td>Y3</td>
<td>HD7</td>
<td>I/O</td>
</tr>
<tr>
<td>Y4</td>
<td>HD4</td>
<td>I/O</td>
</tr>
<tr>
<td>Y5</td>
<td>A20</td>
<td>I/O</td>
</tr>
<tr>
<td>Y6</td>
<td>A19</td>
<td>I/O</td>
</tr>
<tr>
<td>Y7</td>
<td>A16</td>
<td>I/O</td>
</tr>
<tr>
<td>Y8</td>
<td>A9</td>
<td>I/O</td>
</tr>
<tr>
<td>Y9</td>
<td>A6</td>
<td>I/O</td>
</tr>
<tr>
<td>Y10</td>
<td>A3</td>
<td>I/O</td>
</tr>
<tr>
<td>Y11</td>
<td>A28</td>
<td>I/O</td>
</tr>
<tr>
<td>Y12</td>
<td>A26</td>
<td>I/O</td>
</tr>
<tr>
<td>Y13</td>
<td>A27</td>
<td>I/O</td>
</tr>
<tr>
<td>Y14</td>
<td>TIO3</td>
<td>I/O</td>
</tr>
<tr>
<td>Y15</td>
<td>TIO5</td>
<td>I/O</td>
</tr>
<tr>
<td>Y16</td>
<td>TIO7</td>
<td>I/O</td>
</tr>
<tr>
<td>Y17</td>
<td>MA6</td>
<td>O</td>
</tr>
<tr>
<td>Y18</td>
<td>MA9</td>
<td>O</td>
</tr>
<tr>
<td>Y19</td>
<td>MA11</td>
<td>O</td>
</tr>
<tr>
<td>Y20</td>
<td>TIO8</td>
<td>I/O</td>
</tr>
</tbody>
</table>
## 2.4 Alphabetical Pin List

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>--</td>
<td>-</td>
</tr>
<tr>
<td>P16</td>
<td>32K</td>
<td>I</td>
</tr>
<tr>
<td>Y10</td>
<td>A3</td>
<td>I/O</td>
</tr>
<tr>
<td>V9</td>
<td>A4</td>
<td>I/O</td>
</tr>
<tr>
<td>T8</td>
<td>A5</td>
<td>I/O</td>
</tr>
<tr>
<td>Y9</td>
<td>A6</td>
<td>I/O</td>
</tr>
<tr>
<td>W9</td>
<td>A7</td>
<td>I/O</td>
</tr>
<tr>
<td>U8</td>
<td>A8</td>
<td>I/O</td>
</tr>
<tr>
<td>Y8</td>
<td>A9</td>
<td>I/O</td>
</tr>
<tr>
<td>V8</td>
<td>A10</td>
<td>I/O</td>
</tr>
<tr>
<td>W8</td>
<td>A11</td>
<td>I/O</td>
</tr>
<tr>
<td>T7</td>
<td>A12</td>
<td>I/O</td>
</tr>
<tr>
<td>U7</td>
<td>A13</td>
<td>I/O</td>
</tr>
<tr>
<td>V7</td>
<td>A14</td>
<td>I/O</td>
</tr>
<tr>
<td>W7</td>
<td>A15</td>
<td>I/O</td>
</tr>
<tr>
<td>Y7</td>
<td>A16</td>
<td>I/O</td>
</tr>
<tr>
<td>V6</td>
<td>A17</td>
<td>I/O</td>
</tr>
<tr>
<td>W6</td>
<td>A18</td>
<td>I/O</td>
</tr>
<tr>
<td>Y6</td>
<td>A19</td>
<td>I/O</td>
</tr>
<tr>
<td>Y5</td>
<td>A20</td>
<td>I/O</td>
</tr>
<tr>
<td>W13</td>
<td>A21</td>
<td>I/O</td>
</tr>
<tr>
<td>W12</td>
<td>A22</td>
<td>I/O</td>
</tr>
<tr>
<td>V137</td>
<td>A23</td>
<td>I/O</td>
</tr>
<tr>
<td>V12</td>
<td>A24</td>
<td>I/O</td>
</tr>
<tr>
<td>V11</td>
<td>A25</td>
<td>I/O</td>
</tr>
<tr>
<td>Y12</td>
<td>A26</td>
<td>I/O</td>
</tr>
<tr>
<td>Y13</td>
<td>A27</td>
<td>I/O</td>
</tr>
<tr>
<td>Y11</td>
<td>A28</td>
<td>I/O</td>
</tr>
<tr>
<td>V10</td>
<td>A29</td>
<td>I/O</td>
</tr>
<tr>
<td>W10</td>
<td>A30</td>
<td>I/O</td>
</tr>
<tr>
<td>W11</td>
<td>A31</td>
<td>I/O</td>
</tr>
<tr>
<td>D4</td>
<td>A00</td>
<td>I/O</td>
</tr>
<tr>
<td>D5</td>
<td>A01</td>
<td>I/O</td>
</tr>
<tr>
<td>B3</td>
<td>A02</td>
<td>I/O</td>
</tr>
<tr>
<td>A3</td>
<td>A03</td>
<td>I/O</td>
</tr>
<tr>
<td>C4</td>
<td>A04</td>
<td>I/O</td>
</tr>
<tr>
<td>B4</td>
<td>A05</td>
<td>I/O</td>
</tr>
<tr>
<td>A4</td>
<td>A06</td>
<td>I/O</td>
</tr>
<tr>
<td>B5</td>
<td>A07</td>
<td>I/O</td>
</tr>
<tr>
<td>A5</td>
<td>A08</td>
<td>I/O</td>
</tr>
<tr>
<td>D6</td>
<td>A09</td>
<td>I/O</td>
</tr>
<tr>
<td>C5</td>
<td>A10</td>
<td>I/O</td>
</tr>
<tr>
<td>B6</td>
<td>A11</td>
<td>I/O</td>
</tr>
<tr>
<td>A6</td>
<td>A12</td>
<td>I/O</td>
</tr>
<tr>
<td>E7</td>
<td>AD13</td>
<td>I/O</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td>AD14</td>
<td>I/O</td>
</tr>
<tr>
<td>C7</td>
<td>AD15</td>
<td>I/O</td>
</tr>
<tr>
<td>B9</td>
<td>AD16</td>
<td>I/O</td>
</tr>
<tr>
<td>A9</td>
<td>AD17</td>
<td>I/O</td>
</tr>
<tr>
<td>E10</td>
<td>AD18</td>
<td>I/O</td>
</tr>
<tr>
<td>D10</td>
<td>AD19</td>
<td>I/O</td>
</tr>
<tr>
<td>C10</td>
<td>AD20</td>
<td>I/O</td>
</tr>
<tr>
<td>B10</td>
<td>AD21</td>
<td>I/O</td>
</tr>
<tr>
<td>A10</td>
<td>AD22</td>
<td>I/O</td>
</tr>
<tr>
<td>D11</td>
<td>AD23</td>
<td>I/O</td>
</tr>
<tr>
<td>B11</td>
<td>AD24</td>
<td>I/O</td>
</tr>
<tr>
<td>A11</td>
<td>AD25</td>
<td>I/O</td>
</tr>
<tr>
<td>E12</td>
<td>AD26</td>
<td>I/O</td>
</tr>
<tr>
<td>D12</td>
<td>AD27</td>
<td>I/O</td>
</tr>
<tr>
<td>C12</td>
<td>AD28</td>
<td>I/O</td>
</tr>
<tr>
<td>B12</td>
<td>AD29</td>
<td>I/O</td>
</tr>
<tr>
<td>A12</td>
<td>AD30</td>
<td>I/O</td>
</tr>
<tr>
<td>E13</td>
<td>AD31</td>
<td>I/O</td>
</tr>
<tr>
<td>F5</td>
<td>ADSJ</td>
<td>I</td>
</tr>
<tr>
<td>G3</td>
<td>AHOLOD</td>
<td>O</td>
</tr>
<tr>
<td>B1</td>
<td>BEJ0</td>
<td>I</td>
</tr>
<tr>
<td>C3</td>
<td>BEJ1</td>
<td>I</td>
</tr>
<tr>
<td>C2</td>
<td>BEJ2</td>
<td>I</td>
</tr>
<tr>
<td>C1</td>
<td>BEJ3</td>
<td>I</td>
</tr>
<tr>
<td>D3</td>
<td>BEJ4</td>
<td>I</td>
</tr>
<tr>
<td>D2</td>
<td>BEJ5</td>
<td>I</td>
</tr>
<tr>
<td>D1</td>
<td>BEJ6</td>
<td>I</td>
</tr>
<tr>
<td>E4</td>
<td>BEJ7</td>
<td>I</td>
</tr>
<tr>
<td>F2</td>
<td>BOFFJ</td>
<td>O</td>
</tr>
<tr>
<td>F1</td>
<td>BRDYJ</td>
<td>O</td>
</tr>
<tr>
<td>U10</td>
<td>BWEJ</td>
<td>O</td>
</tr>
<tr>
<td>G2</td>
<td>CACHEJ</td>
<td>I</td>
</tr>
<tr>
<td>U11</td>
<td>CADSJ</td>
<td>O</td>
</tr>
<tr>
<td>T11</td>
<td>CADVJ</td>
<td>O</td>
</tr>
<tr>
<td>W19</td>
<td>CASJ0</td>
<td>O</td>
</tr>
<tr>
<td>V19</td>
<td>CASJ1</td>
<td>O</td>
</tr>
<tr>
<td>R18</td>
<td>CASJ2</td>
<td>O</td>
</tr>
<tr>
<td>R20</td>
<td>CASJ3</td>
<td>O</td>
</tr>
<tr>
<td>W20</td>
<td>CASJ4</td>
<td>O</td>
</tr>
<tr>
<td>V18</td>
<td>CASJ5</td>
<td>O</td>
</tr>
<tr>
<td>T20</td>
<td>CASJ6</td>
<td>O</td>
</tr>
<tr>
<td>R19</td>
<td>CASJ7</td>
<td>O</td>
</tr>
<tr>
<td>C5</td>
<td>CBEJ0</td>
<td>I/O</td>
</tr>
<tr>
<td>B7</td>
<td>CBEJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>C9</td>
<td>CBEJ2</td>
<td>I/O</td>
</tr>
</tbody>
</table>
### Alphabetical Pin List (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C11</td>
<td>CBEJ3</td>
<td>I/O</td>
</tr>
<tr>
<td>U9</td>
<td>CCSJ</td>
<td>O</td>
</tr>
<tr>
<td>T10</td>
<td>COEJ</td>
<td>O</td>
</tr>
<tr>
<td>E1</td>
<td>DCJ</td>
<td>I</td>
</tr>
<tr>
<td>B8</td>
<td>DEVSELJ</td>
<td>I/O</td>
</tr>
<tr>
<td>E3</td>
<td>EADSJ</td>
<td>O</td>
</tr>
<tr>
<td>D9</td>
<td>FRAMEJ</td>
<td>I/O</td>
</tr>
<tr>
<td>H10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>J13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>K13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>L13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M10</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M11</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M12</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>M13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M9</td>
<td>GND</td>
<td>P</td>
</tr>
<tr>
<td>N10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CT4</td>
<td>GNTJ0</td>
<td>O</td>
</tr>
<tr>
<td>B14</td>
<td>GNTJ1</td>
<td>O</td>
</tr>
<tr>
<td>A14</td>
<td>GNTJ2</td>
<td>O</td>
</tr>
<tr>
<td>A15</td>
<td>GNTJ3</td>
<td>O</td>
</tr>
<tr>
<td>N17</td>
<td>GNTJ4</td>
<td>O</td>
</tr>
<tr>
<td>T9</td>
<td>GWEJ</td>
<td>O</td>
</tr>
<tr>
<td>K5</td>
<td>HCLKIN</td>
<td>I</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>T6</td>
<td>HD0</td>
<td>I/O</td>
</tr>
<tr>
<td>U6</td>
<td>HD1</td>
<td>I/O</td>
</tr>
<tr>
<td>W5</td>
<td>HD2</td>
<td>I/O</td>
</tr>
<tr>
<td>V5</td>
<td>HD3</td>
<td>I/O</td>
</tr>
<tr>
<td>Y4</td>
<td>HD4</td>
<td>I/O</td>
</tr>
<tr>
<td>W4</td>
<td>HD5</td>
<td>I/O</td>
</tr>
<tr>
<td>V4</td>
<td>HD6</td>
<td>I/O</td>
</tr>
<tr>
<td>Y3</td>
<td>HD7</td>
<td>I/O</td>
</tr>
<tr>
<td>Y2</td>
<td>HD8</td>
<td>I/O</td>
</tr>
<tr>
<td>Y1</td>
<td>HD9</td>
<td>I/O</td>
</tr>
<tr>
<td>W3</td>
<td>HD10</td>
<td>I/O</td>
</tr>
<tr>
<td>W2</td>
<td>HD11</td>
<td>I/O</td>
</tr>
<tr>
<td>W1</td>
<td>HD12</td>
<td>I/O</td>
</tr>
<tr>
<td>V3</td>
<td>HD13</td>
<td>I/O</td>
</tr>
<tr>
<td>V2</td>
<td>HD14</td>
<td>I/O</td>
</tr>
<tr>
<td>V1</td>
<td>HD15</td>
<td>I/O</td>
</tr>
<tr>
<td>U1</td>
<td>HD16</td>
<td>I/O</td>
</tr>
<tr>
<td>U2</td>
<td>HD17</td>
<td>I/O</td>
</tr>
<tr>
<td>U3</td>
<td>HD18</td>
<td>I/O</td>
</tr>
<tr>
<td>U4</td>
<td>HD19</td>
<td>I/O</td>
</tr>
<tr>
<td>U5</td>
<td>HD20</td>
<td>I/O</td>
</tr>
<tr>
<td>T1</td>
<td>HD21</td>
<td>I/O</td>
</tr>
<tr>
<td>T2</td>
<td>HD22</td>
<td>I/O</td>
</tr>
<tr>
<td>T3</td>
<td>HD23</td>
<td>I/O</td>
</tr>
<tr>
<td>T4</td>
<td>HD24</td>
<td>I/O</td>
</tr>
<tr>
<td>T5</td>
<td>HD25</td>
<td>I/O</td>
</tr>
<tr>
<td>R1</td>
<td>HD26</td>
<td>I/O</td>
</tr>
<tr>
<td>R2</td>
<td>HD27</td>
<td>I/O</td>
</tr>
<tr>
<td>R3</td>
<td>HD28</td>
<td>I/O</td>
</tr>
<tr>
<td>R4</td>
<td>HD29</td>
<td>I/O</td>
</tr>
<tr>
<td>R5</td>
<td>HD30</td>
<td>I/O</td>
</tr>
<tr>
<td>P1</td>
<td>HD31</td>
<td>I/O</td>
</tr>
<tr>
<td>P2</td>
<td>HD32</td>
<td>I/O</td>
</tr>
<tr>
<td>P3</td>
<td>HD33</td>
<td>I/O</td>
</tr>
<tr>
<td>P4</td>
<td>HD34</td>
<td>I/O</td>
</tr>
<tr>
<td>P5</td>
<td>HD35</td>
<td>I/O</td>
</tr>
<tr>
<td>N1</td>
<td>HD36</td>
<td>I/O</td>
</tr>
<tr>
<td>N2</td>
<td>HD37</td>
<td>I/O</td>
</tr>
<tr>
<td>N3</td>
<td>HD38</td>
<td>I/O</td>
</tr>
<tr>
<td>N4</td>
<td>HD39</td>
<td>I/O</td>
</tr>
<tr>
<td>N5</td>
<td>HD40</td>
<td>I/O</td>
</tr>
<tr>
<td>M1</td>
<td>HD41</td>
<td>I/O</td>
</tr>
<tr>
<td>M2</td>
<td>HD42</td>
<td>I/O</td>
</tr>
<tr>
<td>M3</td>
<td>HD43</td>
<td>I/O</td>
</tr>
<tr>
<td>M4</td>
<td>HD44</td>
<td>I/O</td>
</tr>
<tr>
<td>M5</td>
<td>HD45</td>
<td>I/O</td>
</tr>
<tr>
<td>L1</td>
<td>HD46</td>
<td>I/O</td>
</tr>
<tr>
<td>L2</td>
<td>HD47</td>
<td>I/O</td>
</tr>
<tr>
<td>L3</td>
<td>HD48</td>
<td>I/O</td>
</tr>
<tr>
<td>L4</td>
<td>HD49</td>
<td>I/O</td>
</tr>
</tbody>
</table>
## Alphabetical Pin List (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>L5</td>
<td>HD50</td>
<td>I/O</td>
</tr>
<tr>
<td>K1</td>
<td>HD51</td>
<td>I/O</td>
</tr>
<tr>
<td>K2</td>
<td>HD52</td>
<td>I/O</td>
</tr>
<tr>
<td>K3</td>
<td>HD53</td>
<td>I/O</td>
</tr>
<tr>
<td>K4</td>
<td>HD54</td>
<td>I/O</td>
</tr>
<tr>
<td>J1</td>
<td>HD55</td>
<td>I/O</td>
</tr>
<tr>
<td>J2</td>
<td>HD56</td>
<td>I/O</td>
</tr>
<tr>
<td>J3</td>
<td>HD57</td>
<td>I/O</td>
</tr>
<tr>
<td>J4</td>
<td>HD58</td>
<td>I/O</td>
</tr>
<tr>
<td>J5</td>
<td>HD59</td>
<td>I/O</td>
</tr>
<tr>
<td>H1</td>
<td>HD60</td>
<td>I/O</td>
</tr>
<tr>
<td>H2</td>
<td>HD61</td>
<td>I/O</td>
</tr>
<tr>
<td>H3</td>
<td>HD62</td>
<td>I/O</td>
</tr>
<tr>
<td>G1</td>
<td>HD63</td>
<td>I/O</td>
</tr>
<tr>
<td>E2</td>
<td>HITMJ</td>
<td>I</td>
</tr>
<tr>
<td>F4</td>
<td>HLOCKJ</td>
<td>I</td>
</tr>
<tr>
<td>E9</td>
<td>IRDYJ</td>
<td>I/O</td>
</tr>
<tr>
<td>G4</td>
<td>KENJ</td>
<td>O</td>
</tr>
<tr>
<td>D8</td>
<td>LOCKJ</td>
<td>I/O</td>
</tr>
<tr>
<td>V15</td>
<td>MA2</td>
<td>O</td>
</tr>
<tr>
<td>W16</td>
<td>MA3</td>
<td>O</td>
</tr>
<tr>
<td>V16</td>
<td>MA4</td>
<td>O</td>
</tr>
<tr>
<td>U16</td>
<td>MA5</td>
<td>O</td>
</tr>
<tr>
<td>Y17</td>
<td>MA6</td>
<td>O</td>
</tr>
<tr>
<td>W17</td>
<td>MA7</td>
<td>O</td>
</tr>
<tr>
<td>V17</td>
<td>MA8</td>
<td>O</td>
</tr>
<tr>
<td>Y18</td>
<td>MA9</td>
<td>O</td>
</tr>
<tr>
<td>W18</td>
<td>MA10</td>
<td>O</td>
</tr>
<tr>
<td>Y19</td>
<td>MA11</td>
<td>O</td>
</tr>
<tr>
<td>T13</td>
<td>MA0A</td>
<td>O</td>
</tr>
<tr>
<td>T14</td>
<td>MA01</td>
<td>O</td>
</tr>
<tr>
<td>U14</td>
<td>MAB0</td>
<td>O</td>
</tr>
<tr>
<td>U15</td>
<td>MAB1</td>
<td>O</td>
</tr>
<tr>
<td>P19</td>
<td>MD0</td>
<td>I/O</td>
</tr>
<tr>
<td>N18</td>
<td>MD1</td>
<td>I/O</td>
</tr>
<tr>
<td>N20</td>
<td>MD2</td>
<td>I/O</td>
</tr>
<tr>
<td>M17</td>
<td>MD3</td>
<td>I/O</td>
</tr>
<tr>
<td>M19</td>
<td>MD4</td>
<td>I/O</td>
</tr>
<tr>
<td>L16</td>
<td>MD5</td>
<td>I/O</td>
</tr>
<tr>
<td>L18</td>
<td>MD6</td>
<td>I/O</td>
</tr>
<tr>
<td>L20</td>
<td>MD7</td>
<td>I/O</td>
</tr>
<tr>
<td>K17</td>
<td>MD8</td>
<td>I/O</td>
</tr>
<tr>
<td>K19</td>
<td>MD9</td>
<td>I/O</td>
</tr>
<tr>
<td>J16</td>
<td>MD10</td>
<td>I/O</td>
</tr>
<tr>
<td>J18</td>
<td>MD11</td>
<td>I/O</td>
</tr>
<tr>
<td>J20</td>
<td>MD12</td>
<td>I/O</td>
</tr>
<tr>
<td>H17</td>
<td>MD13</td>
<td>I/O</td>
</tr>
<tr>
<td>H19</td>
<td>MD14</td>
<td>I/O</td>
</tr>
<tr>
<td>G16</td>
<td>MD15</td>
<td>I/O</td>
</tr>
<tr>
<td>G18</td>
<td>MD16</td>
<td>I/O</td>
</tr>
<tr>
<td>G20</td>
<td>MD17</td>
<td>I/O</td>
</tr>
<tr>
<td>F17</td>
<td>MD18</td>
<td>I/O</td>
</tr>
<tr>
<td>F19</td>
<td>MD19</td>
<td>I/O</td>
</tr>
<tr>
<td>E16</td>
<td>MD20</td>
<td>I/O</td>
</tr>
<tr>
<td>E18</td>
<td>MD21</td>
<td>I/O</td>
</tr>
<tr>
<td>E20</td>
<td>MD22</td>
<td>I/O</td>
</tr>
<tr>
<td>D17</td>
<td>MD23</td>
<td>I/O</td>
</tr>
<tr>
<td>D19</td>
<td>MD24</td>
<td>I/O</td>
</tr>
<tr>
<td>C17</td>
<td>MD25</td>
<td>I/O</td>
</tr>
<tr>
<td>C19</td>
<td>MD26</td>
<td>I/O</td>
</tr>
<tr>
<td>B18</td>
<td>MD27</td>
<td>I/O</td>
</tr>
<tr>
<td>B20</td>
<td>MD28</td>
<td>I/O</td>
</tr>
<tr>
<td>A19</td>
<td>MD29</td>
<td>I/O</td>
</tr>
<tr>
<td>C16</td>
<td>MD30</td>
<td>I/O</td>
</tr>
<tr>
<td>E15</td>
<td>MD31</td>
<td>I/O</td>
</tr>
<tr>
<td>P18</td>
<td>MD32</td>
<td>I/O</td>
</tr>
<tr>
<td>P20</td>
<td>MD33</td>
<td>I/O</td>
</tr>
<tr>
<td>N19</td>
<td>MD34</td>
<td>I/O</td>
</tr>
<tr>
<td>M16</td>
<td>MD35</td>
<td>I/O</td>
</tr>
<tr>
<td>M18</td>
<td>MD36</td>
<td>I/O</td>
</tr>
<tr>
<td>M20</td>
<td>MD37</td>
<td>I/O</td>
</tr>
<tr>
<td>L17</td>
<td>MD38</td>
<td>I/O</td>
</tr>
<tr>
<td>L19</td>
<td>MD39</td>
<td>I/O</td>
</tr>
<tr>
<td>K16</td>
<td>MD40</td>
<td>I/O</td>
</tr>
<tr>
<td>K18</td>
<td>MD41</td>
<td>I/O</td>
</tr>
<tr>
<td>K20</td>
<td>MD42</td>
<td>I/O</td>
</tr>
<tr>
<td>J17</td>
<td>MD43</td>
<td>I/O</td>
</tr>
<tr>
<td>J19</td>
<td>MD44</td>
<td>I/O</td>
</tr>
<tr>
<td>H16</td>
<td>MD45</td>
<td>I/O</td>
</tr>
<tr>
<td>H18</td>
<td>MD46</td>
<td>I/O</td>
</tr>
<tr>
<td>H20</td>
<td>MD47</td>
<td>I/O</td>
</tr>
<tr>
<td>G17</td>
<td>MD48</td>
<td>I/O</td>
</tr>
<tr>
<td>G19</td>
<td>MD49</td>
<td>I/O</td>
</tr>
<tr>
<td>F16</td>
<td>MD50</td>
<td>I/O</td>
</tr>
<tr>
<td>F18</td>
<td>MD51</td>
<td>I/O</td>
</tr>
<tr>
<td>F20</td>
<td>MD52</td>
<td>I/O</td>
</tr>
<tr>
<td>E17</td>
<td>MD53</td>
<td>I/O</td>
</tr>
<tr>
<td>E19</td>
<td>MD54</td>
<td>I/O</td>
</tr>
<tr>
<td>D16</td>
<td>MD55</td>
<td>I/O</td>
</tr>
<tr>
<td>D18</td>
<td>MD56</td>
<td>I/O</td>
</tr>
<tr>
<td>D20</td>
<td>MD57</td>
<td>I/O</td>
</tr>
<tr>
<td>C18</td>
<td>MD58</td>
<td>I/O</td>
</tr>
<tr>
<td>C20</td>
<td>MD59</td>
<td>I/O</td>
</tr>
<tr>
<td>B19</td>
<td>MD60</td>
<td>I/O</td>
</tr>
<tr>
<td>A18</td>
<td>MD61</td>
<td>I/O</td>
</tr>
<tr>
<td>A20</td>
<td>MD62</td>
<td>I/O</td>
</tr>
<tr>
<td>B17</td>
<td>MD63</td>
<td>I/O</td>
</tr>
<tr>
<td>H5</td>
<td>MIOJ</td>
<td>I</td>
</tr>
<tr>
<td>A17</td>
<td>MPD0</td>
<td>I/O</td>
</tr>
<tr>
<td>B16</td>
<td>MPD1</td>
<td>I/O</td>
</tr>
</tbody>
</table>
### Alphabetical Pin List (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A16</td>
<td>MPD2</td>
<td>I/O</td>
</tr>
<tr>
<td>D15</td>
<td>MPD3</td>
<td>I/O</td>
</tr>
<tr>
<td>C15</td>
<td>MPD4</td>
<td>I/O</td>
</tr>
<tr>
<td>B15</td>
<td>MPD5</td>
<td>I/O</td>
</tr>
<tr>
<td>E14</td>
<td>MPD6</td>
<td>I/O</td>
</tr>
<tr>
<td>D14</td>
<td>MPD7</td>
<td>I/O</td>
</tr>
<tr>
<td>U17</td>
<td>MWEJ</td>
<td>I/O</td>
</tr>
<tr>
<td>T17</td>
<td>MWEJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>G5</td>
<td>NAJ</td>
<td>O</td>
</tr>
<tr>
<td>A7</td>
<td>PAR</td>
<td>I/O</td>
</tr>
<tr>
<td>E6</td>
<td>PCIRMQJ</td>
<td>O</td>
</tr>
<tr>
<td>E11</td>
<td>PCLKIN</td>
<td>I</td>
</tr>
<tr>
<td>A2</td>
<td>PHLDAJ</td>
<td>O</td>
</tr>
<tr>
<td>B2</td>
<td>PHLDJ</td>
<td>I</td>
</tr>
<tr>
<td>T19</td>
<td>RASJ0</td>
<td>O</td>
</tr>
<tr>
<td>T18</td>
<td>RASJ1</td>
<td>O</td>
</tr>
<tr>
<td>U20</td>
<td>RASJ2</td>
<td>O</td>
</tr>
<tr>
<td>U19</td>
<td>RASJ3</td>
<td>O</td>
</tr>
<tr>
<td>U18</td>
<td>RASJ4</td>
<td>O</td>
</tr>
<tr>
<td>V20</td>
<td>RASJ5</td>
<td>O</td>
</tr>
<tr>
<td>R16</td>
<td>RASJ6</td>
<td>O</td>
</tr>
<tr>
<td>R17</td>
<td>RASJ7</td>
<td>O</td>
</tr>
<tr>
<td>D13</td>
<td>REQJ0</td>
<td>I</td>
</tr>
<tr>
<td>C13</td>
<td>REQJ1</td>
<td>I</td>
</tr>
<tr>
<td>B13</td>
<td>REQJ2</td>
<td>I</td>
</tr>
<tr>
<td>A13</td>
<td>REQJ3</td>
<td>I</td>
</tr>
<tr>
<td>N16</td>
<td>REQJ4</td>
<td>I/O</td>
</tr>
<tr>
<td>E5</td>
<td>RSTJ</td>
<td>I</td>
</tr>
<tr>
<td>T15</td>
<td>SCASJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>E8</td>
<td>SERRJ</td>
<td>I/O</td>
</tr>
<tr>
<td>F3</td>
<td>SMIACTJ</td>
<td>I</td>
</tr>
<tr>
<td>T16</td>
<td>SRASJ1</td>
<td>I/O</td>
</tr>
<tr>
<td>C8</td>
<td>STOPJ</td>
<td>I/O</td>
</tr>
<tr>
<td>P17</td>
<td>SUSPENDJ</td>
<td>I</td>
</tr>
<tr>
<td>U12</td>
<td>TIO0</td>
<td>I/O</td>
</tr>
<tr>
<td>U13</td>
<td>TIO1</td>
<td>I/O</td>
</tr>
<tr>
<td>V14</td>
<td>TIO2</td>
<td>I/O</td>
</tr>
<tr>
<td>Y14</td>
<td>TIO3</td>
<td>I/O</td>
</tr>
<tr>
<td>W14</td>
<td>TIO4</td>
<td>I/O</td>
</tr>
<tr>
<td>Y15</td>
<td>TIO5</td>
<td>I/O</td>
</tr>
<tr>
<td>W15</td>
<td>TIO6</td>
<td>I/O</td>
</tr>
<tr>
<td>Y16</td>
<td>TIO7</td>
<td>I/O</td>
</tr>
<tr>
<td>Y20</td>
<td>TIO8</td>
<td>I/O</td>
</tr>
<tr>
<td>A8</td>
<td>TRDYJ</td>
<td>I/O</td>
</tr>
<tr>
<td>T12</td>
<td>TWEJ</td>
<td>O</td>
</tr>
<tr>
<td>F14</td>
<td>VCC_C</td>
<td>P</td>
</tr>
<tr>
<td>F15</td>
<td>VCC_C</td>
<td>P</td>
</tr>
<tr>
<td>F6</td>
<td>VCC_B</td>
<td>P</td>
</tr>
<tr>
<td>G15</td>
<td>VCC_C</td>
<td>P</td>
</tr>
<tr>
<td>G6</td>
<td>VCC_A</td>
<td>P</td>
</tr>
</tbody>
</table>
Section 3 : Function Description

3.1 System Architecture

In the following illustration, ALADDIN-IV gives a highly integrated system solution and a most up-to-date system architecture, which includes the Parity/ECC, PBSRAM, SDRAM, ACPI, Ultra-33 IDE Master, USB, PS2 Keyboard/Mouse, and highly concurrent multibus with smart deep FIFO between the buses, such as the HOST/DRAM/PCI/ISA/DEDICATED IDE/USB buses. Using Aladdin-IV, you can achieve a TTL free solution and provide the best system performance.

The M1531B provides a complete integrated solution for the system controller and data path components in a Pentium processor system. It provides a 64-bit CPU bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Memory Cache, PCI master to DRAM interface, and 5 PCI masters, CPU, and M1533/M1543 arbiter. The following figure shows the highly efficient data path in the M1531B. The M1531B bus interfaces are designed to interface with 2.5V, 3.3V and 5V buses. It directly connects to 3.3V or 2.5V CPU bus, 3.3V or 5V Tag, 3.3V or 5V DRAM bus, and 3.3V or 5V PCI bus.

The M1533 provides a highly integrated PCI-to-ISA bridge solution for the best Notebook system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, and Enhanced Green function.
The M1543 provides a highly integrated PCI-to-ISA bridge solution for the best Desktop system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, Green function, and the Super I/O function.
3.2 CPU Interface

The M1531B supports all Pentium-class CPUs including Intel P54C/P55C, Cyrix M1, AMD K5, and Ti Dakota. Furthermore, M1531B supports a high performance CPU interface to Cyrix M2, and AMD K6 with higher CPU bus frequency (up to 83.3 MHz) to achieve the Pentium Pro-class system performance. M1531B also supports Cyrix Linear Wrap mode for M1 and M2 to gain the best system performance. M1531B can also interface to 2.5V CPU I/O interface for Notebook use. In the higher CPU bus frequency interface, M1531B will do the so-called pseudo-synchronous design instead of the asynchronous design. When 75/83.3 MHz CPU bus is used, the PCI bus will be running at 30/33 MHz (divide CPU bus by 2.5). The pseudo-synchronous clock design is a better solution than the pure asynchronous clock design, it eliminates the performance degradation to synchronize two asynchronous buses and helps the chip reliability to resolve the chip testing issue.

3.3 Clock Design Philosophy

The system provides 3 clocks for M1531B, HCLKIN has the same frequency with the CPUCLK, Cache clock, and SDRAM clock. PCLKIN has the same frequency with the PCI bus clock, and 32K is a 32K frequency clock from M1533/M1543 CLK32KO or from the system board clock source. System designer should minimize the clock skew between CPUCLK, Cache clock, SDRAM clock, and HCLKIN, and also the skew between PCLKIN and PCI bus clock. Regarding the skew between M1531B’s HCLKIN and PCLKIN, PCLKIN should lag HCLKIN for 1 ~ 4 ns. The internal clock design philosophy uses the HCLKIN running the state machine of CPU interface, L2 controller, and DRAM controller, and uses the PCLKIN running the PCI state machine, and automatically takes good care of the internal signal interface between different clock frequency state machines. Also M1531B will support the internal smart clock control, it will shut off the internal clock when the CPU or PCI bus is idle to save the power consumption. 32K clock is used for the DRAM Suspend refresh clock. It is a clock input and not necessarily relative to HCLKIN or PCLKIN.
3.4 Cache Memory Timing/Configuration
The M1531B integrates a high performance L2 write back/dynamic-writeback direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag 8Kx2 bits built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for Memory Cache or Pipelined Burst SRAM with cache size ranging from 256KB, 512KB to 1MB. The cacheable region can be up to 512MB under 256KB cache memory configuration, by using 11-bit tag option. Or, by using an 8Kx8 tag RAM, the cacheable region of the system is 64MB. The controller can perform a dynamic-writeback cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution. Also M1531B can support the CPU single read cycle L2 allocation feature, M1531B will do the L2 line fill even when the CPU issues only a single read cycle to improve the L2 hit rate for some special application. The following table shows the best performance for the L2 Read/Write access.

The timing of cache memory system is shown in following table:

<table>
<thead>
<tr>
<th>PBSRAM and Memory cache</th>
<th>READ</th>
<th>WRITE</th>
<th>B2B READ</th>
<th>B2B WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3-1-1-1</td>
<td></td>
<td>3-1-1-1-1-1-1</td>
<td>3-1-1-1-1-1-1</td>
</tr>
</tbody>
</table>

The following L2 Cache Table shows the different configurations supported by M1531B.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>DATA SRAM</th>
<th>TAG SRAM</th>
<th>Internal MESI</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache Size</td>
<td>Size</td>
<td>Bank</td>
<td>Address lines</td>
<td>Address lines</td>
</tr>
<tr>
<td>256K (32K32)*2</td>
<td>1 A3-A17</td>
<td>A5-A17</td>
<td>A18-A25</td>
<td>8K8</td>
</tr>
<tr>
<td>512K (64K16)*4</td>
<td>1 A3-A18</td>
<td>A5-A18</td>
<td>A19-A25</td>
<td>16K8</td>
</tr>
<tr>
<td>512K (32K32)*4</td>
<td>2 A3-A18</td>
<td>A5-A18</td>
<td>A19-A25</td>
<td>16K8</td>
</tr>
<tr>
<td>1M (64K32)*4</td>
<td>2 A3-A19</td>
<td>A5-A19</td>
<td>A20-A25</td>
<td>32K8</td>
</tr>
<tr>
<td>256K (32K32)*2</td>
<td>1 A3-A17</td>
<td>A5-A17</td>
<td>A18-A26</td>
<td>8K9</td>
</tr>
<tr>
<td>512K (64K16)*4</td>
<td>1 A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
<td>16K9</td>
</tr>
<tr>
<td>512K (32K32)*4</td>
<td>2 A3-A18</td>
<td>A5-A18</td>
<td>A19-A26</td>
<td>16K9</td>
</tr>
<tr>
<td>1M (64K32)*4</td>
<td>2 A3-A19</td>
<td>A5-A19</td>
<td>A20-A26</td>
<td>32K9</td>
</tr>
<tr>
<td>256K (32K32)*2</td>
<td>1 A3-A17</td>
<td>A5-A17</td>
<td>A18-A27</td>
<td>8K10</td>
</tr>
<tr>
<td>512K (64K16)*4</td>
<td>1 A3-A18</td>
<td>A5-A18</td>
<td>A19-A27</td>
<td>16K10</td>
</tr>
<tr>
<td>512K (32K32)*4</td>
<td>2 A3-A18</td>
<td>A5-A18</td>
<td>A19-A27</td>
<td>16K10</td>
</tr>
<tr>
<td>1M (64K32)*4</td>
<td>2 A3-A19</td>
<td>A5-A19</td>
<td>A20-A27</td>
<td>32K10</td>
</tr>
<tr>
<td>256K (32K32)*2</td>
<td>1 A3-A17</td>
<td>A5-A17</td>
<td>A18-A28</td>
<td>8K11</td>
</tr>
<tr>
<td>512K (64K16)*4</td>
<td>1 A3-A18</td>
<td>A5-A18</td>
<td>A19-A28</td>
<td>16K11</td>
</tr>
<tr>
<td>1M (64K32)*4</td>
<td>2 A3-A19</td>
<td>A5-A19</td>
<td>A20-A28</td>
<td>32K11</td>
</tr>
</tbody>
</table>
The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.

<table>
<thead>
<tr>
<th>CPU Bus Frequency (MHz)</th>
<th>PBSRAM Clock-to-Output Access Time (ns)</th>
<th>Tag RAM Access Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>13.5</td>
<td>20</td>
</tr>
<tr>
<td>60</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>66</td>
<td>8.5</td>
<td>15</td>
</tr>
<tr>
<td>75</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>83.3</td>
<td>6</td>
<td>10</td>
</tr>
</tbody>
</table>

In the following figures, two recommended cache subsystems are shown as follows:

**Pipelined Burst SRAM L2 with 512K & 8-bit Tag RAM (64M cacheable region)**
3.5 SYSTEM MEMORY TIMING/CONFIGURATION

The DRAM controller of the M1531B supports a variety of DRAM types and improves the first data transaction performance by using a speculative cycle to shorten the latency. Basically, it supports a 32/64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs, and also supports the 64-bit memory bus for 6 banks of single-sided DIMMs or 3 banks of double sided DIMMs. For the best system upgrade ability, ALADDIN IV supports six single-sided 32-bit populated DRAM banks or three double-sided 32-bit populated DRAM banks. The system memory can be easily configured to 12MB by using the most popular 16-Mbit memory types. In this configuration, one bank is 64-bit 8MB, and the other bank is 32-bit 4MB. In the upgrade path, all banks can be extended to 64-bit memory. M1531B also supports the most flexible 32-bit memory population, it supports low DWORD and high DWORD population.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size ranging from 2MB to 1GB. It also supports a programmable driving capability of MA/RAS/CAS/WE to optimize the access timing and the system cost in certain system memory configurations. MA[0-1] are duplicated to gain the burst timing design of the system. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip. M1531B supports a high performance SDRAM controller to push the new DRAM performance to the high edge. M1531B also enhances the DRAM page miss access timing for multithreading and multitasking application. For the best DRAM performance, M1531B has integrated a 16-QWORD deep merging DRAM write buffer. The deep buffer can post the CPU write data and also the PCI master write data and do byte merge to relief the DRAM bus access.

As to the System Management RAM (SMRAM), the M1531B allows several optional noncacheable spaces to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.
3.5.1 Memory Type supported

Table 3-1. Memory Structure Supported for FPM/EDO

<table>
<thead>
<tr>
<th>Memory Structure</th>
<th>Address mode</th>
<th>Address size</th>
<th>Memory Structure</th>
<th>Address mode</th>
<th>Address size</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mbits</td>
<td></td>
<td></td>
<td>2Mx8</td>
<td>Asymmetric</td>
<td>11x10</td>
</tr>
<tr>
<td>512Kx8</td>
<td>Asymmetric</td>
<td>10x9</td>
<td>4Mx4</td>
<td>Symmetric</td>
<td>11x11</td>
</tr>
<tr>
<td>1Mx4</td>
<td>Symmetric</td>
<td>10x10</td>
<td>4Mx4</td>
<td>Asymmetric</td>
<td>12x10</td>
</tr>
<tr>
<td>16Mbits</td>
<td></td>
<td></td>
<td>64Mbits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Mx16</td>
<td>Asymmetric</td>
<td>12x8</td>
<td>4Mx16</td>
<td>Symmetric</td>
<td>11x11</td>
</tr>
<tr>
<td>1Mx16</td>
<td>Symmetric</td>
<td>10x10</td>
<td>8Mx8</td>
<td>Asymmetric</td>
<td>12x11</td>
</tr>
<tr>
<td>2Mx8</td>
<td>Asymmetric</td>
<td>12x9</td>
<td>16Mx4</td>
<td>Symmetric</td>
<td>12x12</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory Structure</th>
<th>Address size</th>
<th>Bank size</th>
</tr>
</thead>
<tbody>
<tr>
<td>16Mbits SDRAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2x2Mx4</td>
<td>11x10</td>
<td>32MB</td>
</tr>
<tr>
<td>2x1Mx8</td>
<td>11x9</td>
<td>16MB</td>
</tr>
<tr>
<td>2x512Kx16</td>
<td>11x8</td>
<td>8MB</td>
</tr>
<tr>
<td>64Mbits SDRAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2x8Mx4</td>
<td>13x10</td>
<td>128MB</td>
</tr>
<tr>
<td>2x4Mx8</td>
<td>13x9</td>
<td>64MB</td>
</tr>
<tr>
<td>2x2Mx16</td>
<td>13x8</td>
<td>32MB</td>
</tr>
<tr>
<td>2x2Mx16</td>
<td>11x10</td>
<td>32MB</td>
</tr>
<tr>
<td>2x1Mx32</td>
<td>11x9</td>
<td>16MB</td>
</tr>
<tr>
<td>2x512Kx64</td>
<td>11x8</td>
<td>8MB</td>
</tr>
<tr>
<td>2x1Mx32</td>
<td>12x8</td>
<td>16MB</td>
</tr>
<tr>
<td>4x4Mx4</td>
<td>12x10</td>
<td>128MB</td>
</tr>
<tr>
<td>4x2Mx8</td>
<td>12x9</td>
<td>64MB</td>
</tr>
<tr>
<td>4x1Mx16</td>
<td>12x8</td>
<td>32MB</td>
</tr>
<tr>
<td>4x2Mx8</td>
<td>11x10</td>
<td>64MB</td>
</tr>
<tr>
<td>4x1Mx16</td>
<td>11x9</td>
<td>32MB</td>
</tr>
<tr>
<td>4x512Kx32</td>
<td>11x8</td>
<td>16MB</td>
</tr>
</tbody>
</table>

3.5.2 MA Mapping Table Supported

In the following table, ALADDIN-IV supports a versatile memory MA mapping table to accommodate many different approaches of DRAM populated banks. Furthermore, it supports the 32-bit memory bus on each possible available bank.

Table 3-2. Several DRAM Address translation supported for some specific purpose

<table>
<thead>
<tr>
<th>Normal FPM/EDO DRAM Address Translation Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA[11:0]</td>
</tr>
<tr>
<td>Row</td>
</tr>
<tr>
<td>Column</td>
</tr>
</tbody>
</table>

Row MA[11]: If 64Mbits DRAM is not populated, then A24 is driven; if 64Mbits DRAM is populated, then A25 is driven.
### 1M x 16, 2M x 8 FPM/EDO DRAM Address Translation Table
Specific DRAM Address Translation Table for Asymmetric 1M x 16

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A22</td>
<td>A21</td>
<td>A11</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
<tr>
<td>Column</td>
<td>A23</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Address Size = 12 x 8, 12 x 9

### 32-bit bank FPM/EDO DRAM Address Translation Table

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A23/A24</td>
<td>A22</td>
<td>A11</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
</tbody>
</table>

Row MA[11] : if 64Mbits DRAM is not populated, then A23 is driven; if 64Mbits DRAM is populated, then A24 is driven

### 32-bit Bank 1M x 16, 2M x 8 FPM/EDO DRAM Address Translation Table

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A10</td>
<td>A21</td>
<td>A11</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
<tr>
<td>Column</td>
<td>A22</td>
<td>A4</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>(A2)</td>
<td>A3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Address Size = 12 x 8, 12 x 9

### 64MB SDRAM MA mapping table (2-bank: 13*10,13*9, 13*8, 12*8) (4-bank: 12*10,12*9,12*8)

| MA[11:0] | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Row      | A23| A24| A11| A22| A21| A20| A19| A18| A17| A16| A15| A14| A13| A12|

### 64MB SDRAM MA mapping table (4-bank: 11*10,11*9,11*8)

| MA[11:0] | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Row      | X   | A23| A11| A22| A21| A20| A19| A18| A17| A16| A15| A14| A13| A12|

### 16MB SDRAM MA mapping table (2-bank: 11*10,11*9, 11*8) 64MB MA mapping table (2-bank: 12*10,12*9,12*8)

| MA[11:0] | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Row      | x   | x  | A11| A22| A21| A20| A19| A18| A17| A16| A15| A14| A13| A12|
| Column   | x   | x  | A11| L  | A24| A23| A10| A9 | A8 | A7 | A6 | A5 | A4 | A3 |   |
3.5.3 Outstanding DRAM timing

The following table shows the timing of EDO/FPM DRAMs:

### Table 3-3. Lead time of first data transaction, check time at T2

<table>
<thead>
<tr>
<th>r.lead</th>
<th>w.lead</th>
<th>ras.prch</th>
<th>t.lead(t2)</th>
<th>sle. lead</th>
<th>ras-cas</th>
<th>read..hit</th>
<th>wr..hit</th>
<th>r.row.mis</th>
<th>r.pg.mis</th>
<th>w.rtr.row.m</th>
<th>w.rtr.pg.ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>5</td>
<td>3</td>
<td>-1</td>
<td>-1</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>7</td>
<td>10</td>
<td>8</td>
<td>11</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>3</td>
<td>-1</td>
<td>-1</td>
<td>2</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>9</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
<td>-1</td>
<td>-1</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>7</td>
<td>11</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
<td>-1</td>
<td>-1</td>
<td>2</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>10</td>
<td>7</td>
<td>11</td>
</tr>
</tbody>
</table>

**Note:**
- r.lead means “read lead off cycle”
- w.lead means “write lead off cycle”
- ras.prch means “RAS precharge time”, and is controlled by Index -44h bit2.
- t.lead(t2) means “Hit/Miss check point”, and is controlled by Index-40h bit0.
- sle.lead means “Read Speculative Leadoff”, and is controlled by Index-45h bit5.
- ras-cas means “RAS to CAS delay”, and is controlled by Index-44h bit3.
- read hit means “read hit lead off cycle”
- write hit means “write hit lead off cycle”
- r.row.mis means “read row miss lead off cycle”
- w.rtr.row.m means “write buffer retired write row miss cycle”
- w.rtr.pg.ms means “write buffer retired write page miss cycle”

### Table 3-4. CPU to DRAM read performance Summary for BEDO/EDO/FPM DRAMs

<table>
<thead>
<tr>
<th>DRAM speed (Burst rate)</th>
<th>DRAM type</th>
<th>Performance (in Host CLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DRAM speed</td>
<td>Read (Burst rate)</td>
</tr>
<tr>
<td>50 ns</td>
<td>EDO</td>
<td>x-222</td>
</tr>
<tr>
<td></td>
<td>FPM</td>
<td>x-333</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>x-222</td>
</tr>
<tr>
<td></td>
<td>FPM</td>
<td>x-333</td>
</tr>
<tr>
<td>70 ns</td>
<td>EDO</td>
<td>x-222</td>
</tr>
<tr>
<td></td>
<td>FPM</td>
<td>x-333</td>
</tr>
</tbody>
</table>

### Page hit
- 50/60 MHz
- 66 MHz
- 75/83 MHz

### Row Miss
- 60 ns
- EDO/FPM
- 60 ns
- 6

### Page Miss
- 60 ns
- EDO/FPM

### Back-to-back Burst Reads with Page hit
- 50/60 MHz
- 60 ns
- EDO
- 6-222-2222
- 5-222-2222
- 5-222-2222
- 6-333-3333
- 60 ns
- FPM
- 4-333-3333
- 5-333-3333
- 6-444-4444
### Table 3-5. CPU to DRAM Write Performance Summary

<table>
<thead>
<tr>
<th>DRAM speed</th>
<th>DRAM type</th>
<th>Performance (in Host CLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Posted Single Write with Write Buffer Empty</td>
<td>50 MHz</td>
<td>60/66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>3.3.3</td>
</tr>
<tr>
<td>Posted Burst Write with Write Buffer Empty</td>
<td>50 MHz</td>
<td>60/66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO/FPM</td>
<td>3-111</td>
</tr>
<tr>
<td>Single Retire Hit</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>2</td>
</tr>
<tr>
<td>60 ns</td>
<td>FPM</td>
<td>2</td>
</tr>
<tr>
<td>Single Retire Row Miss with RAS-CAS = 2T</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>4</td>
</tr>
<tr>
<td>60 ns</td>
<td>FPM</td>
<td>4</td>
</tr>
<tr>
<td>Single Retire Page Miss with RAS-CAS = 2T</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>7</td>
</tr>
<tr>
<td>60 ns</td>
<td>FPM</td>
<td>7</td>
</tr>
<tr>
<td>Retire Burst</td>
<td>50/60 MHz</td>
<td>66 MHz</td>
</tr>
<tr>
<td>60 ns</td>
<td>EDO</td>
<td>x-222</td>
</tr>
<tr>
<td>60 ns</td>
<td>FPM</td>
<td>x-222</td>
</tr>
</tbody>
</table>

### Table 3-6. SDRAM Performance Summary

<table>
<thead>
<tr>
<th>Cycle Type</th>
<th>83/75/66 MHz</th>
<th>60 MHz</th>
<th>50 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAS Latency</td>
<td>CL=3</td>
<td>CL=2</td>
<td>CL=3</td>
</tr>
<tr>
<td>Burst Read Page Hit</td>
<td>7-1-1-1</td>
<td>6-1-1-1</td>
<td>6-1-1-1</td>
</tr>
<tr>
<td>Read Bank Miss</td>
<td>10-1-1-1</td>
<td>8-1-1-1</td>
<td>10-1-1-1</td>
</tr>
<tr>
<td>Read Page Miss</td>
<td>13-1-1-1</td>
<td>10-1-1-1</td>
<td>13-1-1-1</td>
</tr>
<tr>
<td>Back-to-back Burst Read Page Hit</td>
<td>7-1-1-1-2-1-1-1</td>
<td>6-1-1-1-2-1-1-1</td>
<td>6-1-1-1-2-1-1-1</td>
</tr>
<tr>
<td>Write Page Hit</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Write Row Miss</td>
<td>6</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>Write Page Miss</td>
<td>9</td>
<td>7</td>
<td>9</td>
</tr>
<tr>
<td>Posted Write</td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
<td>3-1-1-1</td>
</tr>
<tr>
<td>Write Retire rate from Posted Write Buffer</td>
<td>-1-1-1</td>
<td>-1-1-1</td>
<td>-1-1-1</td>
</tr>
</tbody>
</table>
3.5.4 EDO/FPM/(BEDO) DRAM Configuration

ALADDIN-IV supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. The following diagram shows some possible applications.

2 Double-Sided DRAM Bank (EDO/FPM)

3 Double-Sided DRAM Bank (EDO/FPM) - with buffer
4 Double-Sided DRAM Bank Driving Organization (EDO/FPM)

2 Double-Sided DRAM Bank (EDO/FPM) +
2 Double-Sided SDRAM Bank

3.5.5 SDRAM Support

Aladdin IV supports the most popular synchronous DRAM (SDRAM) at sizes of 1M*16, 2M*8, and 4M*4 with extra performance and flexibility. Interleaved and linear wrap type for both CAS latency 2 and 3 with burst length 4 are supported. Users are permitted to use pure SDRAM up to 6 banks single sided or 3 banks of double sided, or mix with FPM/EDO DRAM on a row-by-row basis without any constraint. Furthermore, M1531B supports SDRAM Speculative Read and Enhanced Page mode which not only minimizes the effect of CAS latency (CL) and RAS Precharge time (Trp) but also largely enhances the overall performance of the system. JEDEC standard for SDRAM including 2n rule are supported too. Note that M1531B does not support the 32-bit SDRAM population.

ALADDIN-IV utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are:

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)
- Device Deselect (DESL)
The following Table shows the command truth table M1531B supports.

**Table 3-7. Command Truth Table**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode Register Set</td>
<td>MRS</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>V</td>
<td>*2</td>
</tr>
<tr>
<td>Self-Refresh</td>
<td>SEFR</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>Precharge All Banks</td>
<td>PALL</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>K</td>
<td>H</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>Precharge Selected Bank</td>
<td>PRCH</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>Row Active</td>
<td>RACT</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>Write</td>
<td>WRITE</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>Read</td>
<td>READ</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>No Operation</td>
<td>NOP</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>V</td>
<td>L</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>Device Deselect</td>
<td>DESL</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
<tr>
<td>CAS-before-RAS</td>
<td>CBR</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>K</td>
<td>K</td>
<td>K</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**
1. V = Valid, L = Logic Low, H = Logic High. K = Keep the value in previous cycle.
2. Please refer to Table 3-8.
3. A11 = 0 to select bank 0. A11 = 1 to select bank 1.
5. A[9:0] is used as the column address for 4M*4 SDRAM, A[8:0] is used as the column address for 2M*8 SDRAM, A[7:0] is used as the column address for 1M*16 SDRAM.

In terms of Wrap Type of SDRAM, ALADDIN-IV supports both Interleave mode and Linear (Sequential) mode. The following table shows the Mode Register Set Table supported by M1531B.

**Table 3-8. Mode Register Set**

<table>
<thead>
<tr>
<th>A11</th>
<th>A10</th>
<th>A9</th>
<th>A8</th>
<th>A7</th>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CAS Latency</td>
<td>Burst Type</td>
<td>Burst Length</td>
<td>Mode Register</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>CAS Latency</th>
<th>Index-5Ch bit4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A3</th>
<th>Burst Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Sequential</td>
<td>for M1/M2 Linear Wrap Mode</td>
</tr>
<tr>
<td>1</td>
<td>Interleave</td>
<td>for P54C/P55C/K5/K6 Interleave mode</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>Burst Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>Others</td>
<td>Not Support</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ALADDIN-IV supports two sets of SDRAM control signals. Following figures show the topological configuration when supporting SDRAM. The first figure below illustrates 4-bank single-sided or 2-bank double sided support of SDRAM. The following figure shows 6-bank support of SDRAM. Please refer to Table 3-5 for the source of SRASJ[1:0], SCASJ[1:0] and MWEJ[1:0].
3.5.6 Signal Assignment of DRAM interface

As several DRAM architectures are supported, the signal of each configuration have to be multiplexed to optimize the pinout. Shown here is the signal assignment for each configuration and is controlled by Index-41h bit6, bit3, and bit0. In the following table, MWEJ[1] will become MKREFQJ when Memory Cache has been used (Index-41h bit6 = 0).

Table 3-9. Signal Assignment of Versatile DRAM Architecture

<table>
<thead>
<tr>
<th></th>
<th>without buffer</th>
<th>with buffer</th>
<th>4 SDRAM bank</th>
<th>6 SDRAM bank</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS0</td>
<td>RAS0</td>
<td>RAS0</td>
<td>RAS0</td>
<td>RAS0</td>
</tr>
<tr>
<td>RAS1</td>
<td>RAS1</td>
<td>RAS1</td>
<td>RAS1</td>
<td>RAS1</td>
</tr>
<tr>
<td>RAS2</td>
<td>RAS2</td>
<td>RAS2</td>
<td>RAS2</td>
<td>RAS2</td>
</tr>
<tr>
<td>RAS3</td>
<td>RAS3</td>
<td>RAS3</td>
<td>RAS3</td>
<td>RAS3</td>
</tr>
<tr>
<td>RAS6</td>
<td>RAS6</td>
<td>RAS6</td>
<td>RAS6</td>
<td>RAS6</td>
</tr>
<tr>
<td>RAS7</td>
<td>RAS7</td>
<td>RAS7</td>
<td>RAS7</td>
<td>RAS7</td>
</tr>
<tr>
<td>MWEJ[0]</td>
<td>MWEJ[0]</td>
<td>MWEJ[0]</td>
<td>MWEJ[0]</td>
<td>MWEJ[0]</td>
</tr>
</tbody>
</table>

3.5.7 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-IV is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING. If only 4 banks of single sided DRAM SIMMs or 2 banks of double sided DRAM SIMMs or 6 banks of single sided DRAM DIMMs or 3 banks of double sided DRAM DIMMs are designed in motherboard, M1531B is designed to be TTL free for the DRAM control signals buffer.

3.6 CPU-to-PCI Posted Write Buffer

The M1531B integrates a 6-DWORD CPU-to-PCI posted write buffer to enhance the CPU-to-PCI performance. With this buffer, the M1531B can minimize the latency of CPU-to-PCI write cycles and maximize the concurrency of CPU bus and PCI bus when CPU writes data to PCI bus. The PCI burst write cycles and fast back-to-back cycles for CPU-to-PCI access are also supported by this buffer.

In addition, the M1531B CPU-to-PCI posted write buffer supports data merge, it can improve the CPU-to-PCI non-32 bits access performance.

3.7 PCI MASTER Latency and Throughput Analysis

The M1531B includes a smart PCI-to-DRAM interface, including a smart deep PCI-to-DRAM buffer and the enhanced PCI arbiter. All these components are designed to optimize the system performance and maximize the PCI bus bandwidth.
3.7.1 Smart Deep Post Write & Prefetch Buffer

The smart deep PCI-to-DRAM buffer of M1531B plays the key role to boost PCI master read/write performance. It consists of 38 DWORDs posted write buffer and 22 DWORDs prefetch buffer.

The 38 DWORDs PCI-to-DRAM posted write buffers enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 writeback merge and smart buffer management, the M1531B can sustain the ultimate 133-Mbytes/sec bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and writeback cycle, the DRAM types and L2 types.

On the other hand, to optimize the PCI master read performance when accessing DRAM, the M1531B includes 22 DWORDs PCI-to-DRAM read prefetch buffers. With the implementation of L1/L2 writeback and smart buffer management, the M1531B can sustain the ultimate 133 Mbytes/sec bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, writeback cycle and L2 types.

Consider the performance and concurrency of multi-master systems, for example the MPEG/Multimedia applications, the PCI-to-DRAM read prefetch buffer of M1531B is configured as two independent units. Each unit prefetches and keeps data independently with the other one. With this configuration, the M1531B minimizes the PCI master read latency and reduces the overhead of snooping and prefetching.

3.7.2 PCI 2.1 Compliant

The M1531B is fully compliant to the PCI 2.1 Specification. The M1531B supports Passive Release and programmable latency control timers for the first and subsequent data transaction. With the flexible PCI latency control, it can achieve the best system performance.

3.7.3 Pipelined Snoop Ahead

The M1531B utilizes an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. While snooping L1 & L2, the M1531B also performs speculative read to DRAM such that the latency of master read cycle can be minimized. It combines with the deep smart read/write buffer to optimize PCI master performance.

3.7.4 PCI Arbiter

The M1531B integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism. The arbitration algorithm is also designed to minimize the snoop overhead. Besides the M1533/M1543 ISA bridge, the M1531B supports up to 5 PCI masters to make the system motherboard design more flexible and engaging.

To balance the bandwidth of ISA masters and PCI masters and utilize the most bandwidth of PCI bus, the M1531B also supports passive release of PCI 2.1 latency requirements, which makes PCI master access possible when ISA master is active. By this way, the Aladdin-IV can target the best system performance and the most concurrency between PCI bus and ISA bus.

3.7.5 ACPI Support

The M1531B provides the scheme to support ACPI relative functions. By means of PM2_BASE_ADDRESS register (Index-70h - Index-71h) and PM2_CONTROL register (Index-72h Bits[1:0]), software can easily enable/disable PCI arbiter as ACPI requirement. In addition, PCIMRQJ signal makes ISA Bridge aware of PCI master bus request to generate SMI/SCI.

3.8 Low Power Features

The ALADDIN-IV supports sophisticated power saving features, called Power On Suspend (Sleeping), Suspend to DRAM (Suspend), and Suspend to Disk. Under Power On Suspend state, the system will turn off the signal event of host and keep the DRAM refresh active through the M1531B’s DRAM interface that is triggered by a 32K clock source. After the Power On suspend event is triggered, by programming a bit of M1533/M1543’s internal register, the M1533/M1543 will initiate a handshake with the M1531B. During the handshake, the M1533/M1543 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH circuit to sustain the DRAM data. Theoretically, the only power request under the Power On suspend is the circuit of DRAM suspend refresh. M1531B core has two different power planes, one for the Suspend Refresh circuit, the other is for the other circuit except Suspend Refresh circuit. During Suspend to DRAM state, the system designer can shut off the power except the DRAM suspend refresh circuit to save more system power. Under the Suspend to Disk, only the M1533/M1543 resume circuit is powered and get the minimized system power consumption.
The M1531B and the M1533/M1543 are designed with a very sophisticated I/O circuit and to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the Power On suspend can provide the system a very efficient STAND-ON feature that is more demanding in future home PC systems for Microsoft On Now technology OS.

In the M1533/M1543 of ALADDIN-IV, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one might design a dedicated PMU device to accompany the Power On suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-IV provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

### 3.9 DRAM Refresh

The M1531B provides CAS-before-RAS (CBR) refresh and RAS-only refresh for FPM DRAM, CAS-before-RAS (CBR) refresh and RAS-only refresh and Extended refresh and self refresh for EDO DRAM, and CAS-before-RAS (CBR) refresh and Self refresh for SDRAMs. FPM/EDO refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h Bits[2:0].

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1531B. The M1531B will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read cycle is performed. The M1531B also corrects all single-bit errors and the corrected data is then transferred to the requester (CPU or PCI). This corrected data will not be written back to DRAM in the current M1531B version. The ECC error reporting condition and status are defined in Index 49h-4Ah. The ECC errors are latched until cleared by software. The software programmer can detect ECC errors from 72-bit wide SIMMs or check ECC circuit operations via the ECC test mode (Index 49h bit1 set to ‘1’). The ECC check bits (or parities) can be forced to any value (defined in Index 4Bh) during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLKIN when the ECC feature is enabled.

The M1531B also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 49h bit0 is set to ‘0’. The DRAM parity checking error reporting condition and status also are defined in Index 49h-4Ah. The DRAM parity generation and checking feature will also be supported to the 32-bit only DRAM populated banks. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode. The conventional Parity check will not degrade the system performance.

### 3.10 ECC/Parity Algorithm

The M1531B provides an ECC DRAM data integrity feature when Index 49h bit0 is set to ‘1’. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. But, the ECC algorithm will not be implemented for the 32-bit only DRAM populated banks. The M1531B will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.
Section 4 : Configuration Registers

I. M1531B PCI Mechanism #1 Configuration Cycle Ports

I/O Address : 0CF8h
Register Name : CFGADR - Configuration Address Register
Default Value : 00000000h
Attribute : Read/Write
Size : This register must be 32-bit I/O access in PCI configuration access mechanism #1. An 8-bit or 16-bit access will pass through the Configuration Address Register onto the PCI bus.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 (0)</td>
<td>PCI Configuration Space Access.</td>
</tr>
<tr>
<td>30-24 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>23-16 (00h)</td>
<td>Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to the M1531B and a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on the PCI bus.</td>
</tr>
<tr>
<td>15-11 (00h)</td>
<td>Device Number. It is used by M1531B to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when Bus Number is 0h. As for the others, the M1531B will send the configuration to a PCI or PCI bridge device.</td>
</tr>
<tr>
<td>10-8 (0h)</td>
<td>Function Number. It is used to select a specific device function during initialization.</td>
</tr>
<tr>
<td>7-2 (00h)</td>
<td>Register Number. It is used to select a specific register during initialization.</td>
</tr>
<tr>
<td>1-0 (0h)</td>
<td>Reserved. Fixed at '00'.</td>
</tr>
</tbody>
</table>

I/O Address : 0CFCh
Register Name : CFGDAT - Configuration Data Register
Default Value : 00000000h
Attribute : Read/Write
Size : This register may be 8-bit or 16-bit or 32-bit I/O access in configuration access mechanism #1.
Description : This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU access of 8, 16 or 32-bit wide to this register are supported.

Note : M1531B only supports PCI mechanism #1 access.
II. M1531B PCI Configuration Space Mapped Registers

The M1531B will respond to CPU/PCI configuration access for which AD16 is high during the address phase.

<table>
<thead>
<tr>
<th>Register Index</th>
<th>01h-00h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Name</td>
<td>VID - Vendor Identification Register</td>
</tr>
<tr>
<td>Default Value</td>
<td>10B9h</td>
</tr>
<tr>
<td>Attribute</td>
<td>Read Only</td>
</tr>
<tr>
<td>Size</td>
<td>16 bits</td>
</tr>
<tr>
<td>Description</td>
<td>This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Index</th>
<th>03h-02h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Name</td>
<td>DID - Device Identification Register</td>
</tr>
<tr>
<td>Default Value</td>
<td>1531h</td>
</tr>
<tr>
<td>Attribute</td>
<td>Read Only</td>
</tr>
<tr>
<td>Size</td>
<td>16 bits</td>
</tr>
<tr>
<td>Description</td>
<td>This is a 16-bit value assigned to the M1531B.</td>
</tr>
</tbody>
</table>
### Register Index: COM - Command Register

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>05h-04h</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-9 (000h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>8 (0)</td>
<td>Enable the SERRJ Output Driver.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>SERRJ uses an o/d (Open Drain) pad in M1531B. The motherboard design should use a pull-up resistor (2.2KΩ) to keep this pin logic high. When the DRAM ECC/Parity check or the PCI Parity check is enabled and an error is found, the M1531B will drive SERRJ low to M1533/M1543 to generate NMI when this bit is enabled. Disabling the SERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 once memory has been scrubbed by BIOS in systems that wish to report DRAM ECC/Parity error.</td>
</tr>
<tr>
<td>7 (0)</td>
<td>Enable Address/Data Stepping. M1531B does not support this feature. Write to this bit has no effect.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Respond to Parity Errors.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>The M1531B will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M1531B will assert SERRJ and set the Parity Error Bit in the DS register.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Enable VGA Palette Snooping. M1531B does not support this feature. Write to this bit has no effect.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Enable Postable Memory Write Command. M1531B does not support this feature. Write to this bit has no effect.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Enable Special Cycle. M1531B does not support this feature. Write to this bit has no effect.</td>
</tr>
<tr>
<td>2 (1)</td>
<td>Control to Act As a PCI Bus Master. M1531B does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect.</td>
</tr>
<tr>
<td>1 (1)</td>
<td>Enable Response to Memory Access. M1531B always accepts PCI master accesses to local memory. Write to this bit has no effect.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>Enable Response to I/O Access. M1531B does not respond to any PCI master I/O accesses. Write to this bit has no effect.</td>
</tr>
</tbody>
</table>
Register Index : 07h-06h
Register Name : DS - Device Status Register
Default Value : 0400h
Attribute : Read Only, Read/Write Clear
Size : 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 (0)</td>
<td>Detected Parity Error. This bit is set by the M1531B whenever it detects a parity error in a PCI transaction even if parity error handling is disabled (as controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.</td>
</tr>
<tr>
<td>14 (0)</td>
<td>Signalled System Error. The M1531B will set this bit whenever it asserts SERRJ. Software can reset this bit to 0 by writing a 1 to it.</td>
</tr>
<tr>
<td>13 (0)</td>
<td>Received Master Abort. This bit is set by M1531B whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>12 (0)</td>
<td>Received Target Abort. This bit is set by the M1531B whenever its initiated transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>11 (0)</td>
<td>Send Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M1531B never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.</td>
</tr>
<tr>
<td>10-9 (10)</td>
<td>DEVSELJ Timing.</td>
</tr>
<tr>
<td></td>
<td>00 : Fast.</td>
</tr>
<tr>
<td></td>
<td>01 : Medium.</td>
</tr>
<tr>
<td></td>
<td>10 : Slow.</td>
</tr>
<tr>
<td></td>
<td>The M1531B timing for DEVSELJ assertion. Slow timing is selected.</td>
</tr>
<tr>
<td>8-0 (000h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Register Index : 08h
Register Name : RI - Revision ID Register
Default Value : B0h (B0 Stepping)
Attribute : Read Only
Size : 8 bits
Description : This register contains the version number of M1531B. The value 01 means A0 stepping.

Register Index : 0Bh-09h
Register Name : CC - Class Code Register
Default Value : 060000h
Attribute : Read Only
Size : 24 bits
Description : These registers contain the Class Codes of the M1531B.
Register Index : 0Dh  
Register Name : LT - PCI Latency Timer value  
Default Value : 20h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3 (04h)</td>
<td>Master Latency Timer Count Value. LT is used to control the amount of time the M1531B, as a bus master, can burst data to the PCI Bus. It can be used to guarantee a minimum amount of the system resources.</td>
</tr>
<tr>
<td>2-0 (0h)</td>
<td>Reserved. They are assumed to be 0 when determining the Count Value.</td>
</tr>
</tbody>
</table>

Register Index : 2Bh-0Eh  
Register Name : Reserved Registers  
Default Value : 00h  
Attribute : Read Only

Register Index : 2Dh-2Ch  
Register Name : SVID - Sub-Vendor Identification  
Default Value : 10B9h  
Attribute : Lock Read Only  
Size : 16 bits  
Description : If Index-70h bit3 = 1, then this port can be Read or Write.

Register Index : 2Fh-2Eh  
Register Name : SDID - Sub-Device Identification  
Default Value : 1531h  
Attribute : Lock Read Only  
Size : 16 bits  
Description : If Index-70h bit3 = 1, then this port can be Read or Write.

Register Index : 3Fh-30h  
Register Name : Reserved Registers  
Default Value : 00h  
Attribute : Read Only
### Register: L2CP - L2 Cache Performance

**Register Index:** 40h  
**Register Name:** L2CP - L2 Cache Performance  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (0h)   | **TAG8O, RASJ[5:4] as TAG[9:10] feature option**  
00 : Tag8O are disabled  
01 : Tag8O are enabled  
10 : Tag8O are enabled  
11 : Tag8O are enabled  

**Bit Function Details:**  
  - 00 : Tag8O are disabled  
  - 01 : Tag8O are enabled  
  - 10 : Tag8O are enabled  
  - 11 : Tag8O are enabled  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 5 (0)      | Fast NAJ asserted in CPU single write cycle.  
0 : Disable.  
1 : Enable.  

This bit controls the NAJ assertion point during CPU single write cycle. When enabled, NAJ will assert at T2 instead of T3 to achieve the best CPU single write performance. Value 1 is recommended during normal operation.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 4 (0)      | L1 Snoop HITMJ Check Point.  
0 : 3rd CPU Clock after asserting EADSJ.  
1 : 2nd CPU Clock after asserting EADSJ.  

This bit controls the HITMJ strobe point during L1 snoop cycle. Value 1 is recommended during normal operation.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 3-1 (0h)   | Reserved.  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 0 (0)      | Hit/Miss Check Point (L2 Hit/Miss & DRAM Page Hit/Miss).  
0 : T3end (3rd CPU Clock after Sampling ADSJ).  
1 : T2end (2nd CPU Clock after Sampling ADSJ).  

This bit controls the cycle checkpoint of L2 & DRAM access. Value 1 is recommended for the CPU bus frequency equal or less than 75 Mhz. In 83.3 Mhz CPU bus frequency configuration, value 0 is recommended for the best system reliability.
Register Index: **41h**  
Register Name: **L2CCI - L2 Cache Configuration-1**  
Default Value: Hardware Strobe Value  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0/1)    | L2 Cache Bank Select.  
            0 : 2-bank Pipelined Burst SRAM / Memory Cache.  
            1 : 1-bank Pipelined Burst SRAM / Memory Cache.  
            The default value is determined by hardware strobe from HA[24]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache. |
| 6 (0/1)    | L2 Cache Type Select.  
            0 : Memory Cache.  
            1 : Pipelined Burst SRAM.  
            The default value is determined by hardware strobe from HA[23]. The system must implement the correct hardware strobe for Memory Cache use. |
| 5 (0)      | Reserved. |
| 4 (0)      | Internal MESI Software Test Mode.  
            0 : Disable.  
            1 : Enable.  
            This bit can be used to test internal MESI tag bits by software. It must be kept to '0' in normal operation. Please refer to the MESI Software Test Mode Section 5.5. |
| 2-1 (0/1,0/1) | L2 Cache Size.  
              00 : None.  
              01 : 256K.  
              10 : 512K.  
              11 : 1M.  
              The default value is determined by hardware strobe from HA[22:21]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache. |
| 3,0 (00)   | Must be set as '10' |
The following L2 Cache Table shows the different configurations supported by M1531B.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>DATA SRAM</th>
<th>TAG SRAM</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Index-41h bits[2:1]</td>
<td>Cache size</td>
<td>Bank Addr Lines</td>
<td>Addr Lines</td>
</tr>
<tr>
<td>01</td>
<td>256K</td>
<td>(32K32)*2</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(64K16)*4</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(32K32)*4</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>1M</td>
<td>(64K32)*4</td>
<td>2</td>
</tr>
<tr>
<td>01</td>
<td>256K</td>
<td>(32K32)*2</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(64K16)*4</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(32K32)*4</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>1M</td>
<td>(64K32)*4</td>
<td>2</td>
</tr>
<tr>
<td>01</td>
<td>256K</td>
<td>(32K32)*2</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(64K16)*4</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(32K32)*4</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>1M</td>
<td>(64K32)*4</td>
<td>2</td>
</tr>
<tr>
<td>01</td>
<td>256K</td>
<td>(32K32)*2</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>512K</td>
<td>(64K16)*4</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>1M</td>
<td>(64K32)*4</td>
<td>2</td>
</tr>
</tbody>
</table>
Register Index: 42h  
Register Name: L2CCII - L2 Cache Configuration-2  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)       | L2 TAG Output Delay.  
             | 0 : Disable.  
             | 1 : Enable. |
|             | This bit is used to increase L2 Tag data hold time when M1531B wants to update the L2 Tag content. The M1531B will delay the Tag data output floating timing by one half CPU clock when this bit is enabled. A '1' is recommended in normal operation. |
| 6 (0)       | CPU Single Read Cycle L2 Cache Allocation.  
             | 0 : Disable.  
             | 1 : Enable. |
|             | When this bit is disabled, the M1531B will only do the L2 Cache allocation after it decodes the CPU burst line-fill cycle. The CPU single read cycle will start a DRAM single read cycle if this cycle is a DRAM cycle and not hit the L2 Cache. When this bit is enabled, the M1531B will also do the L2 Cache allocation after it decodes the CPU single read cycle. The M1531B will issue the AHOLD to hold CPU cycle, start a burst DRAM read cycle to get the whole line data, write the date to the L2 Cache, and then de-assert AHOLD and return the BRDYJ to CPU. This feature is used to increase the L2 hit rate when CPU issues the single cycle instead of the line-fill cycle in some special application. A '1' is recommended in normal operation. |
| 5 (0)       | Cacheability of Address Region from A0000h to BFFFFh.  
             | 0 : Disable.  
             | 1 : Enable. |
|             | This bit is used to enable the cacheability of address region from A0000h to BFFFFh if this region is programmed as local memory (Index-47h bit3 = 1). If Index-47h bit3 = 0, this bit must be 0. |
| 4 (0)       | L2 Dirty Bit Setting.  
             | 0 : Normal.  
             | 1 : Force Non-dirty (Dirty Bit =0). |
|             | When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force non-dirty. This bit is used to initialize L2 cache. Please refer to the hardware and software setup section. |
| 3 (0)       | Reserved. |
| 2 (0)       | L2 Cache Miss or Invalidate.  
             | 0 : Normal.  
             | 1 : Force L2 Cache Miss or Invalidate. |
|             | When this bit is set to 1, all tag lookups result in a miss. This bit is used to initialize L2 cache. Please refer to the hardware and software setup section. |
| 1 (0)       | L2 Dirty Bit Setting.  
             | 0 : Normal.  
             | 1 : Force Dirty (Dirty Bit =1). |
|             | When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force dirty. This bit can be used to flush L2 cache in green application. Software can set this bit and then read all L2 cache tag address to flush the cache. |
| 0 (0)       | L2 Cache ON/OFF.  
             | 0 : Disable External Cache.  
             | 1 : Enable External Cache. |
|             | This bit is used to disable or enable L2 cache. |
Register Index : 43h
Register Name : L1CDBC - L1 Cache/DRAM Buffer Control
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Row 5 (RAS5J) Populated with 32-bit DRAM.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Row 4 (RAS4J) Populated with 32-bit DRAM.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Row 3 (RAS3J) Populated with 32-bit DRAM.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Row 2 (RAS2J) Populated with 32-bit DRAM.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Row 1 (RAS1J) Populated with 32-bit DRAM.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>The M1531B supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Supports DRAM Posted Write Buffer Read-Around-Write Cycle.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control buffer for back-to-back CPU write and read cycles. Since the M1531B implements the DRAM write buffer to post CPU write cycles, the M1531B will do the read first and then flush the DRAM write buffer if this feature is enabled and the required data of the read cycle do not reside in the buffer. When this bit is disabled, the M1531B will flush the DRAM write buffer data first, and then do the CPU read cycle. A ‘1’ is recommended for normal operation.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>L1 Cache ON/OFF.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable Internal Cache.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable Internal Cache</td>
</tr>
<tr>
<td></td>
<td>This bit is used to disable or enable L1 cache. When this bit is reset to 0, the M1531B will negate KENJ to prevent either L1 or L2 line fill. When this bit is set to ‘1’, the M1531B will assert KENJ for cacheable memory cycles.</td>
</tr>
</tbody>
</table>
Register Index: **44h**  
Register Name: **DTCI - DRAM Timing Configuration - 1**  
Default Value: **00h**  
Attribute: **Read/Write**  
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (00)   | EDO Detection Timer.  
00: 128 CPU Clocks.  
01: 256 CPU Clocks.  
10: 512 CPU Clocks.  
11: 1024 CPU Clocks.  
These two bits combined with bit 5 are used to do the EDO detection. |
| 5 (0)      | EDO Detection Mode.  
0: Disable.  
1: Enable.  
For the EDO detection procedure, please refer to the DRAM type detection figure in the Hardware and Software programming section. |
| 4 (0)      | EDO Page mode DRAM Read Timing.  
0: X-3-3-3.  
1: X-2-2-2.  
This bit is used to control EDO DRAM read timing. Please refer to lead off table in Section 3.5.3 to check the X value. |
| 3 (0)      | RAS-to-CAS Delay Time.  
0: 3T.  
1: 2T.  
This bit controls the RASJ to CASJ delay. T is the CPU clock cycle. |
| 2 (0)      | RAS Pre-charge Period.  
0: 4T, and Refresh RAS Assertion 5T.  
1: 3T, and Refresh RAS Assertion 4T.  
This bit controls the RASJ pre-charge high time in row miss and refresh cycle. T is the CPU clock cycle. |
| 1 (0)      | Page Mode DRAM Read Timing.  
0: X-4-4-4 (CASJ: 1H+3L).  
1: X-3-3-3 (CASJ: 1H+2L).  
This bit is used to control the Page Mode DRAM read timing. Please refer to lead off table in Section 3.5.3 to check the X value. |
| 0 (0)      | EDO or Page Mode DRAM Write Timing.  
0: X-3-3-3.  
1: X-2-2-2.  
This bit is used to control the EDO or Page Mode DRAM write timing. Please refer to lead off table in Section 3.5.3 to check the X value. |
Register Index: 45h
Register Name: DTCII - DRAM Timing Configuration -2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Enhanced DRAM Paging Feature. 0: Disable. 1: Enable. When this bit is enabled, the M1531B will use additional information to close the DRAM page in advance. That is, during DRAM irrelevant cycles, an intelligent guess is done to de-assert the RASJ lines and pre-charge them for later use. This bit is recommended to be set ‘1’ in normal operation to enhance DRAM performance.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>DRAM Bank Miss Detection. 0: Disable 1: Enable When this bit is enabled, the M1531B enhances the DRAM bank-miss performance. This bit is recommended to be set ‘1’ during normal operation to enhance DRAM performance.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Read Speculative Leadoff Enable. 0: Disable 1: Enable (CASJ Pre-asserted in T2 when Memory Read). This bit is valid only if index-40h bit 0 =’1’. When set to ‘1’, the DRAM controller read request is presented 1 CPU clock earlier than it normally is, before the final memory target has been decoded. If the memory cycle does not actually target DRAM, the DRAM state machine will terminate and return back its previous state.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Refresh Mode. 0: CAS-before-RAS Mode. 1: RAS-only Mode. This bit is used to control DRAM refresh mode. In suspend mode, only the CAS-before-RAS mode is supported to save power consumption.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>CPU/PCI Master to DRAM Page Mode. 0: DRAM use Page Mode. 1: DRAM use Non-page Mode. When this bit is set to ‘1’, the M1531B will close the DRAM page after DRAM access. Otherwise, it will keep DRAM page open until next access.</td>
</tr>
<tr>
<td>2-0 (0h)</td>
<td>Refresh period. 000: 1024 CPU Clocks (15 us in 66Mhz). 001: 2048 CPU Clocks (30 us in 66Mhz). 010: 4096 CPU Clocks (60 us in 66Mhz). 011: 8192 CPU Clocks (120 us in 66Mhz). 100: 16384 CPU Clocks (256 us in 66Mhz). These three bits are used to control the period to refresh DRAMs.</td>
</tr>
</tbody>
</table>
Register Index: **46h**  
Register Name: **PIPEF - Pipe Function**  
Default Value: **00h**  
Attribute: **Read/Write**  
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (00)   | RASJ de-asserted in CPU Bus Idle.  
            | 00: after 2 CPU Clocks.  
            | 01: after 4 CPU Clocks.  
            | 10: after 6 CPU Clocks.  
            | 11: after 8 CPU Clocks.  
            | These two bits are used to enhance the DRAM Page Miss performance. M1531B will de-assert the RASJ after programmed number of CPU Clocks. This function is enabled when Index-45h bit7 = 1. |
| 5 (0)      | Supports Dynamic Write-Back for Burst Writes.  
            | 0: Disable.  
            | 1: Enable.  
            | This feature is used to optimize DRAM buffer usage. When CPU issues a burst write cycle and hits to the L2 Cache, the burst data will write to L2 cache and also the DRAM Posted Write Buffer if the feature is enabled and the buffer is not full. It can keep L2 cache clean to speed up later L2 cache accesses. If this feature is disabled, the CPU hit L2 Cache burst write cycle will directly write to L2 Cache and make the hit line as dirty in L2 Tag. |
| 4 (0)      | Supports Dynamic Write-Back for Single Write.  
            | 0: Disable.  
            | 1: Enable.  
            | This feature is used to optimize DRAM buffer usage. When CPU issues a single write cycle and hits to the L2 Cache, the single data will write to L2 cache and also the DRAM Posted Write Buffer if the feature is enabled and the buffer is not full. It can keep L2 cache clean to speed up later L2 cache accesses. If this feature is disabled, the CPU hit L2 Cache single write cycle will directly write to L2 Cache and make the hit line as dirty in L2 Tag. |
| 3 (0)      | Fast DRAM Line Fill in L2 Write Back.  
            | 0: Disable.  
            | 1: Enable.  
            | When CPU issues a line fill cycle, the M1531B will decode this cycle at the cycle check point (defined by Index-40h bit 0). If the cycle address is L2 Cache miss, the M1531B will issue a DRAM burst read cycle and write the data to L2 Cache and return the data to CPU at the same time. If the replaced line is dirty, the M1531B also needs to write back the L2 data to DRAM buffer. This bit is used to control the sequence when this condition happens. When this bit is disabled, the M1531B will first write back the dirty L2 data to DRAM buffer, and then start the DRAM state machine to read the burst data to CPU and also write the L2 Cache. If this bit is enabled, the M1531B will write back the dirty data and start the state machine concurrently. The M1531B will intelligently control the state machine to reduce the wait state when this kind of system behavior happens. |
| 2 (0)      | DRAM Pipelined Function Option.  
            | 0: Disable.  
            | 1: Enable.  
            | This bit is used to enable the assertion of NAJ when the cycle is a DRAM access cycle. When this bit is disabled, the M1531B will not assert NAJ during DRAM access. |
| 1 (0)      | L2 Pipelined Function Option.  
            | 0: Disable.  
            | 1: Enable.  
            | This bit is used to enable the assertion of NAJ when the cycle is an L2 access cycle. When this bit is disabled, the M1531B will not assert NAJ during L2 access. |
| 0 (0)      | Flush DRAM Buffer in CPU Bus Idle.  
            | 0: Disable.  
            | 1: Enable.  
            | This bit is used to enable the DRAM buffer flush when CPU bus is idle. M1531B will flush the DRAM buffer when the CPU bus is idle. |
Register Index : 47h  
Register Name : MISI - Miscellaneous-1  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | Supports Cyrix M1/M2 "1+4" Burst Mode & K6 Write Allocation Feature.  
0 : Disable.  
1 : Enable.  
This bit is used to support the Cyrix M1/M2 "1+4" mode to toggle cache address, DRAM Memory address, and issues the correct KENJ disregarding CPU CACHEJ if it is a local memory cycle. This bit is also used to support K6 Write Allocation Feature. If this bit is enabled, M1531B will assert KENJ during CPU single local memory write cycle.  
| 6 (0)      | Supports M1/M2 Linear Burst Order.  
0 : Disable.  
1 : Enable.  
This bit is used to support the Cyrix M1/M2 linear burst mode to toggle cache address and DRAM Memory address. When it is disabled, Intel toggle mode (interleaved burst) is selected.  
| 5 (0)      | 14-15M Memory Location.  
0 : Local Memory Area.  
1 : Non-Local Memory Area.  
When this bit is set to '0', all memory access address from 14M to 15M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 15M. Otherwise, it will be decoded as non-local memory and pass through PCI bus.  
| 4 (0)      | 15-16M Memory's Location.  
0 : Local Memory Area.  
1 : Non-Local Memory Area.  
When this bit is set to '0', all memory access address from 15M to 16M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 16M. Otherwise, it will be decoded as non-local memory and pass through PCI bus.  
| 3 (0)      | Page A-B as Local Memory Area.  
0 : Non-local Memory Area.  
1 : Local Memory Area.  
When this bit is set to '1', all memory access address from A0000h to BFFFFh will be decoded as local memory cycle and access local DRAM. Otherwise, it will be decoded as non-local memory and pass through PCI bus.  
| 2 (0)      | Force Address Region 80000h-9FFFFh as Non-local Memory Area.  
0 : Local Memory Area.  
1 : Non-local Memory Area.  
When this bit is set to '1', all memory access address from 80000h to 9FFFFh will be decoded as non-local cycle and pass through PCI bus. Otherwise, it will be decoded as local memory and access to DRAM.  
| 1-0 (00)   | Reserved. |
Register Index: 48h
Register Name: SMRM - SMRAM Mapping
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (0h)</td>
<td>Refresh period adjustment when CPU clock changes. 00: Refresh period/1 when CPU clock/1. 01: Refresh period/2 when CPU clock/2. 10: Refresh period/4 when CPU clock/4. 11: Refresh period/8 when CPU clock/8. These bits are used to change the refresh period when CPU clock frequency has been changed in some green applications. When CPU clock has slowed down, BIOS should change these bits setting to recompensate the refresh period.</td>
</tr>
<tr>
<td>5 (0h)</td>
<td>NAJ assert delay 1T in SDRAM cycle. 0: disable 1: enable</td>
</tr>
<tr>
<td>4 (0)</td>
<td>SMM Page -A or -B Region Code/Data Split. 0: Disable. 1: Enable. <strong>Note:</strong> This bit is valid only if this register bit [3:2]=&quot;01&quot;. When this bit is enabled, only the cycle command with DCJ='0' can access SMRAM. The CPU data access will pass through PCI bus.</td>
</tr>
<tr>
<td>3-2 (00)</td>
<td>SMRAM Region. 00: SMM Region at D000 Segment will be re-mapped to B000 Segment. 01: SMM Region at A000 or B000 Segment. 10: SMM Region at 3000 Segment will be re-mapped to B000 Segment. 11: Reserved. Please refer to the following table.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>SMRAM Access Control. 0: Disable. 1: Enable. When this bit is disabled, SMRAM can only be accessed during SMI handler. Otherwise, SMRAM area can be accessed any time. This bit is used in SMRAM initialization and must be set to '0' when the initialization process is finished</td>
</tr>
<tr>
<td>0 (0)</td>
<td>Supports SMRAM Mapping. 0: Disable. 1: Enable. This bit is used to disable or enable SMRAM Mapping.</td>
</tr>
</tbody>
</table>
The following is M1531B address re-mapping table for SMRAM mapping enable.

<table>
<thead>
<tr>
<th>Bit 3-2-1</th>
<th>SMIACTJ</th>
<th>CPU Logical Address</th>
<th>Re-mapped Physical Address</th>
<th>Access DRAM Y/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
<td>D0000</td>
<td>B0000</td>
<td>Y</td>
</tr>
<tr>
<td>000</td>
<td>1</td>
<td>D0000</td>
<td>non-local</td>
<td>N</td>
</tr>
<tr>
<td>001</td>
<td>X</td>
<td>D0000</td>
<td>B0000</td>
<td>Y</td>
</tr>
<tr>
<td>010</td>
<td>0</td>
<td>A0000/ B0000</td>
<td>A0000/ B0000</td>
<td>Y</td>
</tr>
<tr>
<td>010</td>
<td>1</td>
<td>A0000/ B0000</td>
<td>non-local</td>
<td>N</td>
</tr>
<tr>
<td>011</td>
<td>X</td>
<td>A0000/ B0000</td>
<td>A0000/ B0000</td>
<td>Y</td>
</tr>
<tr>
<td>100</td>
<td>0</td>
<td>30000</td>
<td>B0000</td>
<td>Y</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
<td>30000</td>
<td>30000</td>
<td>Y</td>
</tr>
<tr>
<td>101</td>
<td>X</td>
<td>30000</td>
<td>B0000</td>
<td>Y</td>
</tr>
</tbody>
</table>
Register Index: 49h  
Register Name: ECCP - ECC/Parity Feature  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 6 (0)      | SERRJ Duration.  
0 : SERRJ will be asserted for 1 PCI Clock.  
1 : SERRJ will be asserted until all the ECC/parity Error Flags are cleared.  
When the M1531B detects an ECC or parity error, the M1531B will assert SERRJ for 1 PCI Clock (pulse mode) if this bit is set to '0'. Otherwise, the M1531B will assert the SERRJ to report the memory error until all the ECC/parity error flags are cleared (level mode). This bit is used to control the assertion time of SERRJ. |
| 5 (0)      | SERRJ on Parity or Multiple-bit ECC Error.  
0 : Disable  
1 : Enable.  
When this bit is set to '0', the M1531B will not assert the SERRJ signal when the memory parity or multiple-bit error occurs. Disabling this bit will disable the DRAM parity error check or DRAM ECC multiple-bit error check. Otherwise, the memory data error will be reported to the system via SERRJ assertion to generate NMI (Non-Maskable Interrupt). |
| 4 (0)      | SERRJ on Single-bit ECC Error.  
0 : Disable  
1 : Enable.  
When this bit is set to '0', the M1531B will not assert SERRJ on single-bit DRAM ECC errors. Disabling this bit will disable the DRAM ECC single-bit error check. Otherwise, the M1531B will assert SERRJ to generate NMI (Non-Maskable Interrupt) when it detects a single-bit DRAM ECC error. |
| 3-2 (0h)   | Reserved     |
| 1 (0)      | ECC/Parity Test Mode Enable.  
0 : Disable  
1 : Enable.  
When this bit is set to '1', the ECC check bits or parity bits will be forced to the value defined in register index 4Bh during all the DRAM write cycles. Otherwise, the ECC check bits or parity bits normal function will be performed. This bit must be set to '0' for normal operation. |
| 0 (0)      | DRAM Data Integrity Mode.  
0 : Parity  
1 : ECC.  
When this bit is set to '0', the DRAM data integrity will be implemented by the parity algorithm. Otherwise, the ECC data integrity will be implemented. |
Register Index : 4Ah  
Register Name : **ECCE - ECC or Parity Error Status**  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (0h)</td>
<td>ECC Multiple-bit or Parity First Row error. These 3 bits record the first row associated with the ECC multiple-bit or parity error. When an error is detected, these bits are updated and ECCE[4] is set.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>ECC Multiple-bit Error or Parity Error Flag. The M1531B sets this bit to '1' when either an ECC multiple-bit error or parity error has been detected, depending on whether ECC or parity feature is enabled, respectively. A write of '1' by software to ECCE[4] will clear this bit and write of '0' has no effect on it.</td>
</tr>
<tr>
<td>3-1 (0h)</td>
<td>ECC Single-bit First Row Error. These 3 bits record the first row associated with the ECC single-bit error. When an error is detected, these bits are updated and ECCE[0] is set.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>ECC Single-bit Error Flag. The M1531B sets this bit to '1' when an ECC single-bit error has been detected and the ECC function is enabled. A write of '1' by software to ECCE[0] will clear this bit and write of '0' has no effect on it.</td>
</tr>
</tbody>
</table>

Register Index : 4Bh  
Register Name : **Reserved**  
Default Value : 00h  
Attribute : Read Only  
Size : 8 bits
Register Index : 4Ch  
Register Name : SHADRI - SHADOW Regions Read Enable - 1  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>DC000h-DFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region DC000h-DFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>D8000h-DBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D8000h-DBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>D4000h-D7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D4000h-D7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>D0000h-D3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D0000h-D3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>CC000h-CFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region CC000h-CFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>C8000h-CBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C8000h-CBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>C4000h-C7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C4000h-C7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>C0000h-C3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C0000h-C3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
</tbody>
</table>
Register Index: 4Dh
Register Name: SHADRII - SHADOW Regions Read Enable - 2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>FC000h-FFFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region FC000h-FFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>F8000h-FBFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region F8000h-FBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>F4000h-F7FFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region F4000h-F7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>F0000h-F3FFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region F0000h-F3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>EC000h-EFFFFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region EC000h-EFFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>E8000h-EBFFFh Shadow Region Read Enable</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region E8000h-EBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>E4000h-E7FFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region E4000h-E7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>E0000h-E3FFFh Shadow Region Read Enable.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region E0000h-E3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
</tr>
</tbody>
</table>
Register Index: **4Eh**
Register Name: **SHADWI - SHADOW Regions Write Enable - 1**
Default Value: **00h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7(0)       | DC000h-DFFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region DC000h-DFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 6 (0)      | D8000h-DBFFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region D8000h-DBFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 5 (0)      | D4000h-D7FFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region D4000h-D7FFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 4 (0)      | D0000h-D3FFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region D0000h-D3FFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 3 (0)      | CC000h-CFFFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region CC000h-CFFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 2 (0)      | C8000h-CBFFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region C8000h-CBFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 1 (0)      | C4000h-C7FFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, address region C4000h-C7FFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
| 0 (0)      | C0000h-C3FFFFh Shadow Region Write Enable.  
0 : Disable.  
1 : Enable.  
When the above bits are enabled, the corresponding memory address region write cycle will access local DRAM. Otherwise, it will pass through PCI bus. |
Register Index: 4Fh  
Register Name: SHADWII - SHADOW Regions Write Enable - 2  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>FC000h-FFFFFh Shadow Region Write Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region FC000h-FFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 (0)</td>
<td>F8000h-FBFFFh Shadow Region Write Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region F8000h-FBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 (0)</td>
<td>F4000h-F7FFFh Shadow Region Write Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region F4000h-F7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 (0)</td>
<td>F0000h-F3FFFh Shadow Region Write Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region F0000h-F3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 (0)</td>
<td>EC000h-EFFFFFh Shadow Region Write Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region EC000h-EFFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 (0)</td>
<td>E8000h-EBFFFh Shadow Region Write Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region E8000h-EBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 (0)</td>
<td>E4000h-E7FFFh Shadow Region Write Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region E4000h-E7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 (0)</td>
<td>E0000h-E3FFFh Shadow Region Write Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, address region E0000h-E3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register Index : 50h  
Register Name : SHADCI - SHADOW Regions Cacheable Enable - 1  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | DC000h-DFFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[7] = '1', address region DC000h-DFFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 6 (0)      | D8000h-DBFFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[6] = '1', address region D8000h-DBFFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 5 (0)      | D4000h-D7FFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[5] = '1', address region D4000h-D7FFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 4 (0)      | D0000h-D3FFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[4] = '1', address region D0000h-D3FFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 3 (0)      | CC000h-CFFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[3] = '1', address region CC000h-CFFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 2 (0)      | C8000h-CBFFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[2] = '1', address region C8000h-CBFFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 1 (0)      | C4000h-C7FFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[1] = '1', address region C4000h-C7FFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 0 (0)      | C0000h-C3FFFFh Shadow Region Cacheable Enable.  
             0 : Disable.  
             1 : Enable.  
             When this bit is enabled and SHADRI[0] = '1', address region C0000h-C3FFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
**Register Index:** 51h  
**Register Name:** SHADCII - SHADOW Regions Cacheable Enable - 2  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0) FC000h-FFFFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[7] = '1', address region FC000h-FFFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 6 (0) F8000h-FBFFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[6] = '1', address region F8000h-FBFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 5 (0) F4000h-F7FFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[5] = '1', address region F4000h-F7FFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 4 (0) F0000h-F3FFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[4] = '1', address region F0000h-F3FFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 3 (0) EC000h-EFFFFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[3] = '1', address region EC000h-EFFFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 2 (0) E8000h-EBFFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[2] = '1', address region E8000h-EBFFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 1 (0) E4000h-E7FFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[1] = '1', address region E4000h-E7FFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
| 0 (0) E0000h-E3FFFh Shadow Region Cacheable Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled and SHADRRII[0] = '1', address region E0000h-E3FFFh memory access will become cacheable. Otherwise, it will be non cacheable. |
Register Index : 52h  
Register Name : MISII - Miscellaneous - 2  
Default Value : F0h  
Attribute : Read/Write  
Size : 8 bits  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3 (00h)</td>
<td>SRAM Module Presence Detect Bits HA[31:27] (Read Only). The M1531B will strobe HA[31:27] values and write them into the five-bit register during reset. BIOS can use these five bits to determine the SRAM module configuration and program the L2 size and type.</td>
</tr>
</tbody>
</table>
| 2-1 (00)   | CPU Bus Frequency. (Read Only)  
00 : 60 MHz.  
01 : 66 MHz.  
10 : 75 MHz.  
11 : 83.3 MHz.  
These two bits are hardware strobe from HA[26:25] to indicate the CPU bus frequency. |
| 0 (0)      | PCI/CPU Concurrency Enable.  
0 : Disable.  
1 : Enable.  
When this bit is enabled, CPU to L2 access will be concurrent with PCI-to-DRAM access. Otherwise, PCI to DRAM access will always prevent the CPU from issuing cycles by asserting AHOLD. |

Register Index : 53h  
Register Name : Reserved  
Default Value : 00h  
Attribute : Read Only  
Size : 8 bits  

Register Index : 55h-54h  
Register Name : FBMR - PCI Programmable Frame Buffer Memory Region  
Default Value : FFFFh  
Attribute : Read/Write  
Size : 16 bits  

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-4(000)</td>
<td>Base address of Programmable Frame Buffer. The 12-bits correspond to A[31:20] of the starting address. The remaining bits A[19:0] are assumed to be zero. These bits combined with bits 3-0 can determine the Frame Buffer starting address and stopping address. When Index-56h bit 0 is set to '1', the M1531B will decode the boundary and enable CPU to PCI write buffer.</td>
</tr>
</tbody>
</table>
| 3-0(0)     | Size of Programmable Frame Buffer.  
X000 : 1 Mbytes.  
X001 : 2 Mbytes  
X010 : 4 Mbytes.  
X011 : 8 Mbytes.  
X100 : 16 Mbytes.  
Others : Reserved.  
These bits are used to program the Frame Buffer Size. |

Note : The Frame Buffer Region should not overlap with local memory.
Register Index : 56h  
Register Name : H2PW - CPU to PCI Write Buffer Option  
Default Value : 00h  
Attribute : Read/Write  
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Host to PCI Write Buffered Cycle Selection.</td>
</tr>
<tr>
<td></td>
<td>0 : Only CPU Memory Write to PCI Frame Buffer.</td>
</tr>
<tr>
<td></td>
<td>1 : All CPU to PCI Memory Write Cycle.</td>
</tr>
<tr>
<td></td>
<td>If this bit is enabled, all non-local memory cycle will enable the CPU to PCI write buffer. Otherwise, only programmable Frame Buffer or fixed A/B segment Frame Buffer will utilize the Host to PCI write buffer.</td>
</tr>
<tr>
<td>6 (0)</td>
<td>Linear-merge for Frame Buffer Cycle.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, only the consecutive linear increased addresses can be merged. Otherwise, the second write cycle will write into a new Host to PCI Write Buffer location instead of merging with the previous buffer location posted by the first write cycle.</td>
</tr>
<tr>
<td>5 (0)</td>
<td>Word-merge for Frame Buffer Cycle.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable the word-merge feature for Frame Buffer cycle. When this feature is enabled, the M1531B will merge the latter 16-bit Frame Buffer write data into the previous buffer location posted by the previous 16-bit Frame Buffer write data if the HBEJ[7:0] are mergeable. The M1531B will check the CPU HBEJ[7:0] and determine if they can be merged or not.</td>
</tr>
<tr>
<td>4 (0)</td>
<td>Byte-merge for Frame Buffer Cycle.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable the byte-merge feature for Frame Buffer cycle. When this feature is enabled, the M1531B will merge the latter 8-bit Frame Buffer write data into the previous buffer location posted by the previous Frame Buffer write data if the HBEJ[7:0] are mergeable. The M1531B will check the CPU HBEJ[7:0] and determine if they can be merged or not.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Use PCI Fast Back-to-Back.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable PCI Fast Back-to-Back capability. If this bit is enabled, consecutive PCI write cycles targeted to the same slave will become fast back-to-back cycle on the PCI bus.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Use PCI Write-Burst.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable PCI write burst capability. If this bit is enabled, the consecutive PCI write cycles will become a burst cycle on the PCI bus.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>VGA 0A0000-0BFFFF Fixed Frame Buffer.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to enable 0A0000h-0BFFFFh Frame Buffer and the Host to PCI Write Buffer.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>Programmable Frame Buffer.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to combine with index 55h-54h to enable the programmable PCI Frame Buffer and the Host to PCI Write Buffer.</td>
</tr>
</tbody>
</table>
Register Index: 57h  
Register Name: H2PO - CPU to PCI Option  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
| 6 (0)      | APIC Support, Invalidate PCI to DRAM Read Ahead Buffer When PHLDAJ Goes Low.  
            | 0 : Disable.  
            | 1 : Enable.  
            |   When APIC is supported in Dual Processor system, this bit must be set to ‘1’ to invalidate PCI to DRAM Read Ahead Buffer since the M1531B cannot realize Interrupt Synchronous event. But in Single Processor systems, the M1531B can detect Interrupt Synchronous event to invalidate PCI to DRAM Read Ahead Buffer automatically. This bit is recommended to be reset to ‘0’ in Single Processor systems.  |
| 5 (0)      | Translate CPU Shutdown cycle to Port 92 cycle.  
            | 0 : Enable.  
            | 1 : Disable.  
            |   When this bit is set to ‘1’, the M1531B will forward a Shut-down Special cycle from CPU bus to PCI bus. When this bit is reset to ‘0’, the M1531B will write 01h to I/O address port 92 on PCI bus.  |
| 4-0 (00h)  | Reserved.    |
Register Index: 58h
Register Name: P2HO - PCI to Main Memory / PCI Arbiter Option
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>PCI Master GAT mode</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td>6-3 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>CPU Access PCI During Passive Release.</td>
</tr>
<tr>
<td></td>
<td>0: Disable.</td>
</tr>
<tr>
<td></td>
<td>1: Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit controls CPU to PCI access during Passive Release. When it is enabled, CPU to PCI access is allowed during Passive Release. Otherwise, arbiter only accepts another PCI master access to local DRAM.</td>
</tr>
<tr>
<td>1 (0)</td>
<td>Passive Release of PHOLD.</td>
</tr>
<tr>
<td></td>
<td>0: Disable.</td>
</tr>
<tr>
<td></td>
<td>1: Enable.</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, the M1531B will recognize Passive Release signaled from M1533/M1543 by de-asserting PHOLDJ for a PCI Clock and then asserting PHOLDJ for a PCI Clock. The M1531B will de-assert the PHLDAJ signal and re-arbitrate PCI bus request and possibly allow the CPU to access PCI depending on the bit 2 setting. When this bit is disabled, the M1531B does not recognize Passive Release, i.e., PHLDAJ will be continued to be asserted. A value '1' is recommended for normal operation.</td>
</tr>
<tr>
<td>0 (0)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Register Index: 59h
Register Name: PCIM - PCI Master Time Slice
Default Value: 20h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Number of PCI clocks for PCI Master time slice. The Time-Slice will guarantee the minimum clocks that the PCI master is granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. The bits [1:0] are assumed to be &quot;00&quot; and are ignored.</td>
</tr>
</tbody>
</table>

Register Index: 5Ah
Register Name: CPUM - CPU Master Time Slice
Default Value: 20h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Number of PCI clocks for CPU Bus time slice. The Time-Slice will guarantee the minimum clocks that the CPU master is granted the ownership of PCI bus. The time-slice counter is started when CPU grant is asserted and bus is idle. The bits [1:0] are assumed to be &quot;00&quot; and are ignored.</td>
</tr>
</tbody>
</table>
Register Index: **5Bh**  
Register Name: **PCIRC - PCI Retry control for P2H cycle**  
Default Value: **00h**  
Attribute: **Read/Write**  
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0h)</td>
<td><strong>Reserved.</strong></td>
</tr>
</tbody>
</table>
| 6 (0)      | **Retry PCI Master when address crosses buffer boundary.**  
             | **0 : disable**  
             | **1 : enable**  
             | When this bit is set, PCI arbiter will become more fair to retry the PCI master if it occupies PCI bus too long. A '1' is recommended in normal operation. |
| 5-4 (0h)   | **Reserved**                                                                                                      |
| 3-2 (00)   | **Retry Latency for Second Data Phase Control.**  
             | **00 : Retry on Second Data Phase if Wait State > 8 PCI Clocks.**  
             | **01 : Retry on Second Data Phase if Wait State > 4 PCI Clocks.**  
             | **10 : Retry on Second Data Phase if Wait State > 2 PCI Clocks.**  
             | **11 : Never Retry on Second Data Phase.**  
             | These bits are used to retry a PCI master cycle when the latency to the second data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1531B will complete the second data transfer regardless of latency. |
| 1-0 (00)   | **Retry Latency for First Data Phase Control.**  
             | **00 : Retry on First Data Phase if Wait State > 32 PCI Clocks.**  
             | **01 : Retry on First Data Phase if Wait State > 16 PCI Clocks.**  
             | **10 : Retry on First Data Phase if Wait State > 8 PCI Clocks.**  
             | **11 : Never Retry on first Data phase.**  
             | These bits are used to retry a PCI master cycle when the latency to the first data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1531B will complete the first data transfer regardless of latency. |
Register Index: 5Ch
Register Name: SDRAMCI - Synchronous DRAM Control Register I
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5 (0h)</td>
<td>SDRAM Operation Mode Selection.</td>
</tr>
<tr>
<td></td>
<td>000: Normal Operation (Default).</td>
</tr>
<tr>
<td></td>
<td>001: NOP (No Operation) Command Enable.</td>
</tr>
<tr>
<td></td>
<td>010: PALL (Pre-charge All Banks) Command Enable.</td>
</tr>
<tr>
<td></td>
<td>011: MRS (Mode Register Set) Command Enable.</td>
</tr>
<tr>
<td></td>
<td>100: CBR (CAS Before RAS Refresh) Enable.</td>
</tr>
<tr>
<td></td>
<td>Others: Reserved.</td>
</tr>
</tbody>
</table>

Note: (1) Before switching from one mode of SDRAM to another, the BIOS should ensure the DRAM buffer is empty. For example, by issuing a DRAM read cycle to flush the DRAM buffer. (2) In the MRS mode, the MA is translated as the column address and the BIOS should issue the appropriate CPU addresses to program the SDRAMs. NOP mode is used to force all CPU cycles to DRAM to generate an SDRAM NOP command on the memory interface. PALL mode is used to force all CPU cycles to DRAM to generate an SDRAM pre-charge all banks command on the memory interface. MRS command is used to convert all CPU cycles to commands on the memory interface. MA[11:0] lines are used to drive command: MA[2:0] = '010' for burst of 4 mode, MA[3]= '1/0' for interleave/linear wrap mode, MA[4]= '1/0' for the value of CAS Latency (3 HCLKIn / 2 HCLKIn), MA[6:5]= '01' and MA[11:7]= '00000'. All these modes are used to initialize SDRAM. Please refer to the hardware and software setup section.

4 (0) CAS Latency.
0 : 3 HCLKIn's.
1 : 2 HCLKIn's.
This bit is used to control read data valid wait states after read command has been issued. '0' means the CAS Latency is 3 HCLKIn's, and 1 means the CAS Latency is 2 HCLKIn's.

3 (0) RAS Active to Read/Write Command Delay Time (tRCD).
0 : 3 HCLKIn's.
1 : 2 HCLKIn's.
This bit is used to control RASJ to CASJ delay. The same programmed value as bit 4 is highly recommended for normal operation.

2-1 (0h) RAS Pre-charge Timing (in HCLKIn's).
RAS Pre-charge RAS Active to Refresh/RAS-Active to Time (tRP)
Pre-charge Time (tRAS)
Refresh/RAS-Active Time (tRC)
<table>
<thead>
<tr>
<th>tRP</th>
<th>tRAS</th>
<th>tRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td>01</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>10</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>11</td>
<td>2</td>
<td>5</td>
</tr>
</tbody>
</table>
These two bits are used to control RAS pre-charge time, RAS active to pre-charge time, refresh to RAS active, refresh to refresh, RASJ active to refresh, and RASJ active to RASJ active time.

0 (0) Selection of RASJ[7]/SRASJ[0] and RASJ[6]/SCASJ[0].
0 : SRASJ[0] and SCASJ[0].
1 : RASJ[7] and RASJ[6].
This bit is used to select the multi-function supported by the RASJ[7]/SRASJ[0] and RASJ[6]/SCASJ[0] pins. When this bit is programmed to be '1', 8 row DRAM configuration is supported. When this bit is programmed to be '0', SDRAM configuration is supported.
Register Index: **5Dh**  
Register Name: **SDRAMCII - Synchronous DRAM Control Register II**  
Default Value: **00h**  
Attribute: **Read/Write**  
Size: **8 bits**

### Bit Number | Bit Function
---|---
7 (0) | Reserved.
6 (0) | SDRAM Speculative Read.  
  0 : Disabled.  
  1 : Enabled.  
  This bit is used to support SDRAM speculative read feature. At the end of T1, M1531B will speculatively read the SDRAM data assuming the memory read cycle is DRAM page hit cycle. If the speculation is not correct (DRAM page miss or non DRAM cycle), M1531B will issue the pre-charge command to reset the SDRAM access after the cycle is decoded correctly (at the end of T2). Since the DRAM address only issues one clock setup time, the feature is suggested to be enabled only when the SDRAM clock is equal or below 60 MHz. In the other condition, this feature should be disabled.
5 (0h) | Reserved
4 (0h) | SDRAM internal Page Hit Detection  
  0 : Disable  
  1 : Enable  
  When this bit is enabled, SDRAM state machine detects the cycle as the page hit during SDRAM bank changing. A ‘1’ is recommended to enhance SDRAM performance.
3-2 (0h) | Reserved
1 (0) | CLKEN[1:0]/PREQJ[4],PGNTJ[4] Select.  
  0 : CLKEN[1:0] Select.  
  This bit is used to select the function supported by the multi-functional pins CLKEN[1:0]/PREQJ[4],PGNTJ[4]. When this bit is programmed as '0', CLKEN[1:0] are selected, SDRAM Self Refresh feature is supported. When this bit is programmed as '1', the fifth PCI master is supported.
0 (0) | JEDEC “2n rule” Restricted.  
  0 : Yes.  
  1 : No. (The Interval Between Two Commands Not Limited to Be Even-numbered.)  
  This bit is used to support TI 2n rule SDRAM, the interval between two commands has to be limited to even-numbers.

Register Index: **5Eh**  
Register Name: **Reserved**  
Default Value: **00h**  
Attribute: **Read Only**  
Size: **8 bits**
Register Index: 5Fh  
Register Name: DRAMHP - DRAM Configuration of Half-Populated Banks  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (0h)</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>5 (0)</td>
<td>Which Half of Row5 (RAS5J) Is Populated</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Lower Dword (MD[31:0])</td>
<td>This bit is valid only if Index-43h bit7 = 1. This bit is used to control Row5 High/Low Dword data swap.</td>
</tr>
<tr>
<td></td>
<td>1: Higher Dword (MD[63:32])</td>
<td></td>
</tr>
</tbody>
</table>

| 4 (0)      | Which Half of Row4 (RAS4J) Is Populated |   |
|            | 0: Lower Dword (MD[31:0]) | This bit is valid only if Index-43h bit6 = 1. This bit is used to control Row4 High/Low Dword data swap. |
|            | 1: Higher Dword (MD[63:32]) | |

| 3 (0)      | Which Half of Row3 (RAS3J) Is Populated |   |
|            | 0: Lower DWord (MD[31:0]) | This bit is valid only if Index-43h bit5 = 1. This bit is used to control Row3 High/Low Dword data swap. |
|            | 1: Higher Dword (MD[63:32]) | |

| 2 (0)      | Which Half of Row2 (RAS2J) Is Populated |   |
|            | 0: Lower Dword (MD[31:0]) | This bit is valid only if Index-43h bit4 = 1. This bit is used to control Row2 High/Low Dword data swap. |
|            | 1: Higher Dword (MD[63:32]) | |

| 1 (0)      | Which Half of Row1 (RAS1J) Is Populated |   |
|            | 0: Lower Dword (MD[31:0]) | This bit is valid only if Index-43h bit3 = 1. This bit is used to control Row1 High/Low Dword data swap. |
|            | 1: Higher Dword (MD[63:32]) | |

| 0 (0)      | Which Half of Row0 (RAS0J) Is Populated |   |
|            | 0: Lower DWord (MD[31:0]) | This bit is valid only if Index-43h bit2 = 1. M1531B supports flexible 32-bit access. This bit is used to control Row0 High/Low Dword data swap. |
|            | 1: Higher Dword (MD[63:32]) | |
Register Index: **60h**
Register Name: **DB0CI - DRAM Row0 Configuration -1**
Default Value: **08h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row0 DRAM Top Address Boundary-1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: **61h**
Register Name: **DB0CII - DRAM Row0 Configuration-2**
Default Value: **40h**
Attribute: **Read/Write**
Size: **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (01)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td>00 : Row0 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.</td>
<td></td>
</tr>
<tr>
<td>01 : Row0 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.</td>
<td></td>
</tr>
<tr>
<td>10 : Row0 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).</td>
<td></td>
</tr>
<tr>
<td>11 : Row0 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).</td>
<td></td>
</tr>
<tr>
<td>These two bits are used to program the DRAM MA used on DRAM Row 0. Please refer to the DRAM MA translation table.</td>
<td></td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row0 DRAM Type.</td>
</tr>
<tr>
<td>00 : Standard Fast-Page Mode DRAM.</td>
<td></td>
</tr>
<tr>
<td>01 : EDO DRAM.</td>
<td></td>
</tr>
<tr>
<td>10 : Reserved.</td>
<td></td>
</tr>
<tr>
<td>11 : Synchronous DRAM.</td>
<td></td>
</tr>
<tr>
<td>These two bits are used to program the DRAM type used on DRAM Row 0.</td>
<td></td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Row0 DRAM Top Address Boundary-2. A31-A28 Address Boundary.</td>
</tr>
<tr>
<td>These four bits are used to combine index-60h to decide the top memory size for DRAM Row 0.</td>
<td></td>
</tr>
</tbody>
</table>

The following types of SDRAMs are supported when bits [7:6] = '00'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx2Mx16</td>
<td>64Mb</td>
<td>13</td>
<td>8</td>
</tr>
<tr>
<td>2Bx4Mx8</td>
<td>64Mb</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>2Bx8Mx4</td>
<td>64Mb</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>2Bx1Mx32</td>
<td>64Mb</td>
<td>12</td>
<td>8</td>
</tr>
</tbody>
</table>

The following types of FPM/EDO DRAMs are supported when bits [7:6] = '01'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>512Kx8</td>
<td>4Mb</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>1Mx4</td>
<td>4Mb</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>1Mx16</td>
<td>16Mb</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>2Mx8</td>
<td>16Mb</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>4Mx4</td>
<td>16Mb</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>4Mx4</td>
<td>16Mb</td>
<td>12</td>
<td>10</td>
</tr>
</tbody>
</table>
The following types of SDRAMs are supported when bits [7:6] = '01'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Bx512Kx16</td>
<td>16Mb</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>2Bx1Mx8</td>
<td>16Mb</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>2Bx2Mx4</td>
<td>16Mb</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>2Bx512Kx64</td>
<td>64Mb</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>2Bx1Mx32</td>
<td>64Mb</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>2Bx2Mx16</td>
<td>64Mb</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

The following types of FPM/EDO DRAMs are supported when bits [7:6] = '10'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mx16</td>
<td>64Mb</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>8Mx8</td>
<td>64Mb</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>16Mx4</td>
<td>64Mb</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>

The following types of SDRAMs are supported when bits [7:6] = '10'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Bx512Kx32</td>
<td>64Mb</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td>4Bx1Mx16</td>
<td>64Mb</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>4Bx2Mx8</td>
<td>64Mb</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

The following types of FPM/EDO DRAMs are supported when bits [7:6] = '11'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Mx16</td>
<td>16Mb</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>2Mx8</td>
<td>16Mb</td>
<td>12</td>
<td>9</td>
</tr>
</tbody>
</table>

The following types of SDRAMs are supported when bits [7:6] = '11'.

<table>
<thead>
<tr>
<th>Memory Organization</th>
<th>Memory Size</th>
<th>Row Address</th>
<th>Column Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Bx1Mx16</td>
<td>64Mb</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>4Bx2Mx8</td>
<td>64Mb</td>
<td>12</td>
<td>9</td>
</tr>
<tr>
<td>4Bx4Mx4</td>
<td>64Mb</td>
<td>12</td>
<td>10</td>
</tr>
</tbody>
</table>
The M1531B supports 8 rows of DRAM, and each of them can be 32-bit or 64-bit wide. DRAM Rowx Configuration register defines populated DRAM type and Top Address Boundary for each row. DB0CI and DB0CII define for Row 0, DB1CI and DB1CII define for Row 1, DB2CI and DB2CII define for Row 2, DB3CI and DB3CII define for Row 3, DB4CI and DB4CII define for Row 4, DB5CI and DB5CII define for Row 5, DB6CI and DB6CII define for Row 6, and DB7CI and DB7CII define for Row 7. Contents of these 8-bit registers represent the boundary address in 1MB granularity and DRAM type populated.

DB0CII[3:0]&DB0CI[7:0] = Total amount of memory in row 0 (Unit: 1MB).

DB0CII[5:4] define different DRAM Type for row 0.

DB0CII[7:6] define different MA Type or unpopulated for row 0.

DB1CII[3:0]&DB1CI[7:0] = Total amount of memory in row 0 + row 1 (Unit: 1MB).

DB1CII[5:4] define different DRAM Type for row 1.

DB1CII[7:6] define different MA Type or unpopulated for row 1.

DB2CII[3:0]&DB2CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 (Unit: 1MB).

DB2CII[5:4] define different DRAM Type for row 2.

DB2CII[7:6] define different MA Type or unpopulated for row 2.

DB3CII[3:0]&DB3CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 (Unit: 1MB).

DB3CII[5:4] define different DRAM Type for row 3.

DB3CII[7:6] define different MA Type or unpopulated for row 3.

DB4CII[3:0]&DB4CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (Unit: 1MB).


DB4CII[7:6] define different MA Type or unpopulated for row 4.

DB5CII[3:0]&DB5CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (Unit: 1MB).

DB5CII[5:4] define different DRAM Type for row 5.

DB5CII[7:6] define different MA Type or unpopulated for row 5.

DB6CII[3:0]&DB6CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 (in 1MB).


DB6CII[7:6] define different MA Type or unpopulated for row 6.

DB7CII[3:0]&DB7CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 + row 7 (in 1MB).

DB7CII[5:4] define different DRAM Type for row 7.
DB7CII[7:6] define different MA Type or unpopulated for row 7.
As an example of a system configuration where 8 physical rows are configured for either single-sided or double-sided SIMMs, the DRAM will be configured like the following figure.

```
<table>
<thead>
<tr>
<th>RAS7J</th>
<th>SIMM-7 Back</th>
<th>SIMM-6 Back</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS6J</td>
<td>SIMM-7 Front</td>
<td>SIMM-6 Front</td>
</tr>
<tr>
<td>RAS5J</td>
<td>SIMM-5 Back</td>
<td>SIMM-4 Back</td>
</tr>
<tr>
<td>RAS4J</td>
<td>SIMM-5 Front</td>
<td>SIMM-4 Front</td>
</tr>
<tr>
<td>RAS3J</td>
<td>SIMM-3 Back</td>
<td>SIMM-2 Back</td>
</tr>
<tr>
<td>RAS2J</td>
<td>SIMM-3 Front</td>
<td>SIMM-2 Front</td>
</tr>
<tr>
<td>RAS1J</td>
<td>SIMM-1 Back</td>
<td>SIMM-0 Back</td>
</tr>
<tr>
<td>RAS0J</td>
<td>SIMM-1 Front</td>
<td>SIMM-0 Front</td>
</tr>
</tbody>
</table>
```

In this configuration, the M1531B will drive two RASJ lines to the SIMM bank. If the single-sided SIMMs are populated, the even RASJ is used and the odd RASJ is not used. If the double-sided SIMMs are populated, both RASJ lines are used.

**Example A**
Two single-sided 1MB X 32 FPM DRAMs (standard MA mapping) are populated at row 0, a total of 8 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

- DB0CI = 08h  DB0CII = 40h
- DB1CI = 08h  DB1CII = 00h
- DB2CI = 08h  DB2CII = 00h
- DB3CI = 08h  DB3CII = 00h
- DB4CI = 08h  DB4CII = 00h
- DB5CI = 08h  DB5CII = 00h
- DB6CI = 08h  DB6CII = 00h
- DB7CI = 08h  DB7CII = 00h
Example B
Four single-sided 1MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 0 and row 2, a
total of 16 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 08h    DB0CII = D0h
DB1CI = 08h    DB1CII = 00h
DB2CI = 10h    DB2CII = D0h
DB3CI = 10h    DB3CII = 00h
DB4CI = 10h    DB4CII = 00h
DB5CI = 10h    DB5CII = 00h
DB6CI = 10h    DB6CII = 00h
DB7CI = 10h    DB7CII = 00h

Example C
Two double-sided 2MB X 32 FPM DRAMs (standard MA mapping) are populated on row 4, row 5, row
6, and row 7, a total of 32 MB of DRAM. The DBxCI and DBxCII registers should be programmed as
follows:

DB0CI = 00h    DB0CII = 00h
DB1CI = 00h    DB1CII = 00h
DB2CI = 00h    DB2CII = 00h
DB3CI = 00h    DB3CII = 00h
DB4CI = 08h    DB4CII = 40h
DB5CI = 10h    DB5CII = 40h
DB6CI = 18h    DB6CII = 40h
DB7CI = 20h    DB7CII = 40h

Example D
One double-sided 2MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 2 and row 3,
and one double-sided 8MB X 32 FPM DRAMs (64Mb MA mapping) are populated on row 6 and row 7,
a total of 80 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h    DB0CII = 00h
DB1CI = 00h    DB1CII = 00h
DB2CI = 08h    DB2CII = D0h
DB3CI = 10h    DB3CII = D0h
DB4CI = 10h    DB4CII = 00h
DB5CI = 10h    DB5CII = 00h
DB6CI = 30h    DB6CII = 80h
DB7CI = 50h    DB7CII = 80h
Register Index: 62h
Register Name: DB1CI - DRAM Row1 Configuration -1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row1 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: 63h
Register Name: DB1CII - DRAM Row1 Configuration-2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (00h)  | DRAM MA Definition.  
00 : Row1 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.  
01 : Row1 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.  
10 : Row1 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).  
11 : Row1 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).  
These two bits are used to program the DRAM MA used on DRAM Row 1. Please refer to the DRAM MA translation table. |
| 5-4 (00h)  | Row1 DRAM Type.  
00 : Standard Fast-Page Mode DRAM.  
01 : EDO DRAM.  
10 : Reserved.  
11 : Synchronous DRAM.  
These two bits are used to program the DRAM type used on DRAM Row 1. |
| 3-0 (00h)  | Row1 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-62h to decide top memory size for DRAM Row1. |
### Register: DB2CI - DRAM Row2 Configuration-1

**Register Index:** 64h  
**Register Name:** DB2CI - DRAM Row2 Configuration-1  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row2 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

### Register: DB2CII - DRAM Row2 Configuration-2

**Register Index:** 65h  
**Register Name:** DB2CII - DRAM Row2 Configuration-2  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7-6 (0h)   | DRAM MA Definition.  
|            | 00 : Row2 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.  
|            | 01 : Row2 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.  
|            | 10 : Row2 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).  
|            | 11 : Row2 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).  
|            | These two bits are used to program the DRAM MA used on DRAM Row 2. Please refer to the DRAM MA translation table. |
| 5-4 (0h)   | Row2 DRAM Type.  
|            | 00 : Standard Fast-Page Mode DRAM.  
|            | 01 : EDO DRAM.  
|            | 10 : Reserved.  
|            | 11 : Synchronous DRAM.  
|            | These two bits are used to program the DRAM type used on DRAM Row 2. |
| 3-0 (0h)   | Row2 DRAM Top Address Boundary-2. A31-A28 Address Boundary.  
|            | These four bits are used to combine index-64h to decide top memory size for DRAM Row2. |
## Register 66h: DB3CI - DRAM Row3 Configuration-1
- **Default Value:** 00h
- **Attribute:** Read/Write
- **Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row3 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
<td></td>
</tr>
</tbody>
</table>

## Register 67h: DB3CII - DRAM Row3 Configuration-2
- **Default Value:** 00h
- **Attribute:** Read/Write
- **Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6(0h)</td>
<td>DRAM MA Definition.</td>
<td></td>
</tr>
<tr>
<td>00 : Row3 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 : Row3 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 : Row3 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 : Row3 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

These two bits are used to program the DRAM MA used on DRAM Row 3. Please refer to the DRAM MA translation table.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-4(0h)</td>
<td>Row3 DRAM Type.</td>
<td></td>
</tr>
<tr>
<td>00 : Standard Fast-Page Mode DRAM.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 : EDO DRAM.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 : Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 : Synchronous DRAM.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

These two bits are used to program the DRAM type used on DRAM Row 3.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0(0h)</td>
<td>Row3 DRAM Top Address Boundary - 2. A31-A28 Address Boundary.</td>
<td></td>
</tr>
</tbody>
</table>

These four bits are used to combine index-66h to decide top memory size for DRAM Row3.
Register Index : 68h
Register Name : DB4CI - DRAM Row4 Configuration-1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row4 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index : 69h
Register Name : DB4CII - DRAM Row4 Configuration-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (0h)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td>00</td>
<td>Row4 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.</td>
</tr>
<tr>
<td>01</td>
<td>Row4 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.</td>
</tr>
<tr>
<td>10</td>
<td>Row4 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected.</td>
</tr>
<tr>
<td>11</td>
<td>Row4 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected.</td>
</tr>
</tbody>
</table>

These two bits are used to program the DRAM MA used on DRAM Row 4. Please refer to the DRAM MA translation table.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-4 (0h)</td>
<td>Row4 DRAM Type.</td>
</tr>
<tr>
<td>00</td>
<td>Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td>01</td>
<td>EDO DRAM.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved.</td>
</tr>
<tr>
<td>11</td>
<td>Synchronous DRAM.</td>
</tr>
</tbody>
</table>

These two bits are used to program the DRAM type used on DRAM Row 4.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0 (0h)</td>
<td>Row4 DRAM Top Address Boundary - 2. A31-A28 Address Boundary.</td>
</tr>
</tbody>
</table>

These four bits are used to combine index-68h to decide top memory size for DRAM Row4.
Register Index: 6Ah
Register Name: DB5CI - DRAM Row5 Configuration-1
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row5 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index: 6Bh
Register Name: DB5CII - DRAM Row0 Configuration-2
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (0h)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>00: Row5 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.</td>
</tr>
<tr>
<td></td>
<td>01: Row5 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.</td>
</tr>
<tr>
<td></td>
<td>10: Row5 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).</td>
</tr>
<tr>
<td></td>
<td>11: Row5 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row5 DRAM Type.</td>
</tr>
<tr>
<td></td>
<td>00: Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td></td>
<td>01: EDO DRAM.</td>
</tr>
<tr>
<td></td>
<td>10: Reserved.</td>
</tr>
<tr>
<td></td>
<td>11: Synchronous DRAM.</td>
</tr>
<tr>
<td>3-0(0h)</td>
<td>Row5 DRAM Top Address Boundary - 2. A31-A28 Address Boundary.</td>
</tr>
<tr>
<td></td>
<td>These four bits are used to combined index-6Ah to decide top memory size for DRAM Row5.</td>
</tr>
</tbody>
</table>
Register Index : 6Ch
Register Name : DB6C1 - DRAM Row6 Configuration-1
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0(00h)</td>
<td>Row6 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

Register Index : 6Dh
Register Name : DB6C2I - DRAM Row6 Configuration-2
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (0h)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td></td>
<td>00 : Row6 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.</td>
</tr>
<tr>
<td></td>
<td>01 : Row6 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.</td>
</tr>
<tr>
<td></td>
<td>10 : Row6 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).</td>
</tr>
<tr>
<td></td>
<td>11 : Row6 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the DRAM MA used on DRAM Row 6. Please refer to the DRAM MA translation table.</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row6 DRAM Type.</td>
</tr>
<tr>
<td></td>
<td>00 : Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td></td>
<td>01 : EDO DRAM.</td>
</tr>
<tr>
<td></td>
<td>10 : Reserved.</td>
</tr>
<tr>
<td></td>
<td>11 : Synchronous DRAM.</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to program the DRAM type used on DRAM Row 6.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Row6 DRAM Top Address Boundary-2. A31-A28 Address Boundary.</td>
</tr>
<tr>
<td></td>
<td>These four bits are used to combine index-6Ch to decide top memory size for DRAM Row6.</td>
</tr>
</tbody>
</table>
### Register Index: 6Eh
**Register Name:** DB7CI - DRAM Row7 Configuration-1  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0 (00h)</td>
<td>Row7 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.</td>
</tr>
</tbody>
</table>

### Register Index: 6Fh
**Register Name:** DB7CII - DRAM Row7 Configuration-2  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (0h)</td>
<td>DRAM MA Definition.</td>
</tr>
<tr>
<td>00</td>
<td>Row7 DRAM Disable in FPM/EDO or SDRAM when 64Mbits 2 bank is selected.</td>
</tr>
<tr>
<td>01</td>
<td>Row7 DRAM uses standard MA Mapping in FPM/EDO or SDRAM when 16Mbits 2 bank is selected.</td>
</tr>
<tr>
<td>10</td>
<td>Row7 DRAM uses 64M technology MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[12:11] are used as bank selection).</td>
</tr>
<tr>
<td>11</td>
<td>Row7 DRAM uses 1Mx16 MA Mapping in FPM/EDO or SDRAM when 64Mbits 4 bank is selected. (MA[13:12] are used as bank selection).</td>
</tr>
<tr>
<td>5-4 (0h)</td>
<td>Row7 DRAM Type.</td>
</tr>
<tr>
<td>00</td>
<td>Standard Fast-Page Mode DRAM.</td>
</tr>
<tr>
<td>01</td>
<td>EDO DRAM.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved.</td>
</tr>
<tr>
<td>11</td>
<td>Synchronous DRAM.</td>
</tr>
<tr>
<td>3-0 (0h)</td>
<td>Row7 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-6Eh to decide top memory size for DRAM Row7.</td>
</tr>
</tbody>
</table>
Register Index : 71h-70h
Register Name : PM2BADR - Base Address of ACPI PM2_CNTL Port
Default Value : 0022h
Attribute : Read/Write
Size : 16 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-0(00h)</td>
<td>Base Address of ACPI PM2_CNTL Port. This 16-bit register is programmed as the I/O base address of ACPI PM2_CNTL Port. The default value is 0022h, and can be programmed by Software to move the base address of ACPI PM2_CNTL Port.</td>
</tr>
</tbody>
</table>

Register Index : 72h
Register Name : PM2C - ACPI PM2_CNTL Function.
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4 (0h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>3 (0)</td>
<td>Sub-Vendor &amp; Sub-Device ID Registers Programming.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>This bit is used to lock the Sub-Vendor &amp; Sub-Device ID register programming. When this bit is enabled, Software can write the data to the Sub-Vendor &amp; Sub-Device ID registers. When this bit is disabled, the Sub-Vendor &amp; Sub-Device ID registers become Read Only.</td>
</tr>
<tr>
<td>2 (0)</td>
<td>Delay for I/O Trap Feature.</td>
</tr>
<tr>
<td></td>
<td>0 : Disable.</td>
</tr>
<tr>
<td></td>
<td>1 : Enable.</td>
</tr>
<tr>
<td></td>
<td>M1531B will delay all the PCI I/O cycle by one clock when this bit is enabled. The BRDYJ to CPU will delay one clock compared to normal I/O access.</td>
</tr>
<tr>
<td>1-0 (0h)</td>
<td>ACPI PM2_CNTL Function.</td>
</tr>
<tr>
<td></td>
<td>00 : Disable.</td>
</tr>
<tr>
<td></td>
<td>01 : Enable, Pass the ACPI PM2_CNTL Port Access to PCI Bus.</td>
</tr>
<tr>
<td></td>
<td>10 : Enable, Not Pass the ACPI PM2_CNTL Port Access to PCI Bus.</td>
</tr>
<tr>
<td></td>
<td>11 : Reserved.</td>
</tr>
<tr>
<td></td>
<td>M1531B has implemented the ACPI PM2_CNTL I/O Port, and the address is defined by Index 71h-70h. When these two bits are programmed to be '00', M1531B will disable the ACPI PM2_CNTL I/O Port decode, and pass the I/O cycle to PCI bus. When these two bits are programmed to be '01', M1531B will snoop the ACPI PM2_CNTL I/O Port write data, and pass the I/O cycle to PCI bus. In this setting, M1531B just do the snoop write, and all the cycle will be terminated by M1533/M1543. When these two bits are programmed to be '10', M1531B will terminate the ACPI PM2_CNTL I/O Port access, and will not pass the I/O cycle to PCI bus.</td>
</tr>
</tbody>
</table>
Register Index : **73h**  
Register Name : **Reserved**  
Default Value : **00h**  
Attribute : **Read Only**

Register Index : **74h**  
Register Name : **RFQU - Refresh Queue Control**  
Default Value : **00h**  
Attribute : **Read/Write**  
Size : **8 bits**

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6 (00h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
| 5 (0)      | SDRAM Speculative read.  
            | 0 : Disable.  
            | 1 : Enable.   |
|            | When this bit is enabled, SDRAM will drive the read command before the cycle is fully decoded. If the CPU bus is running at 66 Mhz or below, a ‘1’ is recommended. Otherwise, a ‘0’ is recommended. |
| 4 (0)      | Reserved.   |
| 3 (0)      | Fast L2 Write back  
            | 0 : Disable.  
            | 1 : Enable.   |
|            | When this bit is enabled, M1531B will perform a fast L2 Write back cycle. A ‘1’ is recommended for best system performance. |
| 2 (0)      | Reserved.   |
| 1 (0)      | PCI to DRAM Speculative Read.  
            | 0 : Disable.  
            | 1 : Enable.   |
|            | This bit is used to control the PCI to DRAM speculative read. When this bit is enabled, M1531B will read the DRAM data before L1 & L2 snoop result is ready. If the snoop is dirty hit to L1 or L2, the speculative read data will be dropped and get the data from L1 or L2. If the snoop is not dirty hit to L1 or L2, the speculative read data is available. This feature is used to gain the PCI master read performance. This bit is suggested to be enabled during normal operation. |
| 0 (0)      | Refresh Queue.  
            | 0 : Disable.  
            | 1 : Enable.   |
|            | This bit is used to control the DRAM Refresh Queue. M1531B has implemented 4 DRAM Refresh Queue. When DRAM refresh request collides with DRAM bus activity, this DRAM refresh will be delayed until the DRAM bus activity is finished. If the DRAM Refresh Queues are full, the DRAM refresh request becomes the top priority, and the other DRAM bus activity will be delayed. |

Register Index : **75h**  
Register Name : **Reserved**  
Default Value : **00h**  
Attribute : **Read Only**
Register Index: 76h  
Register Name: POD - Programmable Output Driving Strength  
Default Value: 00h  
Attribute: Read/Write  
Size: 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | MWEJ Driving Capability Select.  
            | 0 : 12 mA.  
            | 1 : 24 mA.  
            | This bit controls the strength of the output buffers driving the MWEJ pins. |
| 6 (0)      | MAA[1:0]/MAB[1:0] Driving Capability Select.  
            | 0 : 12 mA.  
            | 1 : 24 mA.  
            | This bit controls the strength of the output buffers driving the MAA[1:0] and MAB[1:0] pins. |
| 5 (0)      | MA[11:2] Driving Capability Select.  
            | 0 : 12 mA.  
            | 1 : 24 mA.  
            | This bit controls the strength of the output buffers driving the MA[11:2] pins. |
| 4 (0)      | CASJ[7:0] Driving Capability Select.  
            | 0 : 12 mA.  
            | 1 : 24 mA.  
            | This bit controls the strength of the output buffers driving the CASJ[7:0] pins. |
| 3 (0)      | RASJ[5:0] Driving Capability Select.  
            | 0 : 12 mA.  
            | 1 : 24 mA.  
            | This bit controls the strength of the output buffers driving the RASJ[5:0] pins. |
| 2 (0)      | RASJ[7:6]/SRASJ[1:0], SCASJ[1:0] Driving Capability Select.  
            | 0 : 12 mA.  
            | 1 : 24 mA.  
            | This bit controls the strength of the output buffers driving the RASJ[7:6]/SRASJ[1:0], SCASJ[1:0] pins. |
| 1 (0)      | MD[63:0] and MPD[7:0] Driving Capability Select.  
            | 0 : 8 mA.  
            | 1 : 6 mA.  
            | This bit controls the strength of the output buffers driving the MD[63:0] and MPD[7:0] pins. |
| 0 (0)      | HD[63:0] Driving Capability Select.  
            | 0 : 8 mA.  
            | 1 : 6 mA.  
            | This bit controls the strength of the output buffers driving the HD[63:0] pins. |
## Register Name: SUSC - DRAM Suspend Control Register

**Register Index:** 77h  
**Default Value:** 00h  
**Attribute:** Read/Write  
**Size:** 8 bits

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
</table>
| 7 (0)      | Memory Data Bus Clock Control.  
|            | 0 : Disable Gated Clock.  
|            | 1 : Enable Gated Clock.  
|            | This bit is used to control the internal clock regarding the Memory Data Bus. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no Memory Data Bus activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power. |
| 6 (0)      | DRAM & Cache Controller Clock Control.  
|            | 0 : Disable Gated Clock.  
|            | 1 : Enable Gated Clock.  
|            | This bit is used to control the internal clock regarding the DRAM & Cache Controller. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no Host Bus activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power. |
| 5 (0)      | Host to PCI Interface Logic Clock Control.  
|            | 0 : Disable Gated Clock.  
|            | 1 : Enable Gated Clock.  
|            | This bit is used to control the internal clock regarding the Host to PCI Interface Logic. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no Host to PCI activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power. |
| 4 (0)      | PCI to Host Buffer Clock Control.  
|            | 0 : Disable Gated Clock.  
|            | 1 : Enable Gated Clock.  
|            | This bit is used to control the internal clock regarding the PCI to Host Buffer. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1531B will automatically stop the internal clock when there is no PCI master activity. This bit is suggested to be '0' in desktop application; to be '1' in notebook application to save more power. |
| 3 (0)      | DRAM Suspend Self Refresh Mode.  
|            | 0 : Disable.  
|            | 1 : Enable.  
|            | This bit is used to support EDO Self Refresh mode during DRAM suspend. When this bit is enabled, M1531B will issue EDO Self Refresh timing during DRAM Suspend. |
| 2-1 (00)   | DRAM Suspend Refresh Period.  
|            | 00 : 15 us.  
|            | 01 : 30 us.  
|            | 10 : 60 us.  
|            | 11 : 120 us.  
|            | These 2 bits define the DRAM suspend refresh period. |
| 0 (0)      | CLKRUNJ/SERRJ Function Select.  
|            | 0 : SERRJ.  
|            | 1 : CLKRUNJ.  
|            | This bit is used to define the CLKRUNJ/SERRJ pin function. When this bit is programmed to '0', SERRJ function is selected. In this configuration, M1531B can support DRAM ECC/PARITY and the PCI Parity check error report. When this bit is programmed to '1', CLKRUNJ function is selected. M1531B can support Mobile PCI Specification 2.0 CLKRUNJ function through this configuration. |
Register Index: 7Fh-78h
Register Name: Reserved
Default Value: 00h
Attribute: Read Only

Register Index: 80h
Default Value: 00h
Attribute: Read/Write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>MA output LATCH</td>
</tr>
<tr>
<td></td>
<td>0: MA latch,</td>
</tr>
<tr>
<td></td>
<td>1: MA don't latch.</td>
</tr>
<tr>
<td></td>
<td>M1531B has two ways to drive MA bus. When this bit is reset as '0', M1531B will drive MA bus through a latch to avoid MA bus glitch since MA bus is decoded directly from CPU address or write buffer address. In this mode, M1531B will drive MA bus at the beginning of T3. When this bit is set as '1', M1531B will drive MA bus directly through the decoding circuit. In this mode, MA will drive earlier. A '1' is recommended in normal operation.</td>
</tr>
<tr>
<td>6-3 (0h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>2</td>
<td>RASJ asserted point in ROW Miss Cycle</td>
</tr>
<tr>
<td></td>
<td>0: T3 End</td>
</tr>
<tr>
<td></td>
<td>1: T2 End</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the RASJ assertion point in Row miss cycle. A '1' recommended in normal operation for best system performance</td>
</tr>
<tr>
<td>1-0 (0h)</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Register Index: 81h
Default Value: 00h
Attribute: Read/Write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 (0)</td>
<td>DRAM Pipe Read falling change MA for next line</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, M1531B will change MA early half clock in DRAM. A '1' is recommended in normal operation for best reliability.</td>
</tr>
<tr>
<td>6-1 (00h)</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0</td>
<td>Refresh function</td>
</tr>
<tr>
<td></td>
<td>0: Enable</td>
</tr>
<tr>
<td></td>
<td>1: Disable</td>
</tr>
</tbody>
</table>

Register Index: 83h
Default Value: 00h
Attribute: Read/Write

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 (0)</td>
<td>SDRAM command drive 2T in high frequency bus</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
</tr>
<tr>
<td></td>
<td>When this bit is enabled, SDRAM command will drive 2T instead of 1T in high SDRAM bus frequency. If SDRAM bus is running at 66 Mhz or below, a '0' is recommended. Otherwise, a '1' is recommended.</td>
</tr>
</tbody>
</table>

Register Index: FFh-84h
Register Name: Reserved
Default Value: 00h
Attribute: Read Only
### III. ACPI PM2_CNTL I/O Port

Register Name: **PM2_CNTL** - ACPI PM2_CNTL I/O Port  
I/O Address:  **0000h - FFFFh Movable**  
Default Value: **00h**  
Attribute: **Read/Write**  
Size: This register must be 8-bit I/O access.

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Bit Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-1(00h)</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 0 (0)      | PCI Master Arbiter Function.  
            0 : Enable.  
            1 : Disable.  
            This bit is used to control the PCI Master Arbiter Function. When this bit is set to be ‘1’, the M1531B internal PCI master arbiter will be disabled, and the M1531B on behalf of the CPU host is the only one master in the system. In normal operation, the bit must be set to ‘0’. |
Section 5 : Hardware and Software Programming Guide

5.1 Hardware Setup Table :

The M1531B will strobe the hardware setting value in the respective registers when the RSTJ goes inactive. BIOS can utilize the register value to save the software programming time to detect L2 type, size, and the bus frequency. For notebook applications, it is recommended to use software programming to reduce power consumption since the pull-up and pull-down resistors will continuously consume system power. If the BIOS wants to utilize the hardware setting value, the system board designer must make sure the strobing value is identical to their definition. Otherwise, the software programming must be used to detect the hardware configuration.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Description</th>
<th>Pull-up</th>
<th>Pull-down</th>
<th>Register</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>HA[31..27]</td>
<td>Cache module detect bits</td>
<td>—</td>
<td>—</td>
<td>Index-52h bits[7:3]</td>
<td>(1)</td>
</tr>
<tr>
<td>HA[26..25]</td>
<td>Indicate host frequency</td>
<td>—</td>
<td>—</td>
<td>Index-52h bits[2:1]</td>
<td>(2)</td>
</tr>
<tr>
<td>HA24</td>
<td>L2 cache bank select</td>
<td>1-bank</td>
<td>2-bank</td>
<td>Index-41h bit[7]</td>
<td></td>
</tr>
<tr>
<td>HA[22..21]</td>
<td>Cache size detect</td>
<td>—</td>
<td>—</td>
<td>Index-41h bits[2:1]</td>
<td>(3)</td>
</tr>
</tbody>
</table>

**Note**:

(1) Please refer to cache module specification for detailed setting or the system designer can define their own meaning.

(2) | HA26 | HA25 | Host frequency |
---|------|------|----------------|
  0  | 0    | 60 MHz |
  0  | 1    | 66 MHz |
  1  | 0    | 75 MHz |
  1  | 1    | 83 MHz |

(3) | HA22 | HA21 | Cache size |
---|------|------|-----------|
  0  | 0    | None |
  0  | 1    | 256KB |
  1  | 0    | 512KB |
  1  | 1    | 1MB   |
5.2 DRAM Detection Flow:

The “DRAM Detection Flow” is a row-by-row basis algorithm. The flow starts from Row 0 and then up to the final row depending on the motherboard configuration. The “DRAM Type Detection” is used to detect the DRAM type including Fast Page Mode (FPM) DRAM, EDO and SDRAM. The “32-bit or 64-bit DRAM Row Detection” is used to detect the 32-bit or 64-bit DRAM Population on this Row. The M1531B supports 32-bit DRAM Population, the MA table will be different. The 32-bit or 64-bit MA Mapping Detection is used to detect the MA mapping as the standard or 64MB or 1Mx16 or 2M x8 (12x9). The “Autosizing” is used to detect the Row size. The M1531B can support from 2MB to 128MB per Row.
5.2.1 DRAM Type Detection and 32-bit vs. 64-bit Row Detect:

```
Start

Disable L1 and L2
Index 42h bit [0] = '0'
Index 43h bit [0] = '0'

Set DRAM size to 128M
Set DRAM type to Fast Page Mode
Set MA to Standard MA mapping
Set current Row as 64-bit DRAM Population

Set DRAM size to 128M
Set DRAM type to Fast Page Mode
Set MA to Standard MA mapping
Set current Row as 64-bit DRAM Population

Set Proper EDO Detection access timer
(Index 44h bits [7:6])

Enable EDO Detection Mode
Index 44h bit [5] = '1'

MDW; BEJ:=DW; HA:=TM+0h, Dat:=D0
MDW; BEJ:=DW; HA:=TM+4h, Dat:=D1
MDR; BEJ:=DW; HA:=TM+0h, Dat:=Q0
MDR; BEJ:=DW; HA:=TM+4h, Dat:=Q1

Is Q0 =D0 ?
and Q1 =D1 ?

Yes

64-bit EDO DRAM Population
A

No

Is Q0 =D0 ?
and Q1 ≠D1 ?

Yes

Low Dword 32-bit EDO DRAM Population
A

No

Is Q0 ≠D0 ?
and Q1 =D1 ?

Yes

High Dword 32-bit EDO DRAM Population
A

No

Disable EDO Detection Mode
Index 44h bit [5] = '0'

MDW; BEJ:=DW; HA:=TM+0h, Dat:=D0
MDW; BEJ:=DW; HA:=TM+4h, Dat:=D1
MDR; BEJ:=DW; HA:=TM+0h, Dat:=Q0
MDR; BEJ:=DW; HA:=TM+4h, Dat:=Q1
```

TM: Total Memory Size of the Previous Row

```
B
```
Is Q0 =D0 ?
and Q1 =D1 ?
Yes
64-bit FPM DRAM Population
No
Is Q0 =D0 ?
and Q1 ≠D1 ?
Yes
Low Dword 32-bit FPM DRAM Population
No
Is Q0 ≠D0 ?
and Q1 =D1 ?
Yes
High Dword 32-bit FPM DRAM Population
No
SDRAM Initialization
### SDRAM Initialization

1. **Set DRAM as SDRAM**
   - Index: 60h - 6Fh

2. **NOP**
   - wait for 200 µs

3. **Precharge both banks**
   - Index: 5Ch, bits[7:5] = '010'
   - MDR, BEJ=DW, HA=0h

4. **8 CBR refresh cycles**
   - Index: 5Ch, bits[7:5] = '100'
   - MDR, BEJ=DW, HA=0h
   - HA=100h for burst length=4, interleave mode, CAS latency =3
   - HA=150h for burst length=4, interleave mode, CAS latency =2
   - HA=190h for burst length=4, linear mode, CAS latency =3
   - HA=110h for burst length=4, linear mode, CAS latency =2

5. **Set Mode Register**
   - Index: 5Ch, bits[7:5] = '011'
   - MDR, BEJ=DW, HA=0h

6. **2 CBR refresh cycles**
   - Index: 5Ch, bits[7:5] = '100'
   - MDR, BEJ=DW, HA=0h

7. **Issue a write sequence followed by a Read sequence**

8. **Data read matches the write data?**
   - Yes: SDRAM population
   - No: Bank empty or DRAM error

9. **Bank empty or DRAM error**
   - Set the correct DRAM type & 32-bit vs. 64-bit DRAM population
   - Index: 60h-6Fh
   - Index: 43h, 5Fh

10. **Exit**
5.2.2 32-bit MA Mapping Detection

Set current bank to be 64Mbits MA mapping

Is Q=D1?
Yes
No

Is Q=D2 or Q=D3 or Q=D5?
Yes
No

Is Q=D4?
Yes
No

DRAM error

Set the correct MA mapping (Index 60h-6Fh)

<table>
<thead>
<tr>
<th>Din</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>D5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MA</td>
<td>Column</td>
<td>MA</td>
<td>Column</td>
<td>MA</td>
</tr>
<tr>
<td>MA Row</td>
<td>800</td>
<td>000</td>
<td>800</td>
<td>000</td>
<td>C00</td>
</tr>
<tr>
<td>Column</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>64Mb 12x12 Row</td>
<td>800</td>
<td>000</td>
<td>800</td>
<td>000</td>
<td>C00</td>
</tr>
<tr>
<td>Column</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>12x11 Row</td>
<td>800</td>
<td>000</td>
<td>800</td>
<td>000</td>
<td>C00</td>
</tr>
<tr>
<td>Column</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>11x11 Row</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>400</td>
</tr>
<tr>
<td>Column</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>STD 12x10 Row</td>
<td>800</td>
<td>000</td>
<td>800</td>
<td>000</td>
<td>C00</td>
</tr>
<tr>
<td>Column</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>11x11 Row</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>400</td>
</tr>
<tr>
<td>Column</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>11x10 Row</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>400</td>
</tr>
<tr>
<td>Column</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>10x10 Row</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>400</td>
</tr>
<tr>
<td>Column</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>10x9 Row</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>400</td>
</tr>
<tr>
<td>Column</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>1Mx16 12x8 Row</td>
<td>800</td>
<td>000</td>
<td>800</td>
<td>000</td>
<td>C00</td>
</tr>
<tr>
<td>Column</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
</tr>
<tr>
<td>2Mx8 12x9 Row</td>
<td>800</td>
<td>000</td>
<td>800</td>
<td>000</td>
<td>C00</td>
</tr>
<tr>
<td>Column</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>
32-bit bank DRAM Address Translation Table

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A23/A24</td>
<td>A22</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
<tr>
<td>Column</td>
<td>A25</td>
<td>A23</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
</tbody>
</table>

Row MA[11]: if 64Mbits DRAM is not populated, then A23 is driven; if 64Mbits DRAM is populated, then A24 is driven

32-bit Bank 1M x 16, 2M x 8 DRAM Address Translation Table

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A10</td>
<td>A21</td>
<td>A11</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
<tr>
<td>Column</td>
<td>A22</td>
<td>A23</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
</tbody>
</table>

Address Size = 12 x 8, 12 x 9

5.2.3 64-bit MA Mapping Detection

![Diagram of 64-bit MA mapping detection process]

Set current bank to be 64Mbits MA mapping

- Is Q=D1?
  - Yes: 64Mbits MA mapping
  - No:
    - Is Q=D2 or Q=D3 or Q=D5?
      - Yes: Standard MA mapping
      - No:
        - Is Q=D4?
          - Yes: 1M x 16 MA mapping
          - No: 2M x 8 (12x9) MA mapping
    - DRAM error

Set the correct MA mapping (Index 60h-6Fh)

Exit
## M1531B: Memory, Cache and Buffer Controller

### Normal DRAM Address Translation Table

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A24/25</td>
<td>A23</td>
<td>A21</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
<tr>
<td>Column</td>
<td>A26</td>
<td>A24</td>
<td>A22</td>
<td>A11</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
</tr>
</tbody>
</table>

Row MA[11]: If 64Mbits DRAM is not populated, then A24 is driven; if 64Mbits DRAM is populated, then A25 is driven

### 1M x 16, 2M x 8 DRAM Address Translation Table

Specific DRAM Address Translation Table for Asymmetric 1M x 16

<table>
<thead>
<tr>
<th>MA[11:0]</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row</td>
<td>A22</td>
<td>A21</td>
<td>A11</td>
<td>A20</td>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
</tr>
<tr>
<td>Column</td>
<td>A23</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
</tr>
</tbody>
</table>

Address Size = 12 x 8, 12 x 9
5.2.4 Synchronous DRAM MA Mapping and Bank Select Detection

SDRAM MA mapping Detect

Set current bank to be 64Mbits MA mapping with bank select MA[13:12]
Set current bank size to be 128MB
Enable SDRAM MA detection
Write Dword D1 to address HA[31:0] = x’00000000’
Write Dword D2 to address HA[31:0] = x’00800000’
Write Dword D3 to address HA[31:0] = x’01000000’
Read Data Q1 from address HA[31:0]= x’00800000’
Read Data Q2 from address HA[31:0]= x’00000000’

Is Q1=D3 and Q2=D1?
Yes → 64Mb MA Bksel : MA[13]
No

Is Q1=D3 and Q2=D2?
No

Is Q1=D2 and Q2=D2?
Yes → 64 Mb MA Bksel : MA[12:11]
No

Is Q1=D2 and Q2=D1?
Yes → 64Mb MA Bksel : MA[13:12]
No → DRAM error
## Data Sheet

### M1531B : Memory, Cache and Buffer Controller

#### 64Mbits (2bank, 4bank)

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>MA[13:6]</td>
<td>0000-0000</td>
<td>1000-0000</td>
<td>0100-0000</td>
<td>1000-0000</td>
<td>0000-0000</td>
</tr>
<tr>
<td>64Mb 13x10</td>
<td>0000-0000</td>
<td>0010-0000</td>
<td>0100-0000</td>
<td>xxxxxxxx</td>
<td>D3</td>
</tr>
<tr>
<td>13x9</td>
<td>0000-0000</td>
<td>0010-0000</td>
<td>0100-0000</td>
<td>xxxxxxxx</td>
<td>D3</td>
</tr>
<tr>
<td>13x8</td>
<td>0000-0000</td>
<td>0010-0000</td>
<td>0100-0000</td>
<td>xxxxxxxx</td>
<td>D3</td>
</tr>
</tbody>
</table>

#### 12x8

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>12x8</td>
<td>0000-0000</td>
<td>0010-0000</td>
<td>0010-0000</td>
<td>xxxxxxxx</td>
<td>D3</td>
</tr>
</tbody>
</table>

#### 11x10

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>11x10</td>
<td>x000-0000</td>
<td>x000-0000</td>
<td>x010-0000</td>
<td>xxxxxxxx</td>
<td>D2</td>
</tr>
</tbody>
</table>

#### 11x9

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>11x9</td>
<td>x000-0000</td>
<td>x000-0000</td>
<td>x010-0000</td>
<td>xxxxxxxx</td>
<td>D2</td>
</tr>
</tbody>
</table>

#### 11x8

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>11x8</td>
<td>x000-0000</td>
<td>x000-0000</td>
<td>x010-0000</td>
<td>xxxxxxxx</td>
<td>D2</td>
</tr>
</tbody>
</table>

#### 16Mb

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>16Mb 11x10</td>
<td>xx00-0000</td>
<td>xx00-0000</td>
<td>xx00-0000</td>
<td>xxxxxxxx</td>
<td>D3</td>
</tr>
</tbody>
</table>

#### 64Mbits (4bank)

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>MA[11:0]</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>Row</td>
<td>A23</td>
<td>A24</td>
<td>A11</td>
<td>A22</td>
<td>A21</td>
</tr>
</tbody>
</table>

#### 16Mbits (2bank); 64Mbits (2bank)

<table>
<thead>
<tr>
<th>Data</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>MDW</td>
<td>MDW</td>
<td>MDW</td>
<td>MDR</td>
<td>Dout</td>
</tr>
<tr>
<td>MA[11:0]</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>Row</td>
<td>X</td>
<td>A23</td>
<td>A11</td>
<td>A22</td>
<td>A21</td>
</tr>
</tbody>
</table>

---

**Acer Labs:** 7F, 115 Tung Hsing Street, Taipei 110, Taiwan, R.O.C.  
**Tel:** 886-2-762-8800  
**Fax:** 886-2-762-6060
5.2.5 DRAM Autosizing

```
AUTOSIZING

MDW; BEJ := QW; HA[26] := '1'; Dat := D1;
MDW; BEJ := QW; HA[26] := '0'; Dat := D2;
MDR; BEJ := QW; HA[26] := '1'; HD = Q;

Is Q=D1? Yes → 128 MB

MDW; BEJ := QW; HA[25] := '1'; Dat := D1;
MDW; BEJ := QW; HA[25] := '0'; Dat := D2;
MDR; BEJ := QW; HA[25] := '1'; HD = Q;

Is Q=D1? Yes → 64 MB

MDW; BEJ := DW; HA[24] := '1'; Dat := D1;
MDW; BEJ := DW; HA[24] := '0'; Dat := D2;
MDR; BEJ := DW; HA[24] := '1'; HD = Q;

Is Q=D1? Yes → 32 MB

MDW; BEJ := DW; HA[23] := '1'; Dat := D1;
MDW; BEJ := DW; HA[23] := '0'; Dat := D2;
MDR; BEJ := DW; HA[23] := '1'; HD = Q;

Is Q=D1? Yes → 16 MB

MDW; BEJ := DW; HA[22] := '1'; Dat := D1;
MDW; BEJ := DW; HA[22] := '0'; Dat := D2;
MDR; BEJ := DW; HA[22] := '1'; HD = Q;

Is Q=D1? Yes → Below 16MB

```

Is current bank 32-bit populated?

Yes

Is Q=D1?

Yes

2 MB

No

DRAM error

Set the correct DRAM size (Index 60h-6Fh)

Exit

No

MDW; BEJ := DW; HA[22] := '1'; Dat := D1;
MDW; BEJ := DW; HA[22] := '0'; Dat := D2;
MDR; BEJ := DW; HA[22] := '1'; HA = Q;

Is Q=D1?

Yes

8 MB

No

4 MB

A

A

MDW; BEJ := QW; HA[21] := '1'; Dat := D1;
MDW; BEJ := QW; HA[21] := '0'; Dat := D2;
MDR; BEJ := QW; HA[21] := '1'; HA = Q;

MDW; BEJ := DW; HA[20] := '1'; Dat := D1;
MDW; BEJ := DW; HA[20] := '0'; Dat := D2;
MDR; BEJ := DW; HA[20] := '1'; HA = Q;
5.3 L2 Cache Autosizing Flowchart

Start

Perform DRAM Detection Flow

Memory write address=0h, data=D1

- enable L1 (Index-43h bit0='1')
- enable L2, force L2 miss and non-dirty (Index-42h =15h)
- set TAG as 8-bit wide, L2 as 256KB, 1-bank pipelined SRAM (Index-41h =C2h)

Memory line fill address=0h (Burst Read)

- Disable L2 (Index 42h = 00h)

Memory write address=0h, data=D2 (D2 ≠ D1)

- enable L2 as normal condition (Index 42h =01h)

Memory read address=0h, returned data =Q

Is Q =D1?

- No
  - No L2
    - Disable L2
    - Index 42h=00h
  - Exit

- Yes
  - Define a vector (K,i,M) whose values are a specific row of the following matrix.

<table>
<thead>
<tr>
<th>Row</th>
<th>K</th>
<th>i</th>
<th>M</th>
</tr>
</thead>
<tbody>
<tr>
<td>row1</td>
<td>1M</td>
<td>11</td>
<td>512M</td>
</tr>
<tr>
<td>row2</td>
<td>512K</td>
<td>11</td>
<td>512M</td>
</tr>
<tr>
<td>row3</td>
<td>256K</td>
<td>11</td>
<td>512M</td>
</tr>
<tr>
<td>row4</td>
<td>1M</td>
<td>10</td>
<td>256M</td>
</tr>
<tr>
<td>row5</td>
<td>512K</td>
<td>10</td>
<td>256M</td>
</tr>
<tr>
<td>row6</td>
<td>256K</td>
<td>10</td>
<td>256M</td>
</tr>
<tr>
<td>row7</td>
<td>1M</td>
<td>8</td>
<td>64M</td>
</tr>
<tr>
<td>row8</td>
<td>512K</td>
<td>8</td>
<td>64M</td>
</tr>
<tr>
<td>row9</td>
<td>256K</td>
<td>8</td>
<td>64M</td>
</tr>
</tbody>
</table>

Legend :

- K : Define the L2 Cache size
- i : Tag Width
- M : Memory Cacheable region

Assign the value of row1 to the vector (K,i,M)
Assign the value of total DRAM size to M

Is total DRAM size ≥ M?

Yes

disable L2 (Index 42h bit[0] = ‘0’)  
Memory write address=M-8, data=D1

enable L1 (Index 43h bit[0] = ‘0’)  
enable L2, force L2 miss and non-dirty (Index 42h=15h)  
set TAG as i-bit wide, L2 size as K (Index 41h)

Is K =1M ?

Yes

Is K =512K ?

No

set L2 as 2-bank pipelined burst SRAM (Index41h)

Memory line fill burst read address=M-8

Disable L2 (Index 42h bit[0] = ‘0’)

Memory write address=M-8, data=D2 (D2≠D1)

enable L2 as normal condition (Index42h bit[0] = ‘1’)  
Memory line fill burst read address=M-8, returned data=Q

Is Q =D1 ?

Yes

L2 size is K, TAG is i-bit wide

Is K=512K or 1M?

No

L2 is 1-bank pipelined SRAM

Yes

L2 is 2-bank pipelined SRAM

No

Does the process moved to the last row of the matrix?

Yes

L2 error

No

Goto A, and substitute the value of next row to the vector (K, i, M)

Does the process moved to the last row of the matrix?

Yes

Goto A, and substitute the value of next row to the vector (K, i, M)

No

Goto A, and substitute the value of next row to the vector (K, i, M)

A

B

Set the correct L2 configuration (Index 41h,42h)

Exit
5.4 Enable Shadow Region

- DRAM autosizing and initialization
- SRAM autosizing and initialization
- Disable all caches
- Set Index-4Eh and 4Fh to appropriate values (Set the shadowed region writeable)
- Move data from ROM regions to shadowed regions. (Read ROM data and then write to DRAM)
- Set Index-4Eh and 4Fh to zeros (Set shadowed regions not writeable)
- Set Index-4Ch and 4Dh to appropriate values (Set the shadowed region readable)
- Set Index-50h and 51h to appropriate values (Set the shadowed regions cacheable, corresponding to offset x4C and x4D)
- Enable the 1st and 2nd level caches
- Line fill the data of shadowed region to L1 and L2
5.5 Software MESI Test

M1531B integrates an 8K by2 MESI SRAM. Before the chips are shipped out, the RAM cells are tested meticulously. However, for system board debugging and troubleshooting, M1531B has a software test mode for testing internal MESI-SRAM cells. System makers can probe the internal RAM cell by this software scheme, and the BIOS writer is suggested to do so. The procedure is illustrated as below:

1. Initialize:
   - Set index-41h bits [7:6] = ‘11’ (Set PBSRAM)
   - Set index-41h bit [4] = ‘1’ (Enable MESI Software Test Mode)
   - Set index-41h bits [2:1] = ‘01’ (Set Cache size 256K)
   - Set index-41h bit [0] = ‘0’ (Set 8-Bit Tag)

2. Write/Read RAM cell via memory write/read command.

   Write SRAM cell:
   - Command: Memory Data Write
   - Address: HA[15:5] as RAM address, HA[31:17] as don’t care
   - Data: HD[7:0] as RAM write data.

   Read SRAM cell:
   - Command: Memory Data Read
   - Address: HA[15:5] as RAM address, HA[31:17] as don’t care
   - Data: HD[63:0] as don’t care.
   - Read Index-53h bits 7-0 for read data.

When the M1531B is set to the internal MESI-RAM software test mode, only the CPU Memory-Code-Read/Write cycles can be passed to (access) the system memory. Memory-Data-Read/Write cycles are used to access internal MESI-RAM.
Section 6 : Packaging Information

328L BGA Dimension Spec (27 x 27 mm)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>0.55</td>
<td>0.60</td>
<td>0.65</td>
</tr>
<tr>
<td>A2</td>
<td>1.12</td>
<td>1.17</td>
<td>1.22</td>
</tr>
<tr>
<td>( \phi_b )</td>
<td>0.60</td>
<td>0.75</td>
<td>0.90</td>
</tr>
<tr>
<td>c</td>
<td>0.51</td>
<td>0.56</td>
<td>0.61</td>
</tr>
<tr>
<td>D</td>
<td>23.80</td>
<td>24.00</td>
<td>24.20</td>
</tr>
<tr>
<td>D1</td>
<td>23.93</td>
<td>24.13</td>
<td>24.33</td>
</tr>
<tr>
<td>E</td>
<td>23.80</td>
<td>24.00</td>
<td>24.20</td>
</tr>
<tr>
<td>E1</td>
<td>23.93</td>
<td>24.13</td>
<td>24.33</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>1.27</td>
<td></td>
</tr>
<tr>
<td>Hd</td>
<td>26.80</td>
<td>27.00</td>
<td>27.20</td>
</tr>
<tr>
<td>He</td>
<td>26.80</td>
<td>27.00</td>
<td>27.20</td>
</tr>
<tr>
<td>( \theta )</td>
<td>23°</td>
<td>30°</td>
<td>37°</td>
</tr>
<tr>
<td>Y (radius of ball)</td>
<td></td>
<td></td>
<td>0.25</td>
</tr>
</tbody>
</table>
Section 7 : Revision History

Note : Text in shaded areas or underlined indicate differences with previous version.

p.49,62  05/26/97
p.91,92  05/29/97
P.84,91-93 06/11/97
1. The pinout difference between M1531 & M1531B:

<table>
<thead>
<tr>
<th>Pinout</th>
<th>M1531</th>
<th>M1531B</th>
</tr>
</thead>
<tbody>
<tr>
<td>U15</td>
<td>MAB1</td>
<td>MAB1/MA13</td>
</tr>
<tr>
<td>U14</td>
<td>MAB0</td>
<td>MAB0/MA12</td>
</tr>
<tr>
<td>V20</td>
<td>RASJ5</td>
<td>RASJ5/TIO9</td>
</tr>
<tr>
<td>U18</td>
<td>RASJ4</td>
<td>RASJ4/TIO10</td>
</tr>
<tr>
<td>Y20</td>
<td>NC</td>
<td>TIO8</td>
</tr>
<tr>
<td>T17</td>
<td>TIO10/MWEJ1/MKREFRQJ</td>
<td>MWEJ1</td>
</tr>
<tr>
<td>T16</td>
<td>TIO9/SRASJ1</td>
<td>SRASJ1</td>
</tr>
<tr>
<td>T15</td>
<td>TIO8/SCASJ1</td>
<td>SCASJ1</td>
</tr>
</tbody>
</table>

2. SIMM x 4 implementation:

2 Double-Sided DRAM Bank (EDO/FPM)
3. SIMM x 6 implementation:

3 Double-Sided DRAM Bank (EDO/FPM)
4. SIMM x4 + DIMM x 2 implementation:

**M1531B**

- **32-bit SIMM**
- **32-bit SIMM**

**64-bit DIMM**

- **32-bit SIMM**
- **32-bit SIMM**

2 Double-Sided DRAM Bank (EDO/FPM) +
2 Double-Sided SDRAM Bank
5. DIMM x 2 implementation:

2 Double-Sided SDRAM Bank
6. DIMM x 3 implementation:

3 Double-Sided SDRAM Bank
Subject: M1531B Memory Cacheable Size Implementation

Date: March 6, 1997

Part & Version: M1531B

Prepared by: Bruce Hsueh

Approved by: Charles Chiang

1. 64M byte cacheable size implementation:

2. 128M byte cacheable size implementation:
3. 256M byte cacheable size implementation:

```
<table>
<thead>
<tr>
<th>CAS[7..0]</th>
<th>RASJ[4..0]</th>
<th>MAB[1..0]/MA[13..12]</th>
<th>MAA[1..0]</th>
<th>MWEJ1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RASJ6/SCASJ0</td>
<td>RASJ7/SRASJ0</td>
<td>TAG8/SCASJ1</td>
<td>TAG9/SRASJ1</td>
<td>MA[11..2]</td>
</tr>
<tr>
<td>M1531B</td>
<td>MWEJ0</td>
<td>TAG[7..0]</td>
<td>TAG8</td>
<td>RASJ5/TAG9</td>
</tr>
<tr>
<td>TAG RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4. 512M byte cacheable size implementation:

```
<table>
<thead>
<tr>
<th>CAS[7..0]</th>
<th>RASJ[3..0]</th>
<th>MAB[1..0]/MA[13..12]</th>
<th>MAA[1..0]</th>
<th>MWEJ1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RASJ6/SCASJ0</td>
<td>RASJ7/SRASJ0</td>
<td>TAG8/SCASJ1</td>
<td>TAG9/SRASJ1</td>
<td>MA[11..2]</td>
</tr>
<tr>
<td>M1531B</td>
<td>MWEJ0</td>
<td>TAG[7..0]</td>
<td>TAG8</td>
<td>RASJ5/TAG9</td>
</tr>
<tr>
<td>TAG RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Worldwide Distributors and Sales Offices:

**Taiwan**

**Acer Laboratories Inc.**
7F, No. 115 Tung Hsing Street, Taipei 110, Taiwan, R.O.C.
Tel: 886 (2) 762-8800
Fax: 886 (2) 762-6060

**Acer Sertek**
11-15F, 135, Sec. 2, Chien Kuo North Road, Taipei 10479, Taiwan, R.O.C.
Tel: 886 (2) 501-0055
Fax: 886 (2) 501-2521

**Arrow / Ally, Inc.**
11F, 678, Sec. 4, Pa Teh Road, Taipei, Taiwan, R.O.C.
Tel: 886 (2) 768-6399
Fax: 886 (2) 768-6390

**Asec International Inc.**
4F, 223 Chung Yang Road, Nan Kang, Taipei, Taiwan, R.O.C.
Tel: 886 (2) 786-6677
Fax: 886 (2) 786-5257

**Hong Kong**

**Lestina International Ltd.**
14/F, Park Tower 15, Austin Road, Tsimshatsui, Hong Kong
Tel: 852-2735-1736
Fax: 852-2730-5260

**Texny Glorytact (HK) Ltd.**
Unit M, 6/F, Kaiser Estate Phase 3, 11 Hok Yuen Street, Hunghom, Kowloon, Hong Kong
Tel: 852-2765-0118
Fax: 852-2765-0557

**Japan**

**ASCII Corporation**
8-1, Inarimae, Tsukuba-shi Ibaraki, 305, Japan
Tel: 81-298-55-4004
Fax: 81-298-55-1985

**Kanematsu Electronic Components Corp.**
11F Shin-Ohsaki Kangyo Bldg., 6-4, Ohsaki 1-Chome, Shinagawa-Ku, Tokyo, Japan 141
Tel: 81 (3) 3779-7850
Fax: 81 (3) 3779-7898

**Macnica Inc.**
Hakusan High-Tech Park, 1-22-2 Hakusan, Midori-Ku, Yokohama City, Japan 226
Tel: 81 (45) 939-6116
Fax: 81 (45) 939-6117

**Technova Incorporated**
9F Daiichi-Seimei Daini Bldg., 2-14-27, Shin-Yokohama, Kouhoku-ku, Yokohama-Shi, Kanagawa, 222
Tel: 81 (45) 472-7800
Fax: 81 (45) 472-7830

**Korea**

**I&C Microsystems Co., Ltd.**
801, 8/F, Bethel Bldg., 324-1, Yangjae-Dong, Seocho-Ku, Seoul, Korea
Tel: 82 (2) 577-9131
Fax: 82 (2) 577-9130

**Singapore**

**Electronic Resources Ltd.**
205 Kallang Bahru, #04-00, Singapore 339341
Tel: 65-298-0888
Fax: 65-298-1111

**A Li U. S. Office**
1830-B Bering Drive
San Jose, CA 95112 USA
Tel: 1 (408) 467-7456
Fax: 1 (408) 467-7474
This material is recyclable.

Acer Labs products are not licensed for use in medical applications, including, but not limited to, use in life support devices without proper authorization from medical officers. Buyers are requested to inform ALi sales office when planning to use the products for medical applications.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Acer Laboratories Inc. makes no warranty for the use of its products and assumes no responsibility for any errors which may appear in this document nor does it make a commitment to update the information contained herein.

Acer Laboratories Inc. retains the right to make changes to these specifications at any time, without notice.

Contact your local sales office to obtain the latest specifications before placing your order.

ALi is a registered trademark of Acer Laboratories Incorporated and may only be used to identify ALi’s products.

© ACER LABORATORIES INCORPORATED 1993